Integrated circuits

Part 5 February 1982

Digital integrated circuits

ECL 10 000 products

ECL 100 000 products

Dedicated designs

INTEGRATED CIRCUITS

PART 5 - FEBRUARY 1982

DIGITAL INTEGRATED CIRCUITS - ECL

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DATA HANDBOOK SYSTEM

Our Data Handbook System is a comprehensive source of information on electronic components, sub-assemblies and materials; it is made up of four series of handbooks each comprising several parts.

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The several parts contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

Where ratings or specifications differ from those published in the preceding edition they are pointed out by arrows. Where application information is given it is advisory and does not form part of the product specification.

If you need confirmation that the published data about any of our products are the latest available, please contact our representative. He is at your service and will be glad to answer your inquiries.

May 1980

ELECTRON TUBES (BLUE SERIES)

Starting in 1980, new part numbers and corresponding codes are being introduced. The former code of the preceding issue is given in brackets under the new code.

Part 1	February 1980	T1 02-80 (ET1a 12-75)	**Tubes for r.f. heating**
Part 2	April 1980	T2 04-80 (ET1b 08-77)	**Transmitting tubes for communications**
Part 2b	May 1978	ET2b 05-78	**Microwave semiconductors and components** Gunn, Impatt and noise diodes, mixer and detector diodes, backward diodes, varactor diodes, Gunn oscillators, sub-assemblies, circulators and isolators.
Part 3	June 1980	T3 06-80 (ET2a 11-77)	**Klystrons, travelling-wave tubes, microwave diodes**
Part 3	January 1975	ET3 01-75	**Special Quality tubes, miscellaneous devices**
Part 4	September 1980	T4 09-80 (ET2a 11-77)	**Magnetrons**
Part 5	August 1981	T5 08-81 (ET5a 10-79)	**Cathode-ray tubes** Instrument tubes, monitor and display tubes, C.R. tubes for special applications.
Part 6	July 1980	T6 07-80 (ET6 01-77)	**Geiger-Müller tubes**
Part 7	February 1982	T7 02-82 (ET7a 03-77) (ET7b 05-79)	**Gas-filled tubes** Segment indicator tubes, indicator tubes, dry reed contact units, thyratrons, industrial rectifying tubes, ignitrons, high-voltage rectifying tubes, associated accessories.
Part 8	February 1982	T8 02-82 (ET8 07-79)	**Picture tubes and components** Colour TV picture tubes, black and white TV picture tubes, colour monitor tubes for data graphic display, monochrome monitor tubes for data graphic display, components for colour television, components for black and white television and monochrome data graphic display.
Part 9	June 1980	T9 06-80 (ET9 03-78)	**Photo and electron multipliers** Photomultiplier tubes, phototubes, single channel electron multipliers, channel electron multiplier plates.
Part 10	May 1981	T10 05-81 (ET5b 12-78)	**Camera tubes and accessories, image intensifiers**

SEMICONDUCTORS (RED SERIES)

Starting in 1980, new part numbers and corresponding codes are being introduced. The former code of the preceding issue is given in brackets under the new code.

Part 1	**March 1980**	**S1 03-80** **(SC1b 05-77)**	**Diodes** Small-signal germanium diodes, small-signal silicon diodes, special diodes, voltage regulator diodes (< 1,5 W), voltage reference diodes, tuner diodes, rectifier diodes
Part 2	**May 1980**	**S2 05-80** **(SC1a 08-78)**	**Power diodes, thyristors, triacs** Rectifier diodes, voltage regulator diodes (> 1,5 W), rectifier stacks, thyristors, triacs
Part 3	**April 1980**	**S3 04-80** **(SC2 11-77, partly)** **(SC3 01-78, partly)**	**Small-signal transistors**
Part 4	**September 1981**	**S4 09-81** **(SC2 06-79)**	**Low-frequency power transistors**
Part 4a	**December 1978**	**SC4a12-78**	**Transmitting transistors and modules**
Part 5	**October 1980**	**S5 10-80** **(SC3 01-78, partly)**	**Field-effect transistors**
Part 7	**December 1980**	**S7 12-80** **(SC4c 07-78)**	**Microminiature semiconductors for hybrid circuits**
Part 8	**April 1980**	**S8 06-81** **(SC4b 09-78)**	**Devices for optoelectronics** Photosensitive diodes and transistors, light-emitting diodes, displays, photocouplers, infrared sensitive devices, photo-conductive devices
Part 10	**September 1981**	**S10 09-81** **(SC3 01-78, partly)**	**Wideband transistors and wideband hybrid IC modules**

INTEGRATED CIRCUITS (PURPLE SERIES)

Starting in 1980, new part numbers and corresponding codes are being introduced. The former code of the preceding issue is given in brackets under the new code. Books with the purple cover will replace existing red covered editions as each is revised.

Part 1	**May 1980**	**IC1 05-80** **(SC5b 03-77)**	**Bipolar ICs for radio and audio equipment**
Part 2	**May 1980**	**IC2 05-80** **(SC5b 03-77)**	**Bipolar ICs for video equipment**
Part 4	**October 1980**	**IC4 10-80** **(SC6 10-77)**	**Digital integrated circuits** LOCMOS HE4000B family
Part 5	**February 1982**	**IC5 02-82**	**Digital integrated circuits - ECL** ECL10 000 (GX family) ECL100 000 (HX family) Dedicated designs
Part 5a	**November 1976**	**SC5a 11-76**	**Professional analogue integrated circuits**
Part 6b	**August 1979**	**SC6b 08-79**	**ICs for digital systems in radio and television receivers**
Part 7	**May 1981**	**IC7 05-81**	**Signetics Bipolar memories**
Part 8	**May 1981**	**IC8 05-81**	**Signetics Analogue circuits**
Part 9	**November 1981**	**IC9 11-81**	**Signetics TTL Logic**

COMPONENTS AND MATERIALS (GREEN SERIES)

Starting in 1980, new part numbers and corresponding codes are being introduced. The former code of the preceding issue is given in brackets under the new code.

Part 1	October 1981	C1 10-81	**Assemblies for industrial use** PLC modules, PC20 modules, HNIL FZ/30 series, NORbits 60-, 61-, 90-series, input devices, hybrid ICs, peripheral devices
Part 2	June 1981	C2 06-81 (CM3a 09-78)	**FM tuners, television tuners, video modulators, surface acoustic wave filters**
Part 3	January 1981	C3 01-81 (CM3b 10-78)	**Loudspeakers**
Part 4	December 1981	C4 12-81	**Ferroxcube potcores, square cores and cross cores**
Part 4a	November 1978	CM4a 11-78	**Soft Ferrites** Ferrites for radio, audio and television, beads and chokes, FXC potcores and square cores, FXC transformer cores
Part 6	May 1981	C6 05-81 (CM6 04-77)	**Electric motors and accessories** Permanent magnet synchronous motors, stepping motors, direct current motors
Part 7a	January 1979	CM7a 01-79	**Assemblies** Circuit blocks 40-series and CSA70 (L), counter modules 50-series, input/output devices
Part 8	September 1981	C8 09-81 (CM8 06-79)	**Variable mains transformers**
Part 9	August 1979	CM08-79	**Piezoelectric quartz devices** Quartz crystal units, temperature compensated crystal oscillators
Part 10	October 1980	C10 10-80	**Connectors**
Part 11	December 1979	CM11 12-79	**Non-linear resistors** Voltage dependent resistors (VDR), light dependent resistors (LDR), negative temperature coefficient thermistors (NTC), positive temperature coefficient thermistors (PTC)
Part 12	November 1979	CM12 11-79	**Variable resistors and test switches**
Part 13	December 1979	CM13 12-79	**Fixed resistors**
Part 14	April 1980	C14 04-80 (CM2b 02-78)	**Electrolytic and solid capacitors**
Part 15	May 1980	C15 05-80 (CM2b 02-78)	**Film capacitors, ceramic capacitors, variable capacitors**
Part 16	January 1982	C16 01-82 (CM4b 02-79)	**Piezoelectric ceramics, permanent magnet materials**

NUMERICAL AND FUNCTIONAL INDEX

NUMERICAL INDEX GX FAMILY (ECL10 000)

GXB10100	quadruple 3-input NOR gate (1 input common)
GXB10101	quadruple 2-input OR/NOR gate (1 input common)
GXB10102	quadruple 2-input, 3 NOR and 1 OR/NOR gate
GXB10103	quadruple 2-input, 3 OR and 1 OR/NOR gate
GXB10104	quadruple 2-input, 3 AND and 1 AND/NAND gate
GXB10105	triple 2-3-2 input OR/NOR gate
GXB10106	triple 4-3-3 input NOR gate
GXB10107	triple 2-input EXCLUSIVE-OR/EXCLUSIVE-NOR gate
GXB10108	dual 3-input AND/NAND gate
GXB10109	dual 4-5 input OR/NOR gate
GXB10110	dual 3-input/3-output OR gate (line driver)
GXB10111	dual 3-input/3-output NOR gate (line driver)
GXB10112	dual 3-input/3-output (1 OR and 2 NOR) line driver
GXB10113	quadruple EXCLUSIVE-OR gate (with enable)
GXB10114	triple line receiver
GXB10115	quadruple line receiver
GXB10116	triple line receiver
GXB10117	dual 2-wide 2-3 input OR-AND/OR-AND-INVERT gate
GXB10118	dual 2-wide 3-input OR-AND gate
GXB10119	4-wide 4-3-3-3 input OR-AND gate
GXB10121	4-wide OR-AND/OR-AND-INVERT gate
GXB10123	triple BUS driver
GXB10124	quadruple TTL to ECL translator
GXB10125	quadruple ECL to TTL translator
GXB10129	quadruple TTL/IBM bus receiver/latch
GXB10130	dual D-type latch
GXB10131	dual D-type master-slave flip-flop
GXB10132	dual 2-input multiplexer with clocked D-type latches and common reset
GXB10133	quadruple latch with D-type inputs and enable outputs
GXB10134	dual 2-input multiplexer with clocked D-type latches
GXB10135	dual JK master-slave flip-flop
GXB10136	universal hexadecimal counter
GXB10137	universal decade counter
GXB10141	4-bit universal shift register
GXB10145	64-bit, 4-bits per word RAM

GXB10149	1024-bit, 4-bits per word PROM
GXB10155	16-bit, 2-bits per word CAM (content addressable memory)
GXB10158	quadruple 2-to-1 multiplexer (non-inverting)
GXB10159	quadruple 2-to-1 multiplexer (inverter)
GXB10160	12-bit parity checker/generator
GXB10161	3-bit decoder with two enable inputs (1 of 8 lines LOW)
GXB10162	3-bit decoder with two enable inputs (1 of 8 lines HIGH)
GXB10164	8-input multiplexer with enable input
GXB10165	8-input priority encoder
GXB10171	dual 2-bit decoder (one of four lines LOW)
GXB10172	dual 2-bit decoder (one of four lines HIGH)
GXB10173	quadruple 2-input multiplexer with latched outputs
GXB10174	dual 4-to-1 multiplexer (with enable)
GXB10175	quint D-latch with common reset and two wired-OR common clock inputs
GXB10176	hex D-type master-slave flip-flop
GXB10179	look-ahead carry block
GXB10180	dual 2-bit adder/subtractor
GXB10181	4-bit arithmetic logic unit
GXB10188	hex buffer (non-inverting)
GXB10189	hex inverter
GXB10191	hex ECL-MST translator
GXB10192	quadruple current mode BUS driver
GXB10210	high speed dual 3-input/3-output OR gate
GXB10211	high speed dual 3-input/3-output NOR gate
GXB10216	triple differential amplifier
GXB10231	high speed dual D-type master-slave flip-flop
GXB10415; A	1024-bit, 1-bit per word RAM
GXB10422; A	256-word by 4-bit READ/WRITE RAM

NUMERICAL INDEX HX FAMILY (ECL100 000)

HXA100101	triple 5-input OR/NOR gate
HXA100102	quintiple 2-input OR/NOR gate with common enable
HXA100107	quintiple exclusive OR/NOR gate with compare
HXA100112	quadruple double fan-out OR/NOR gate
HXA100114	quintiple differential line receiver
HXA100117	triple 1-2-2-input OR/AND-OR/NAND gate
HXA100118	2-4-4-4-5-input OR/AND-OR/NAND gate
HXA100122	9-bit buffer gate
HXA100123	hex bus driver
HXA100131	triple D flip-flop
HXA100136	multipurpose counting register
HXA100141	8-bit universal shift register
HXA100142	4 x 4 CAM
HXA100145	16 x 4 register file
HXA100150	hex D-type latch flip-flop
HXA100151	hex D-type master-slave flip-flop
HXA100155	quadruple 2-way multiplexer latch
HXA100156	mask-merge selector
HXA100158	8-bit shift matrix
HXA100160	dual 9-bit parity generator/8-bit comparator
HXA100163	dual 8-bit multiplexer
HXA100164	16-input multiplexer
HXA100165	universal priority encoder
HXA100166	9-bit comparator
HXA100170	universal decoder
HXA100171	triple bit 4-way multiplexer
HXA100175	5-bit 100k to 10k interface with latch
HXA100180	fast 6-bit adder
HXA100181	4-bit ALU binary/decimal
HXA100255	5-bit ECL/TTL interface
HXA100415; A	1024 x 1 bit RAM
HXA100422; A	256 x 4 bit RAM
HXA220XXX	master slice logic cell array (500 gates)
HXA220384	4-byte multiplexer
HXA220402	4-byte comparator and multiplexer
HXA230XXX	master slice logic cell array (800 gates)
HXA230101	high level connection matrix 16 → 8

Dedicated designs

SAA1059	125 MHz amplifier and divider-by-32/33
SAB1018; A	sensitive 950 MHz divider-by-256
SAB1077	sensitive 1 GHz divider-by-248/256
SAB1078	650 MHz divider-by-10/11; prescaler
SAB1801D	dual differential D-type flip-flop
SAF1034	1,05 GHz divider-by-4
SAF1534	1,50 GHz divider-by-4

FUNCTIONAL INDEX GX FAMILY (ECL10 000)

(selection guide)

Gates	GXB10100	quadruple 3-input NOR gate (1 input common)
	GXB10101	quadruple 2-input OR/NOR gate (1 input common)
	GXB10102	quadruple 2-input, 3 NOR and 1 OR/NOR gate
	GXB10103	quadruple 2-input, 3 OR and 1 OR/NOR gate
	GXB10104	quadruple 2-input, 3 AND and 1 AND/NAND gate
	GXB10105	triple 2-3-2 input OR/NOR gate
	GXB10106	triple 4-3-3 input NOR gate
	GXB10107	triple 2-input EXCLUSIVE-OR/EXCLUSIVE-NOR gate
	GXB10108	dual 3-input AND/NAND gate
	GXB10109	dual 4-5 input OR/NOR gate
	GXB10110	dual 3-input/3-output OR gate (line driver)
	GXB10111	dual 3-input/3-output NOR gate (line driver)
	GXB10113	quadruple EXCLUSIVE-OR gate (with enable)
	GXB10117	dual 2-wide 2-3 input OR-AND/OR-AND-INVERT gate
	GXB10118	dual 2-wide 3-input OR-AND gate
	GXB10119	4-wide 4-3-3-3 input OR-AND gate
	GXB10121	4-wide OR-AND/OR-AND-INVERT gate
	GXB10210	high speed dual 3-input/3-output OR gate
	GXB10211	high speed dual 3-input/3-output NOR gate
	GXB10216	triple differential amplifier
Interfaces	GXB10112	dual 3-input/3-output (1 OR and 2 NOR) line driver
	GXB10114	triple line receiver
	GXB10115	quadruple line receiver
	GXB10116	triple line receiver
	GXB10123	triple bus driver
	GXB10124	quadruple TTL to ECL translator
	GXB10125	quadruple ECL to TTL translator
	GXB10129	quadruple TTL/IBM bus receiver/latch
	GXB10188	hex buffer (non-inverting)
	GXB10189	hex inverter
	GXB10192	quadruple current mode bus driver
Flip-flops	GXB10130	dual D-type latch
	GXB10131	dual D-type master-slave flip-flop
	GXB10133	quadruple latch with D-type inputs and enable outputs
	GXB10135	dual JK master-slave flip-flop
	GXB10175	quint D-latch with common reset and two wired-OR common clock inputs
	GXB10176	hex D-type master-slave flip-flop
	GXB10231	high speed dual D-type master-slave flip-flop
Counters and registers	GXB10136	universal hexadecimal counter
	GXB10137	universal decade counter
	GXB10141	4-bit universal shift register

Complex	GXB10132	dual 2-input multiplexer with clocked D-type latches and common reset
	GXB10134	dual 2-input multiplexer with clocked D-type latches
	GXB10158	quadruple 2-to-1 multiplexer (non-inverting)
	GXB10159	quadruple 2-to-1 multiplexer (inverting)
	GXB10160	12-bit parity checker/generator
	GXB10161	3-bit decoder with two enable inputs (1 of 8 lines LOW)
	GXB10162	3-bit decoder with two enable input (1 of 8 lines
	GXB10164	8-input multiplexer with enable input
	GXB10165	8-input priority encoder
	GXB10171	dual 2-bit decoder (one of four lines LOW)
	GXB10172	dual 2-bit decoder (one of four lines HIGH)
	GXB10173	quadruple 2-input multiplexer with latched outputs
	GXB10174	dual 4-to-1 multiplexer (with enable)
	GXB10179	look-ahead carry block
	GXB10180	dual 2-bit adder/subtractor
	GXB10181	4-bit arithmetic logic unit
	GXB10191	hex ECL-MST translator
Memories	GXB10145	64-bit, 4-bits per word RAM
	GXB10149	1024-bit, 4-bits per word PROM
	GXB10155	16-bit, 2-bits per word CAM (content addressable memory)
	GXB10415	1024-bit, 1-bit per word RAM
	GXB10422	256-bit, 4-bits per word read/write RAM

FUNCTIONAL INDEX HX FAMILY (ECL100 000)

(selection guide)

Gates	HXA100101	triple 5-input OR/NOR gate
	HXA100102	quintiple 2-input OR/NOR gate with common enable
	HXA100107	quintiple exclusive OR/NOR gate with compare
	HXA100112	quadruple double fan-out OR/NOR gate
	HXA100117	triple 1-2-2-input OR/AND-OR/NAND gate
	HXA100118	2-4-4-4-5-input OR/AND-OR/NAND gate
Driver	HXA100123	hex bus driver
Interface	HXA100114	quintiple differential line receiver
	HXA100122	9-bit buffer gate
	HXA100175	5-bit 100k to 10k interface with latch
	HXA100255	5-bit ECL/TTL interface
Flip-flops	HXA100131	triple D flip-flop
	HXA100150	hex D latch flip-flop
	HXA100151	hex D master-slave flip-flop
Matrix	HXA100158	8-bit shift matrix
Multiplexers	HXA100155	quadruple 2-way multiplexer latch
	HXA100163	dual 8-bit multiplexer
	HXA100164	16-input multiplexer
	HXA100171	triple bit 4-way multiplexer
Memories	HXA100142	4 x 4 CAM
	HXA100415; A	1024 x 1 bit RAM
	HXA100422; A	256 x 4 bit RAM
Counters and registers	HXA100136	multipurpose counting register
	HXA100141	8-bit universal shift register
	HXA100145	16 x 4 register file
Complex	HXA100156	mask-merge selector
	HXA100160	dual 9-bit parity generator/8-bit comparator
	HXA100165	universal priority encoder
	HXA100166	9-bit comparator
	HXA100170	universal decoder
	HXA100180	fast 6-bit adder
	HXA100181	4-bit ALU binary/decimal
Gate array	HXA220XXX	MLA24 (500 gates)
	HXA220384	4-byte multiplexer
	HXA220402	4-byte comparator and multiplexer
	HXA230XXX	MLA36 (800 gates)
	HXA230101	high level connection matrix 16 → 8

GENERAL

Preface
Type designation code
Rating systems
Definition of letter symbols
Soldering instructions

PREFACE TO DATA

The published data comprise useful design information and criteria on which to base acceptance testing of the circuits. For ease of reference, the data on each circuit are grouped according to the several headings as described below. For an explanation of the letter symbols used in designating terminals and performance, the electrical and logic quantities pertaining to them and for an explanation of the type designation code, see the chapters **type designation code** and **letter symbols.**

Quick reference data

The main properties of the integrated circuit summarized for quick reference.

Circuit diagram

Circuit diagrams and logic symbols are given to illustrate the circuit function. The diagrams show only essential elements, parasitic elements due to the method of manufacture normally being omitted. The manufacturer reserves the right to make minor changes to improve manufacturability.

Logic symbols (digital circuits)

Graphical logic symbols accord with MIL standard 806B. Supplementary drawings correlate logic functions with pin locations as a help to laying out printed circuit boards.

Ratings

Ratings are limits beyond which the serviceability of the integrated circuit may be impaired. The ratings given here are in accordance with the Absolute Maximum System as defined in publication no. 134 of the International Electrical Commission; for further details see chapter Rating Systems.

If a circuit is used under the conditions set forth in the sections Characteristics and Additional System Design Data, its operation within the ratings is ensured.

Characteristics

Characteristics are measurable properties of the integrated circuit described. Under a specific set of test conditions compliance with limit values given under this heading establishes the specified performance of the circuit; this can be used as a criterion for acceptance testing.

Values cited as typical are given for information only and are not subject to any form of guarantee.

Application information

Under this heading, practical circuit connections and the resulting performance are described. Care has been taken to ensure the accuracy and completeness of the information given, but no liability therefor is assumed, nor is licence under any patent implied.

PRO ELECTRON TYPE DESIGNATION CODE FOR INTEGRATED CIRCUITS

This type nomenclature applies to semiconductor monolithic, semiconductor multi-chip, thin-film, thick-film and hybrid integrated circuits.

A basic number consists of:

THREE LETTERS FOLLOWED BY A SERIAL NUMBER

FIRST AND SECOND LETTER

1. DIGITAL FAMILY CIRCUITS

   The FIRST TWO LETTERS identify the FAMILY (see note 1).

2. SOLITARY CIRCUITS

   The FIRST LETTER divides the solitary circuits into:

   S : Solitary digital circuits
   T : Analogue circuits
   U : Mixed analogue/digital circuits

   The SECOND LETTER is a serial letter without any further significance except 'H' which stands for hybrid circuits.

3. MICROPROCESSORS

   The FIRST TWO LETTERS identify microprocessors and correlated circuits as follows:

   MA : Microcomputer / Central processing unit
   MB : Slice processor (see note 2)
   MD : Correlated memories
   ME : Other correlated circuits (interface, clock, peripheral controller, etc.)

THIRD LETTER

It indicates the operating ambient temperature range.
The letters A to G give information about the temperature:

A : temperature range not specified
B : 0 to + 70 °C
C : −55 to + 125 °C
D : −25 to + 70 °C
E : −25 to + 85 °C
F : −40 to + 85 °C
G : −55 to + 85 °C

If a circuit is published for another temperature range, the letter indicating a narrower temperature range may be used or the letter 'A'.

Example: the range 0 to + 75 °C can be indicated by 'B' or 'A'.

SERIAL NUMBER

This may be either a 4-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

To the basic type number may be added:

A VERSION LETTER

Indicates a minor variant of the basic type or the package. Except for 'Z', which means customized wiring, the letter has no fixed meaning. The following letters are recommended for package variants:

C : for cylindrical
D : for ceramic DIL
F : for flat pack
L : for leadless chip carrier
P : for plastic DIL
Q : for QIL
U : for uncased chip

Alternatively a TWO LETTER SUFFIX may be used instead of a single package version letter, if the manufacturer (sponsor) wishes to give more information.

FIRST LETTER: General shape

C : Cylindrical
D : Dual-in-line (DIL)
E : Power DIL (with external heatsink)
F : Flat (leads on 2 sides)
G : Flat (leads on 4 sides)
K : Diamond (TO-3 family)
M : Multiple-in-line (except Dual-, Triple-, Quadruple-in-line)
Q : Quadruple-in-line (QIL)
R : Power QIL (with external heatsink)
S : Single-in-line
T : Triple-in-line

SECOND LETTER: Material

C : Metal-ceramic
G : Glass-ceramic (cerdip)
M : Metal
P : Plastic

A hyphen precedes the suffix to avoid confusion with a version letter.

Notes

1. A logic family is an assembly of digital circuits designed to be interconnected and defined by its basic electrical characteristics (such as: supply voltage, power consumption, propagation delay, noise immunity).
2. By 'slice processor' is meant: a functional slice of microprocessor.

RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

DEFINITIONS OF TERMS USED

Electronic device. An electronic tube or valve, transistor or other semiconductor device.

Note
This definition excludes inductors, capacitors, resistors and similar components.

Characteristic. A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

Bogey electronic device. An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

Rating. A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note
Limiting conditions may be either maxima or minima.

Rating system. The set of principles upon which ratings are established and which determine their interpretation.

Note
The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

LETTER SYMBOLS FOR LINEAR INTEGRATED CIRCUITS

The voltages and currents are normally related to the terminals to which they are applied or at which they appear. Each terminal is indicated by a number. In appropriate cases, voltages, currents etc. pertinent to one or more of the circuit elements (transistors, diodes) are given in which case symbols are based on the recommendations as published in IEC Publication 148.

Quantity symbols

1. Instantaneous values of current, voltage and power, which vary with time are represented by the appropriate lower case letter.

   Examples: i, v, p

2. Maximum (peak), average, d.c. and root-mean-square values are represented by the appropriate upper case letter.

   Examples: I, V, P

Polarity of current and voltage

A current is defined to be positive when its conventional direction of flow is into the device.

A voltage is measured with respect to the reference terminal, which is indicated by the subscripts. Its polarity is defined to be positive when the potential is higher on the measured terminal than on the reference terminal.

Subscripts

For currents the number behind the quantity symbol indicates the terminal carrying the current.

Examples: I_2, i_{14}

For voltages normally two number subscripts are used, connected by a hyphen. The first number indicates the terminal at which the voltage is measured and the second subscript the reference terminal. Where there is no possibility of confusion the second subscript may be omitted.

Examples: $V_{2\text{-}12}$, $v_{14\text{-}2}$, V_5, v_8

To distinguish between maximum (peak), average, d.c. and root-mean-square values the following subscripts are added:

For maximum (peak) values	M or m
For average values	AV or av
For root-mean-square values	(RMS) or (rms)
For d.c. values	no additional subscripts

The upper case subscripts indicate total values. The lower case subscripts indicate values of varying components:

Examples: I_2, I_{2AV}, $I_{2(rms)}$, $I_{2(RMS)}$

If in appropriate cases quantity symbols are pertinent to single elements of a circuit (transistors or diodes), the normal subscripts for semiconductor devices can be used.

Examples: V_{CBO}, V_{be}, V_{CES}, I_C

List of subscripts:

E, e = Emitter terminal	(BR) = Break-down
B, b = Base terminal for bipolar transistors	M, m = Maximum (peak) value
	AV, av = Average value
C, c = Collector terminal	(RMS), (rms) = R.M.S. value
S, s = Substrate for bipolar transistor circuits	

Electrical parameter symbols

The values of four pole matrix parameters or other resistances, impedances, admittances, etc., inherent in the device, are represented by the lower case symbol with appropriate subscript.

Examples: h_i, z_f, y_o, k_r

Subscripts for parameter symbols

1. The static values of parameters are indicated by upper case subscripts.

   Examples: h_{FE}, h_I

2. The small signal values of parameters are indicated by lower case subscripts.

   Examples: h_i, z_o

3. The first subscript, in matrix notation identifies the element of the four pole matrix.

   i (for 11) = input
   o (for 22) = output
   f (for 21) = forward transfer
   r (for 12) = reverse transfer

   Examples: $V_1 = h_i I_1 + h_r V_2$; $I_2 = h_f I_1 + h_o V_2$

   The voltage and current symbols in matrix notation are indicated by a single digit subscript.
   The subscript 1 = input; the subscript 2 = output.
   The voltages and currents in these equations may be complex quantities.

4. A second subscript is used only for separate circuit elements (e.g. transistors) to identify the circuit configuration:

   e = common emitter; b = common base; c = common collector

5. If it is necessary to distinguish between real and imaginary parts of the four pole parameters, the following notation may be used:

   R_e (h_i) etc. . . . for the real part
   I_m (h_i) etc. . . . for the imaginary part

SOLDERING RECOMMENDATIONS

To assure reliable and consistent connections particular attention should be paid to:

1. **Flux**

   A non-active flux is recommended. Where active fluxes are employed, great care in subsequent substrate cleaning must be exercised.

2. **Metal-alloy solder or solder paste**

   Correct choice of solder alloy or solder paste to be employed e.g. 62% Sn, 36% Pb, 2% Ag or 60% Sn/40% Pb. Any paste used should contain at least 85% metal dry weight.

3. **Soldering temperature**

   This will vary according to the actual method employed.

REFLOW SOLDERING

The preferred technique for mounting miniature or short leaded components on hybrid thick and thin-film is the method of reflow soldering.

Having first been fluxed, all components are positioned on the substrate. The slight adhesive force of the flux is sufficient to keep the components in place. Solder paste contains a flux and has therefore good inherent adhesive properties which eases positioning of the components.

With the components in position the substrate is heated to a point where the solder begins to flow. This can be done on a heating plate or on a conveyor belt running through an infrared tunnel. The maximum allowed temperature of the plastic body of a device must be kept below 280 °C during the soldering cycle.

After cooling the connections may be visually inspected and, where necessary, repaired with a light soldering iron. Finally any remaining flux must be removed carefully.

IMMERSION SOLDERING

Where a complete substrate or printed circuit board is immersed in solder:

a. The temperature of the soldering bath should not exceed 280 °C.
b. The duration of the soldering cycle should not exceed 10 seconds.
c. Forced cooling may be applied.

HAND SOLDERING

It is possible to solder miniature devices with a light hand-held soldering iron, but this method has obvious drawbacks and should therefore be restricted to laboratory use and/or incidental repairs on production circuits.

1. It is time-consuming and expensive.
2. The device cannot be positioned accurately and therefore the connecting tabs may come into contact with the substrate and damage it.
3. There is a great risk of breaking either substrate or even internal connections inside the encapsulation.
4. The envelope may be damaged by the iron.

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

FAMILY SPECIFICATIONS

Introduction
Handling ECL devices
Definitions of symbols
ECL10 000 (GX family)
ECL100 000 (HX family)

INTRODUCTION TO THE ECL DATA HANDBOOK

Emitter coupled logic

Emitter coupled logic (ECL) is the fastest logic type available for practical use today. Traditionally developed for the high-speed elements of mainframe computers, it is being increasingly applied wherever ultra-high switching speeds are required. Typical applications include signal generation and processing, digital switching and filtering networks, arithmetic and logic units of computers, optical transmission line interfaces and digital video systems.

This data book describes the 10 000 and 100 000 ranges of ECL as well as the high speed memories and standard and semi-custom LSI circuits fabricated using ECL. These last categories are particularly valuable to the entrepreneurial circuit designer, being suitable for conventional and state of the art designs. The semi-custom cell arrays, with a speed-power product of only 3 pJ per gate, are most useful where ECL operating frequencies, of up to 300 MHz, combined with low power consumption are critical factors of circuit design.

General

The table below shows a comparison of the propagation delay and switched power per gate of 100 000 ECL against other logic styles.

conventional logic	gate delay ns	switched power mW
TTL	10	10
LS TTL	9	2
S TTL	3	20
10 000 ECL	2	25
new logic		
ALS	3,5	1
FAST	2	4
100 000 ECL	0,75	40

ECLis a current switching logic. In the base gate of Fig. 1, the current from the current source flows continuously, through either branch A or branch B. The exponential change of emitter current with base-emitter voltage results in a rapid switching of the current path. This sensitivity allows a considerable amount of noise immunity to be built into the circuits. Furthermore, the constant current nature of the circuits minimizes voltage fluctuations (noise), due to switching, in the supply lines, eliminating the need for ultra-fast voltage regulators. The effects of switching output loads are isolated from the inputs by the use of separate supplies for the outputs.

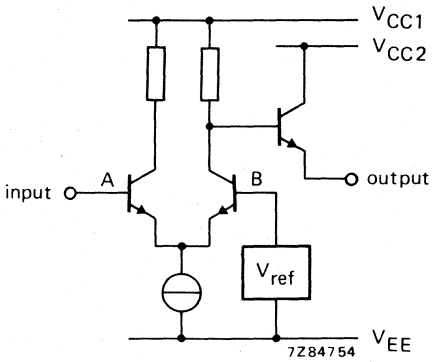


Fig. 1 ECL is a current-switching logic. The current drawn from the supply voltage (V_{CC1}) is thus independent of the state of the inputs. The use of a separate supply (V_{CC2}) for the output load minimizes the effect of output noise on the inputs.

Since there are no internal load resistors on the outputs, these can be OR-wired, thus saving additional circuitry. External pull-down resistors are thus required on outputs. Most of the circuits provide complementary outputs, allowing simpler system design and eliminating inverters that would otherwise increase power consumption and circuit cost.

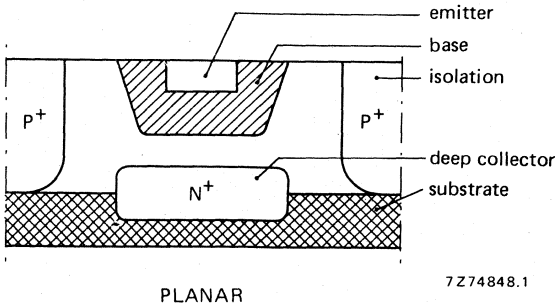
The 100 000 range of ECL is fully compensated for changes in both temperature and voltage. The 10 000 range has voltage compensation only in the memories and cell arrays, with no compensation in the logic circuits.

The high current drive capability of 100 000 ECL, as shown in the table on page 1, is a valuable feature when switching signals at speeds that call for transmission line techniques. High current drive contributes to the signal-to-noise ratio achieved at the receiving end. It also permits a large fan-out, since all inputs have an internal pull-down resistor of typically 50 kΩ to V_{EE}.

TECHNICAL FEATURES OF ECL

The technology

A conventional planar process is used for the 10 000 ECL range, with a density of about ten gates per mm^2 and a delay of 2 ns per gate. This junction-isolated process, achieving about 1,5 GHz transition frequency, is shown schematically in Fig. 2.



PLANAR

Fig. 2 Junction-isolated planar technique used for 10 000 ECL.

To achieve the delay of only 0,75 ns per gate and the density of 20 gates per mm^2 of the 100 000 ECL range (including the memories and LSI circuits of the 10 000 range), an oxide-isolated SUBILO process is used. This state of the art technique, shown in Fig. 3, achieves a transition frequency of about 4,5 GHz.

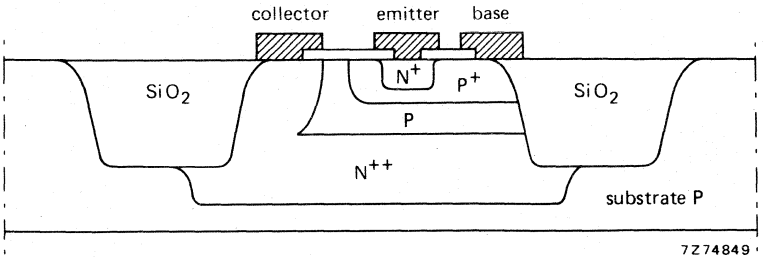


Fig. 3 The SUBILO process uses silicon oxide between devices instead of the p^+ regions used in the planar process.

Typical circuits

Figures 4 and 5 show basic schematic diagrams of an OR gate, implemented in 10 000 and 100 000 ECL respectively.

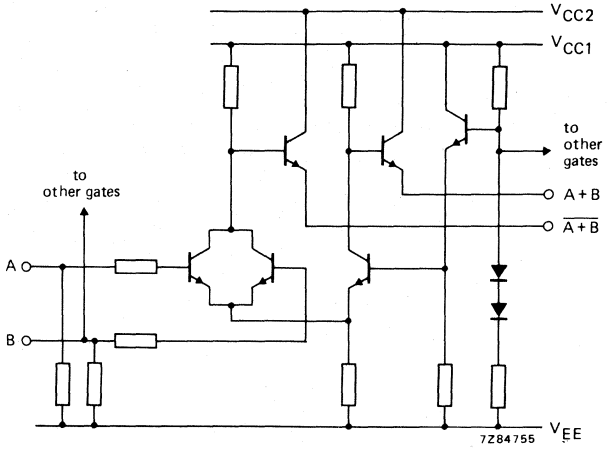


Fig. 4 OR/NOR gate of 10 000 ECL (simplified).
V_{EE} = −5,2 V; V_{CC1} = V_{CC2} = 0 V (ground)
t_{PHL} = t_{PLH} ⩽ 2,9 ns; typ. 2 ns.

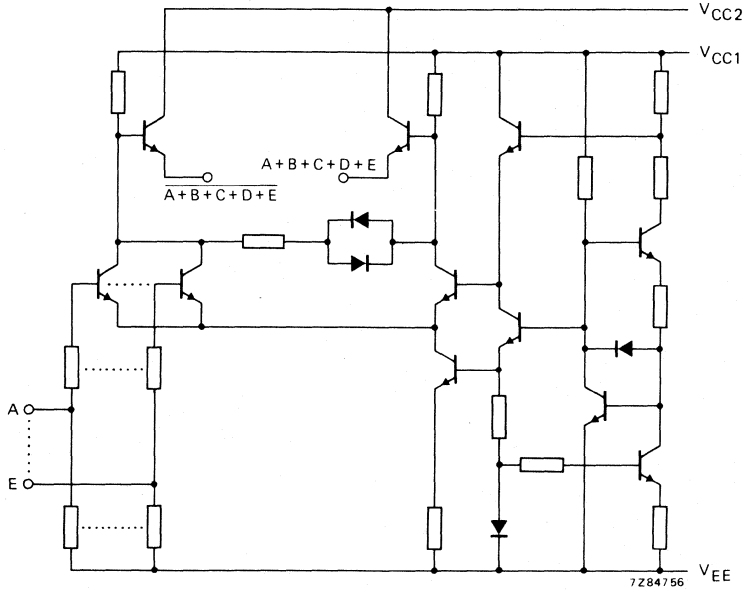


Fig. 5 OR/NOR gate of 100 000 ECL (simplified).
V_{BE} = −4,5 V; V_{CC1} = V_{CC2} = 0 V (ground). t_{PLH} = t_{PHL} = typ. 0,75 ns; range 0,45 to 0,95 ns.

Printed circuit design for ECL circuits

The switching speed of ECL requires that connections are treated as transmission lines, see Fig. 6. The output of the ECL device can be considered as a voltage source, feeding a transmission line of characteristic impedance Z_O, with a load impedance Z_L. The relationship between a voltage step function at the source and that resulting at the load follows the equation:

$$V_L = V_S (1 + \rho),$$

where ρ is the reflection coefficient, determined by the mismatch of the characteristic impedance, Z_O, and the load impedance Z_L:

$$\rho = \frac{Z_L - Z_O}{Z_L + Z_O}.$$

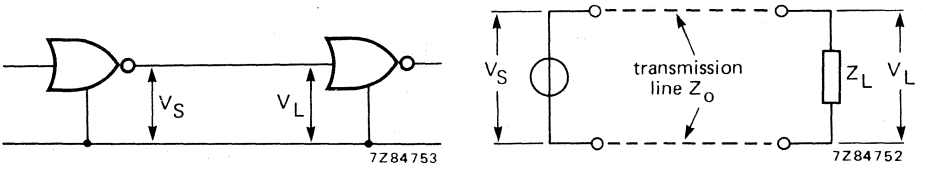


Fig. 6 The high switching speed of ECL requires that connections are treated as transmission lines with characteristic impedance Z_O, feeding a load impedance Z_L.

Reflections along the line can be prevented ($\rho = 0$) by matching the load impedance to the characteristic impedance of the line ($Z_L = Z_O$). However, the noise margins of the ECL circuits are such that a 15% loss in transmission can be tolerated. This corresponds to an approximate 30% variation between Z_L and Z_O.

Microstrip or stripline techniques are recommended for accurate repetition of the distributed inductance and capacitance of printed circuits: these factors determine the characteristic impedance of the connections:

$$Z_O = \sqrt{\frac{L}{C}},$$

where L and C are the inductance and capacitance per unit length.

The signal delay along these transmission lines is also determined by the distributed inductance and capacitance, being proportional to $\sqrt{LC}$. This parameter greatly affects system performance and care must be taken when determining the dimensions and spacing of connections.

Power consumption of ECL systems is relatively high and care must be taken to avoid unduly high voltage drops along supply lines. The use of large-cross-section conductors is recommended. For large circuits, several supply lines may be considered necessary.

HANDLING ECL DEVICES

ECL integrated circuits can be accidentally damaged by over-voltages due to electrostatic discharges from operators, equipment, work surfaces, packing material etc.

Caution

Testing or handling and mounting call for special attention to personal safety. Personnel handling ECL devices should normally be connected to ground via a resistor.

Storage and transport

Store and transport the circuits in their original packing. Alternatively, use may be made of a conductive material or special IC carrier that connects all leads together.

Testing or handling

Work on a conductive surface (e.g. metal table top) when testing the circuits or transferring them from one carrier to another. Electrically connect the person doing the testing or handling to the conductive surface, for example by a metal bracelet and a conductive cord or chain. Connect all testing and handling equipment to the same surface.
Signals should not be applied to the inputs while the device power supply is off. All unused input leads can be left unconnected unless otherwise specified in the individual data sheets.

Mounting

Mount ECL integrated circuits on printed circuit boards *after* all other components have been mounted. Take care that the circuits themselves, metal parts of the board, mounting tools, and the person doing the mounting are kept at the same electric (ground) potential. If it is impossible to ground the printed-circuit board the person mounting the circuits should touch the board before bringing ECL circuits into contact with it.

Soldering

Soldering iron tips, including those of low-voltage irons, or soldering baths should also be kept at the same potential as the ECL circuits and the board.

Static charges

Dress personnel in clothing of non-electrostatic material (no wool, silk or synthetic fibres). After the ECL circuits have been mounted on the board proper handling precautions should still be observed. Until the sub-assemblies are inserted into a complete system in which the proper voltages are supplied, the board is no more than an extension of the leads of the device mounted on the board. To prevent static charges from being transmitted through the board wiring to the device it is recommended that conductive clips or conductive tape be put on the circuit board terminals.

Transient voltages

To prevent permanent damage due to transient voltages, do not insert or remove ECL devices, or printed-circuit boards with ECL devices, from test sockets or systems with power on.

Voltage surges

Beware of voltage surges due to switching electrical equipment on or off, relays and power lines.

DEFINITIONS OF SYMBOLS AND TERMS

The symbols and terms used in the data sheets have been chosen to agree with the standards of the International Electrotechnical Commission. The relative values of the specified conditions and limits are referenced to an algebraic scale. The extremities of the scale are:

"A" is the most positive value of a spread (value closest to positive infinity).
"B" is the most negative value of a spread (value closest to negative infinity).

Currents

Positive-current is defined as conventional current flow into a device pin. Negative current is defined as conventional current flow out of a device pin.

I_{EE} Power supply current. The current required by each device from the V_{EE} supply. This value represents only the internal current required by the specified device, and does not include the current required for loads or terminations.

I_{IH} Input current HIGH. The current flowing into a device pin with the specified V_{IH} applied to the input. This value represents the worst case d.c. input load that a device presents to a driving element.

I_{IHA} The most positive value of I_{IH}.

I_{IHB} The most negative value of I_{IH}.

I_{IL} Input current LOW. The current flowing into a device pin with the specified V_{IL} applied to the input.

I_{ILA} The most positive value of I_{IL}.

I_{ILB} The most negative value of I_{IL}.

Voltages

V_T Termination voltage for external output resistors (usually $V_T = -2$ V).

V_{BB} Bias voltage. The internally generated reference voltage and output threshold levels.

V_{CC} Circuit ground. This is the most positive potential in an ECL system and it is used as the reference level for other voltages.

V_{EE} Power supply voltage. It is the most negative potential in the system.

V_{IH} Input voltage HIGH. The range of input voltages that represents a logic HIGH level in the system.

V_{IHB} The most negative V_{IH}. This value represents the guaranteed input HIGH threshold for the device.

V_{IHA} The most positive V_{IH}.

V_{IL}	Input voltage LOW. The range of input voltages that represents a logic LOW level in the system.
V_{ILB}	The most negative V_{IL}.
V_{ILA}	The most positive V_{IL}. This value represents the guaranteed input LOW threshold for the device.
V_{OH}	Output voltage HIGH. The range of voltages at an output terminal with the specified output loading and with the inputs conditioned to establish a HIGH level at the outputs.
V_{OHB}	The most negative V_{OH} under the specified input and loading conditions.
V_{OHA}	The most positive V_{OH} under the specified input and loading conditions.
V_{OHC}	The output HIGH corner point or guaranteed HIGH output voltage with the inputs set to their respective threshold levels.
V_{OL}	Output voltage LOW. The range of voltages at an output terminal with the specified output loading and with the inputs conditioned to establish a LOW level at the output.
V_{OLA}	The most positive V_{OL} under the specified input and loading conditions.
V_{OLB}	The most negative V_{OL} under the specified input and loading conditions.
V_{OLC}	The output LOW corner point or guaranteed LOW output voltage with the inputs set to their respective threshold levels.

AC switching parameters

t_{AA}	Address access time. 50% points of address input pulse to data output pulse.
t_{ACS}	Chip-select access time. 50% points of select pulse to data output pulse-leading edges.
$t_h - t_{hold}$	Hold time. Minimum time which a signal must be present and remain static *after* an active transition of the control input to guarantee the recognition of the data.
$t_s - t_{set\text{-}up}$	Set-up time. Minimum time which a signal must be present and remain static *before* an active transition at the control input to guarantee the recognition of the data.
t_w	Pulse width. The time between 50% amplitude points on the leading and trailing edges of a pulse to ensure proper action.
$t_{THL} - t_f$	Fall time. The transition time between two specified reference points (20 and 80%) on a waveform which is changing from HIGH to LOW.
$t_{TLH} - t_r$	Rise time. The time between two specified reference points (20 and 80%) on a waveform which is changing from LOW to HIGH.
$t_{PLH} - t_{pdr}$	Rise propagation delay time. The time between the 50% points on the input and output voltage waveforms with the output changing from the defined LOW level to the defined HIGH level.
$t_{PHL} - t_{pdf}$	Fall propagation delay time. The time between the 50% points on the input and output voltage waveforms with the output changing from the defined HIGH level to the defined LOW level.
t_{WSCS} t_{WHCS}	Set-up or hold time at 50% points of leading/trailing edges of a chip select pulse to a write enable pulse.
t_{RCS}	Chip select recovery time. Fifty per cent points of trailing edges of chip select output pulse to data output pulse.

Miscellaneous

$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Voltage compensation.
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	The ratio of the change in the $\frac{\text{LOW}}{\text{HIGH}}$ output voltage to the change in the supply voltage.
R_L	Load resistance. (Usually 50 Ω.)

ECL10 000 (GX FAMILY)

These specifications cover the common electrical characteristics of the ECL10 000 (GX family), unless otherwise specified in the individual device data sheet.

RATINGS

Supply voltage	V_{EE}	−8 V
Input voltage	V_I	0 to V_{EE} V
Output current	I_O	50 mA
Storage temperature	T_{stg}	−55 to +125 °C

D.C. CHARACTERISTICS at V_{CC} = ground; V_{EE} = −5,2 V

Each CX circuit has been designed to meet the d.c. specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed-circuit board and transverse air flow > 2,5 m/s is maintained. Test values are given in the table and defined in the figure.

Test parameters

	temperature °C			unit
	−30	+25	+85	
V_{IHA}	−890	−810	−700	mV
V_{IHB}	−1205	−1105	−1035	mV
V_{ILA}	−1500	−1475	−1440	mV
V_{ILB}	−1890	−1850	−1825	mV

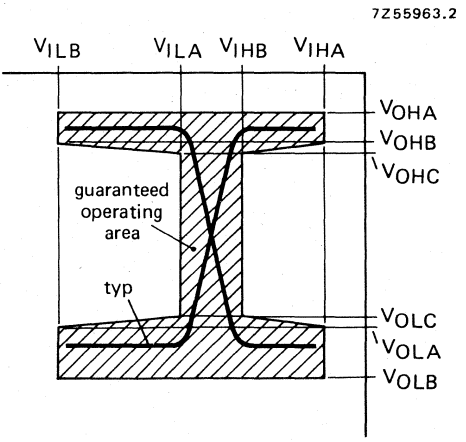


Fig. 1 Transfer characteristics.

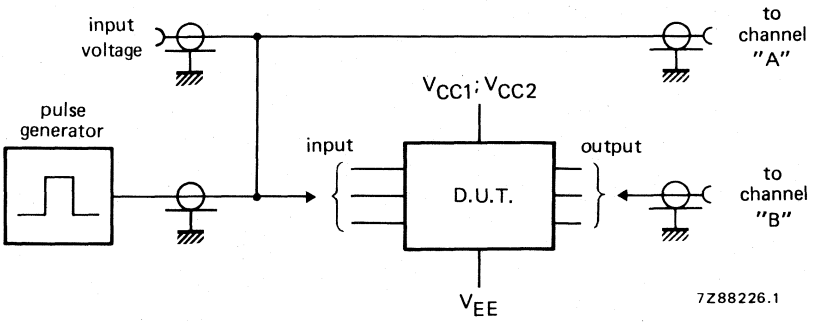


Fig. 2 Switching times test circuit.

$V_{CC1} = V_{CC2} = +2,0$ V
$V_{EE} = -3,2$ V

input pulse:

$t_r = t_f = 2,0 \pm 0,2$ ns
between 20 and 80%
$V_{IH} = +1,1$ V
$V_{IL} = +0,3$ V

Test table $V_{CC} = 0$ V (ground); $V_{EE} = -5,2$ V; $R_L = 50\ \Omega$ to -2 V.

characteristic	symbol	temperature (°C)			unit	remarks
		−30	+25	+85		
Output voltage HIGH	V_{OHA}	−890	−810	−700	mV	
	V_{OHB}	−1060	−960	−890	mV	
Output threshold voltage HIGH	V_{OHC}	−1080	−980	−960	mV	
Output threshold voltage LOW	V_{OLC}	−1655	−1630	−1595	mV	
Output voltage LOW	V_{OLA}	−1675	−1650	−1615	mV	
	V_{OLB}	−1890	−1850	−1825	mV	

Notes

1. Input resistance is positive at any frequency.
2. Non-specified input pins should be connected to V_{ILmin} or left open.
3. Input and output cables to the oscilloscope are 50 Ω coaxial cables with equal length.
4. Input impedance of the oscilloscope is 50 Ω.
6. The unmatched wire stub between coaxial cable and pins under test must be less than 6 mm long for proper test.

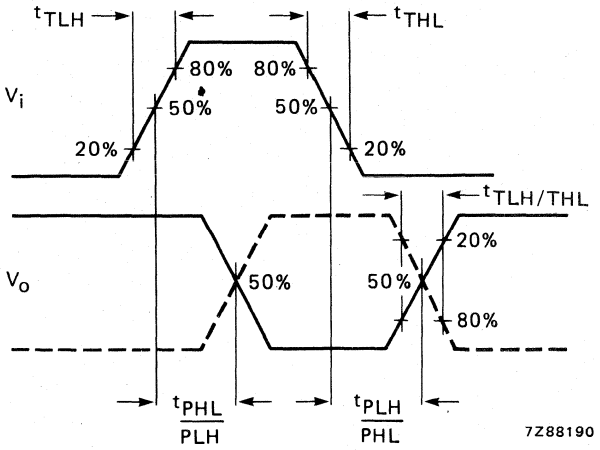


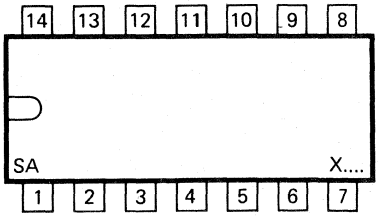
Fig. 3 Propagation delay waveform.

ORDERING INFORMATION

Code GXB10415 AL D

- package
- electrical specifications
- serial number
- series

MARKING



SA quality level A
SB quality level B (with burn-in)
X origin
.... date code

ECL100 000 (HX FAMILY)

ECL100 000 is a standard ECL family with subnanosecond switching speed. It interfaces directly with the 2 ns ECL circuits.

The use of current-switch emitter-follower gates offers the following advantages:

- excellent a.c. characteristics
- compatibility with existing ECL logic and memories
- high fan-out capability
- complementary outputs
- good noise immunity
- external wired-OR capability
- full compensation and extended temperature characteristics
- series gating capability

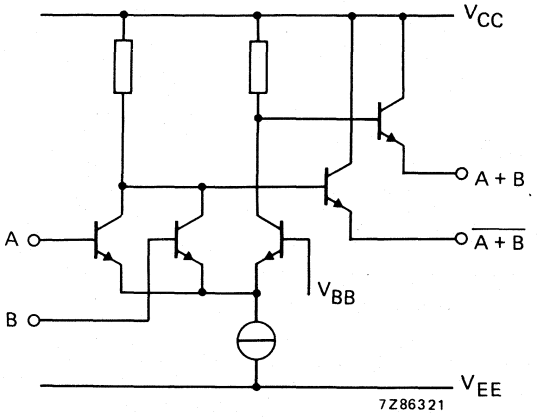


Fig. 1 ECL current-switch emitter follower.

The basic gate consists of three blocks:
– the current switch
– the output emitter followers
– the reference network.

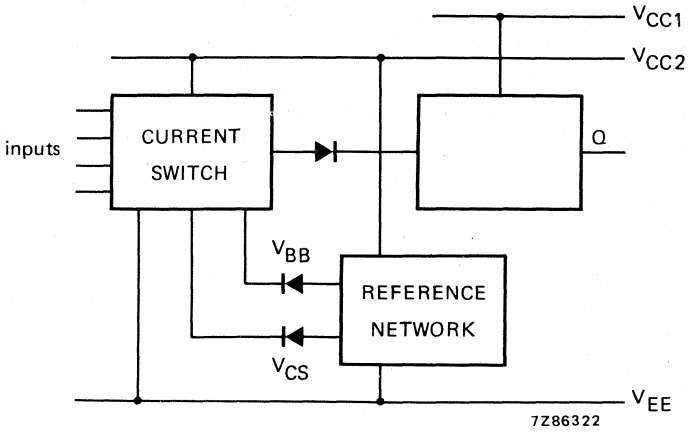


Fig. 2 ECL gate.

The output emitter followers provide high drive capability; the reference network sets the switching threshold and current source.bias voltage.

ECL100 000 is voltage and temperature compensated, providing constant levels and thresholds independent of voltage and temperature changes.

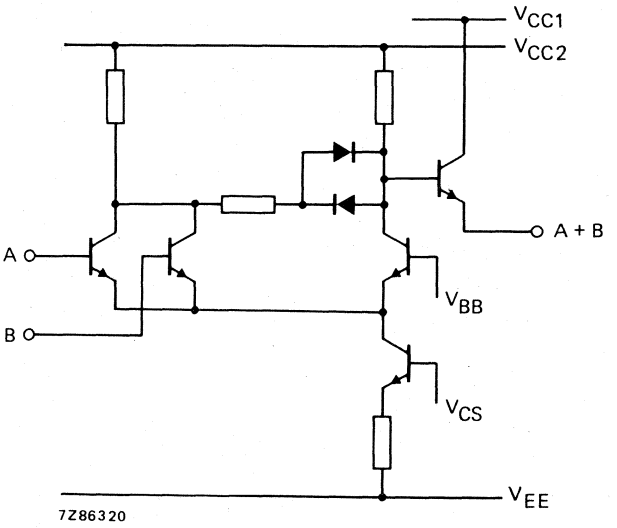


Fig. 3 Temperature compensation.

Temperature compensation is realized by adding a cross connect branch between the collector nodes of the current switch and driving the current source with a temperature-independent bias network.

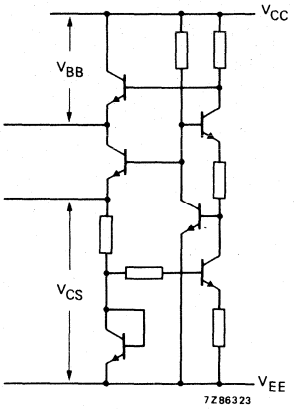


Fig. 4 Reference network.

The reference network generates, regulates and temperature-compensates the internal reference voltages V_{BB} and V_{CS}.

All inputs have a 50 kΩ (typical) pull-down resistor internally connected to V_{EE}. Outputs do not have pull-down resistors, but have wired-OR compatability. They require external load resistors.

Regulation performance

All voltage levels are specified with a 50 Ω load to −2 V at all outputs to provide transmission line drive capability.

Output levels and thresholds are constant over the temperature range 0 °C to 85 °C at V_{EE} = −4,5 V and the supply voltage range −4,2 V to −5,7 V at T_{amb} = 25 °C.

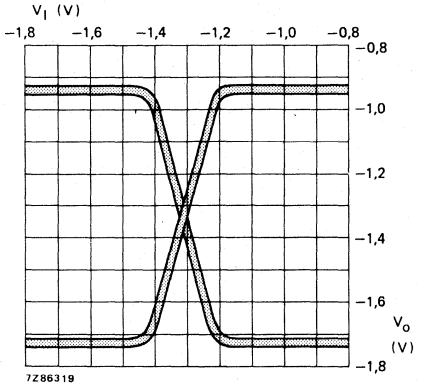


Fig. 5 Output voltage as a function of input voltage at T_{amb} = 25 °C.

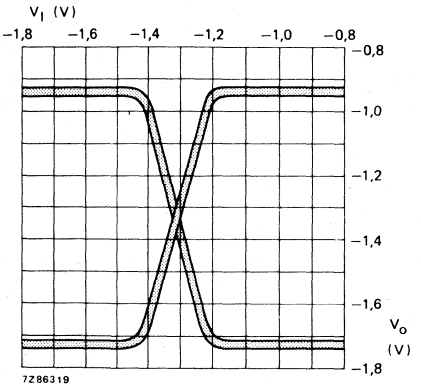


Fig. 6 Output voltage as a function of input voltage at V_{EE} = −4,5 V.

These specifications cover the common electrical characteristics of the ECL100 000 (HX family), unless otherwise specified in the individual device data sheet.

RATINGS

Supply voltage	V_{EE}	−7 V
Input voltage	V_I	0 to −4,5 V
Output current	I_O	55 mA
Storage temperature	T_{stg}	−55 to +125 °C

D.C. CHARACTERISTICS at V_{CC} = ground; V_{EE} = −4,5 V

Each HX circuit has been designed to meet the d.c. specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed-circuit board and transverse air flow > 2,5 m/s is maintained. Test values are given in the table and defined in the figure.

Test table V_{CC} = 0 V (ground), V_{EE} = −4,5 V; T_{amb} = −30 to +85 °C; R_L = 50 Ω to −2 V.

characteristics	symbol	value	unit
Input voltage HIGH	V_{IHA}	880	mV
	V_{IHB}	1165	mV
Input voltage LOW	V_{ILA}	1475	mV
	V_{ILB}	1810	mV
Output voltage HIGH	V_{OHA}	880	mV
	V_{OHB}	1025	mV
Output voltage LOW	V_{OLA}	1620	mV
	V_{OLB}	1810	mV
Output threshold HIGH	V_{OHC}	1035	mV
LOW	V_{OLC}	1610	mV

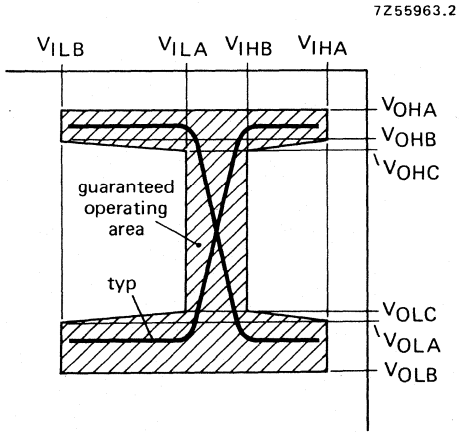


Fig. 7 Transfer characteristics.

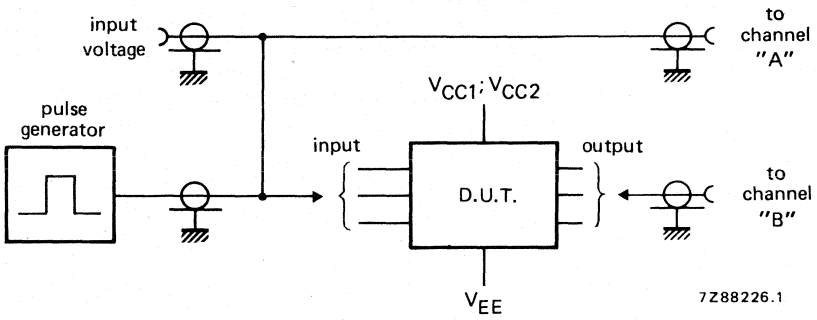


Fig. 8 Switching times test circuit. $V_{CC1} = V_{CC2} = +2{,}0$ V; $V_{EE} = -2{,}5$ V.

In order to test ECL100 000 circuits with a standard oscilloscope (load to ground), it is easier to use the test circuit with $V_{CC} = +2$ V, $V_{EE} = -2{,}5$ V and $R_L = 50\ \Omega$ to ground. All voltages given in the type specifications have then to be shifted by +2 V.

A.C. CHARACTERISTICS

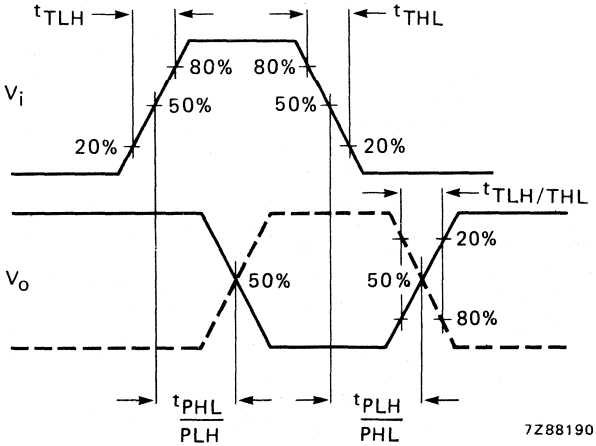


Fig. 9 Propagation delay waveform.

Notes

1. Input resistance is positive at any frequency.
2. In order to enable the output some circuits require application at HIGH level on other inputs. Refer to truth table in individual type specification.
3. Input and output cables to the oscilloscope are 50 Ω coaxial cables with equal length.
4. Input impedance of the oscilloscope has to be 50 Ω.
5. The unmatched wire stub between coaxial cable and pins under test must be less than 2 mm long for proper tests.

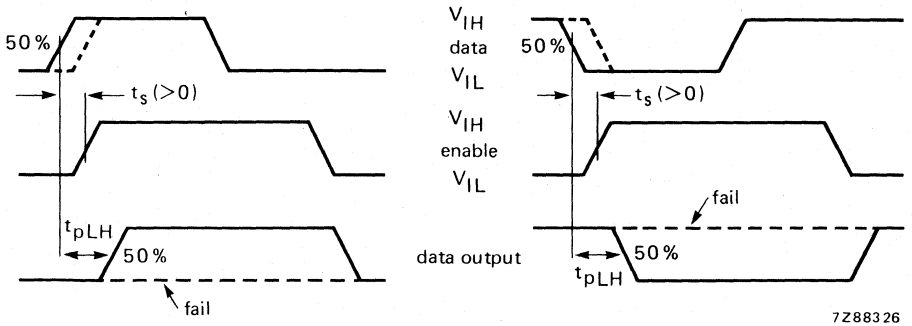


Fig. 10 Waveforms for data set-up time (t_s).

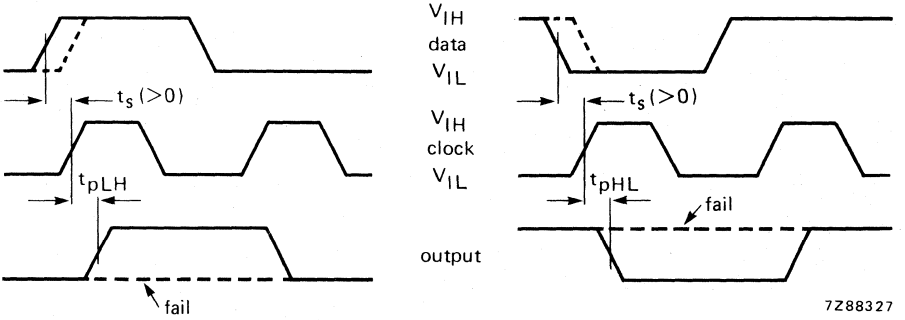


Fig. 11 Set-up time waveforms for rising and falling data signal.

Set up time (t_s) is the minimum time before the transition of the clock (or enable) that information must be present at the data input.

The limit value of set up time is positive if the transition of data signal is before the transition of clock (or enable) signal.

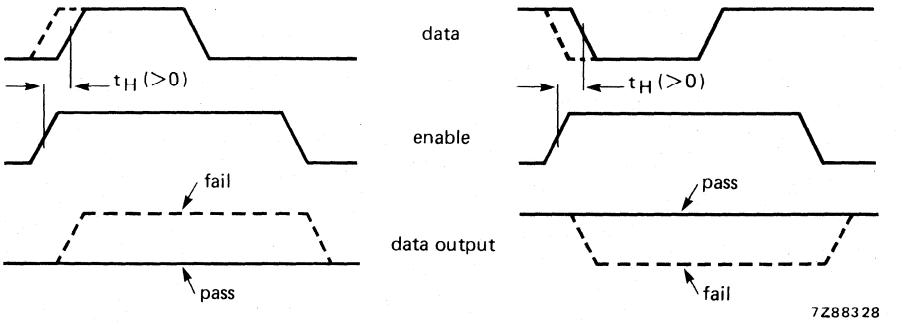


Fig. 12 Waveforms for data hold time (t_h).

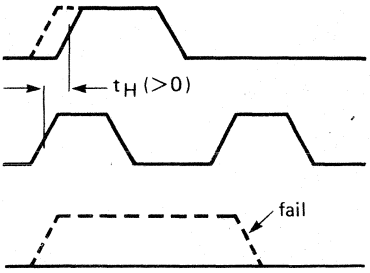


Fig. 13 Hold time for rising data signal.

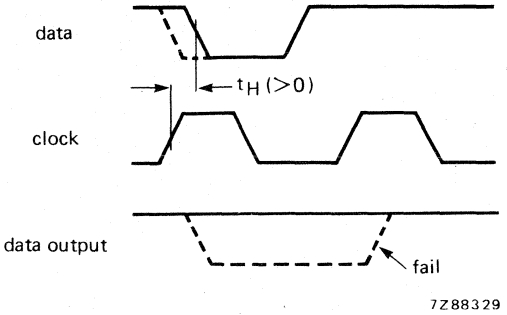


Fig. 14 Hold time for falling data signal.

Hold time (t_h) is the minimum time after the transition of the clock (or enable) that information must remain unchanged at the data input.

The limit value of hold time is positive if the transition of data signal is after the transition of clock (or enable) signal.

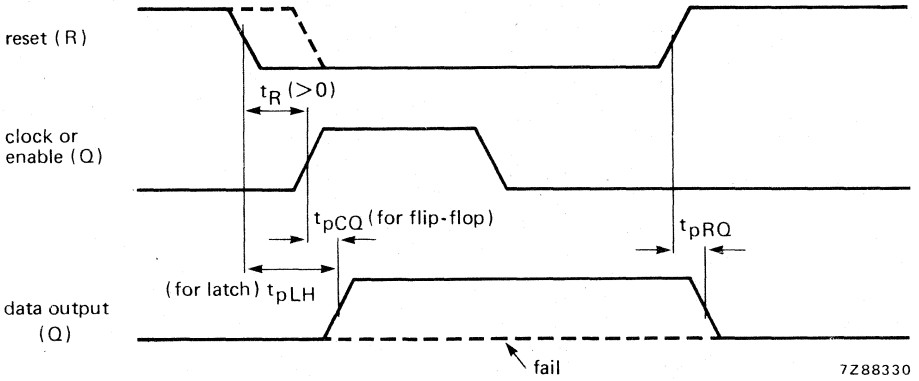


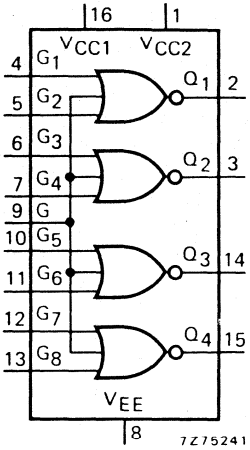
Fig. 15 Waveforms for release time (t_R) Reset; Data inputs are at HIGH level.

Release time (t_R) is the minimum time before the transition of the clock (or enable) that Reset must be suppressed.

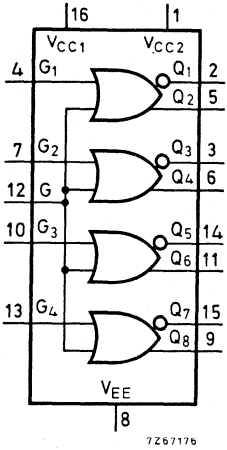
The limit value of release time is positive if the transition of reset is before the transition of clock (or enable).

LOGIC DIAGRAMS

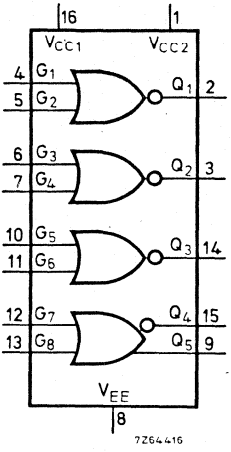
ECL10 000 FAMILY LOGIC DIAGRAMS



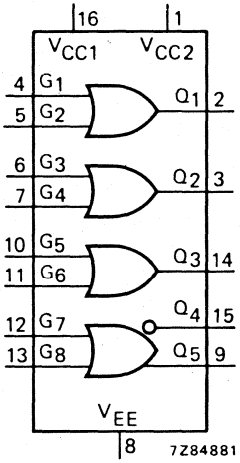
GXB10100



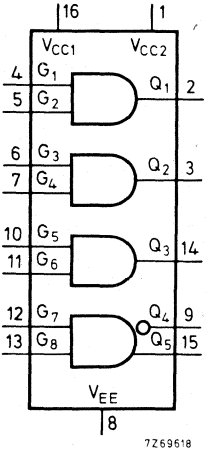
GXB10101



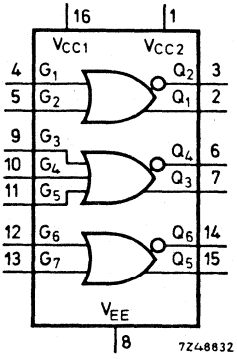
GXB10102



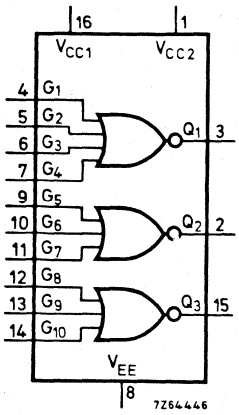
GXB10103



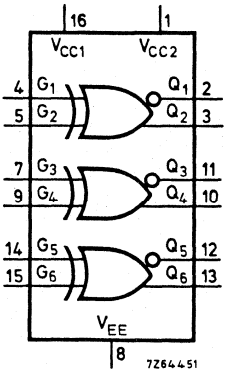
GXB10104



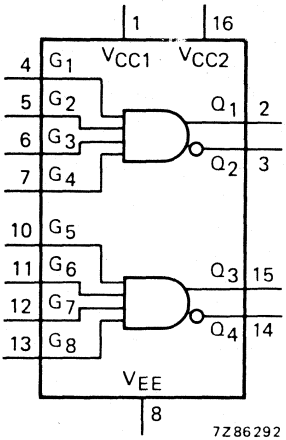
GXB10105



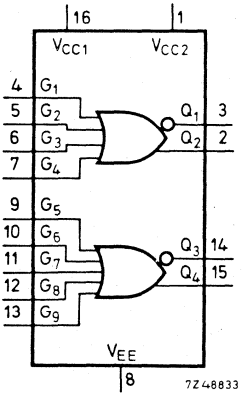
GXB10106



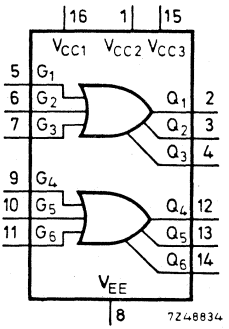
GXB10107



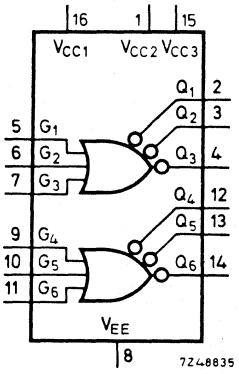
GXB10108



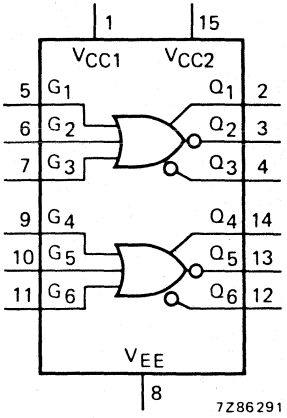
GXB10109



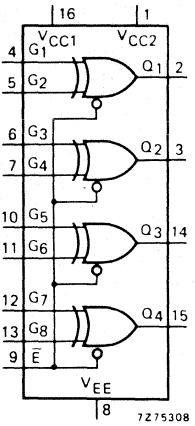
GXB10110



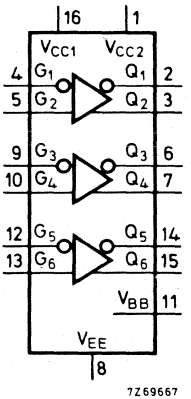
GXB10111



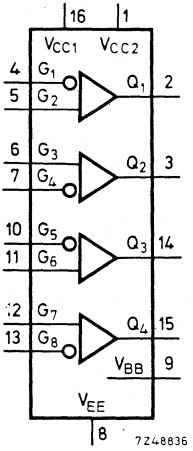
GXB10112



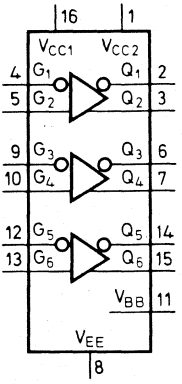
GXB10113



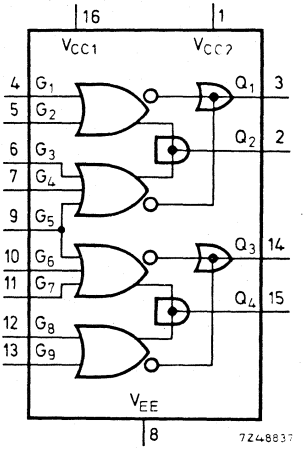
GXB10114



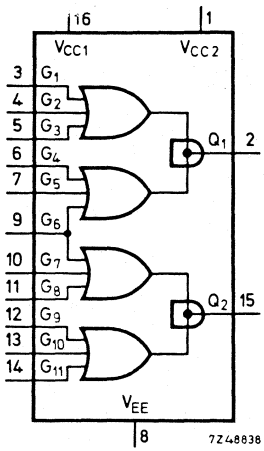
GXB10115



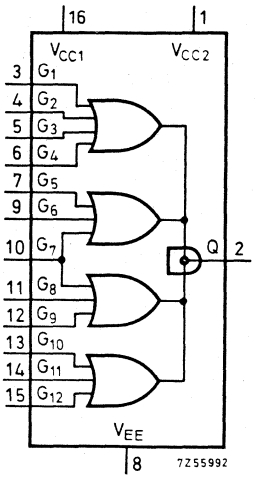
GXB10116



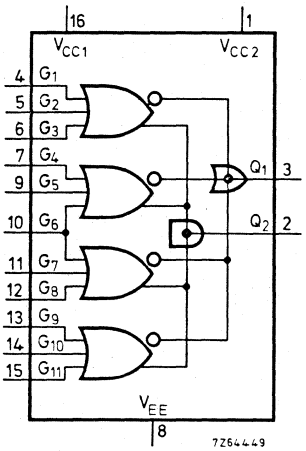
GXB10117



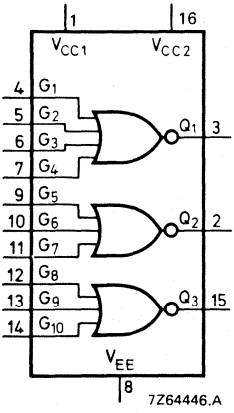
GXB10118



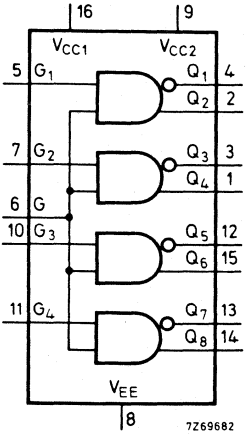
GXB10119



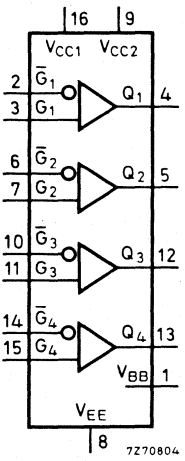
GXB10121



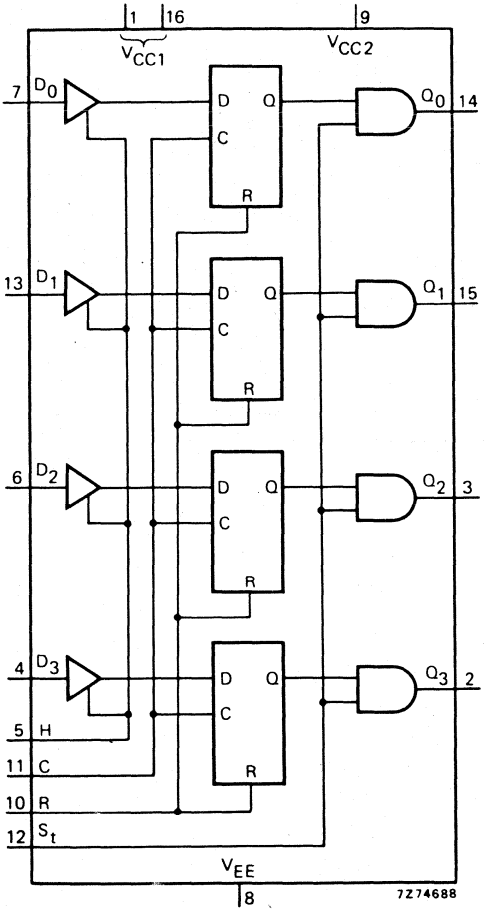
GXB10123



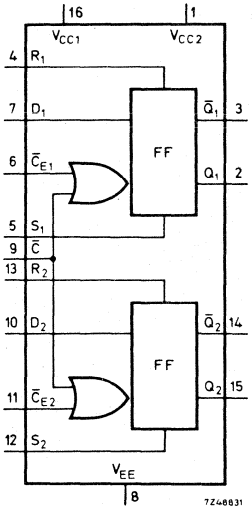
GXB10124



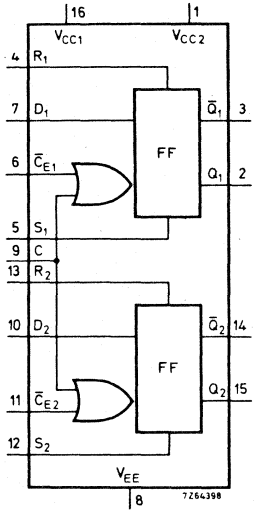
GXB10125



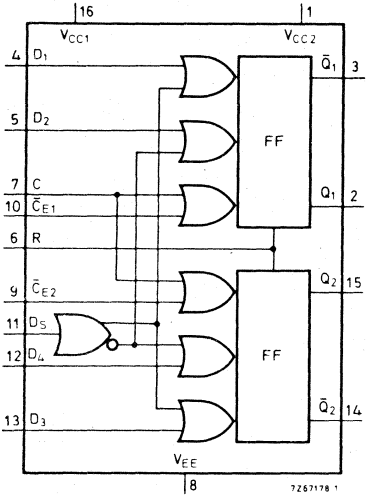
GXB10129



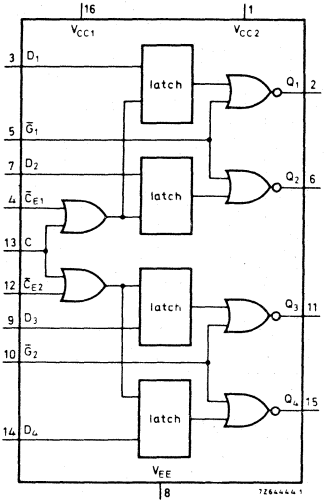
GXB10130



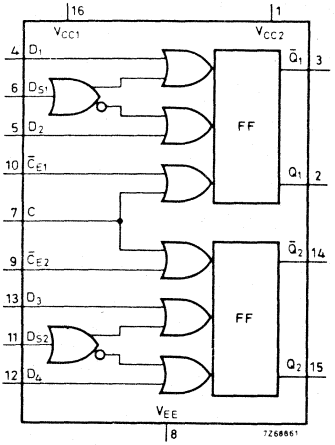
GXB10131



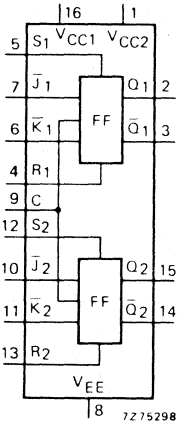
GXB10132



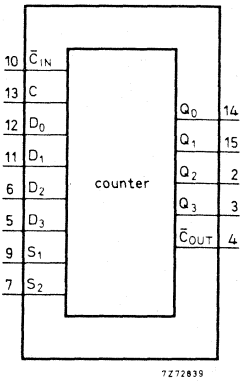
GXB10133



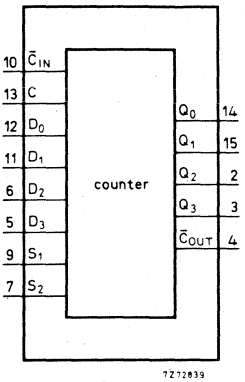
GXB10134



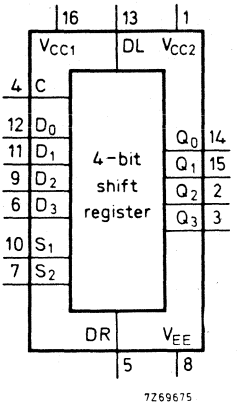
GXB10135



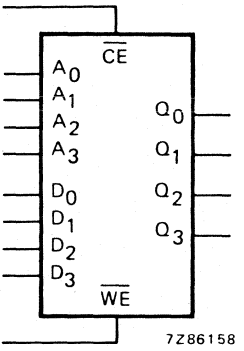
GXB10136



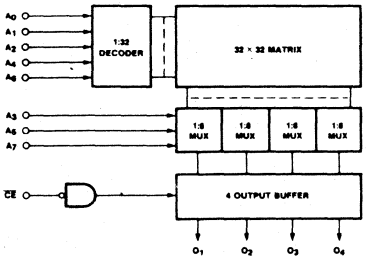
GXB10137



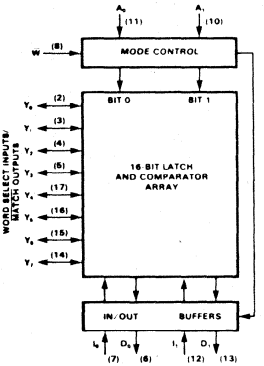
GXB10141



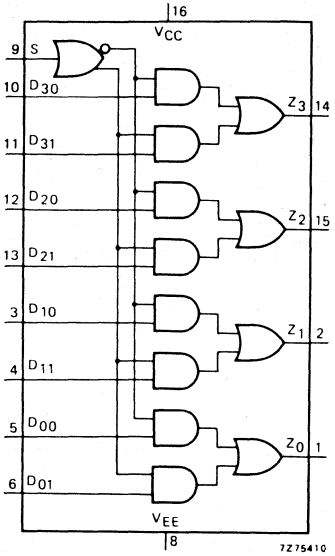
GXB10145



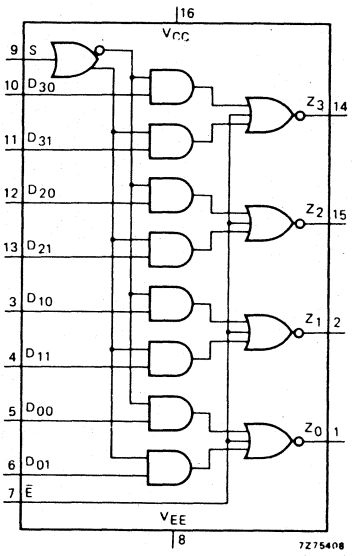
GXB10149



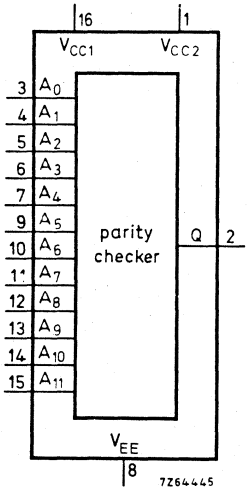
GXB10155



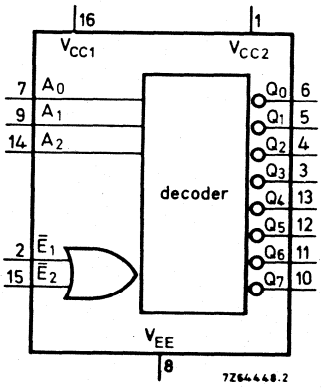
GXB10158



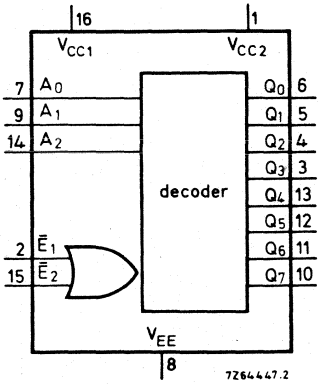
GXB10159



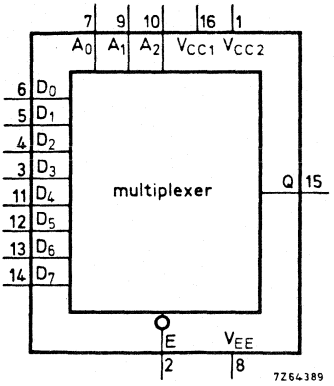
GXB10160



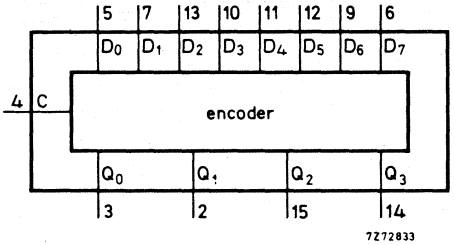
GXB10161



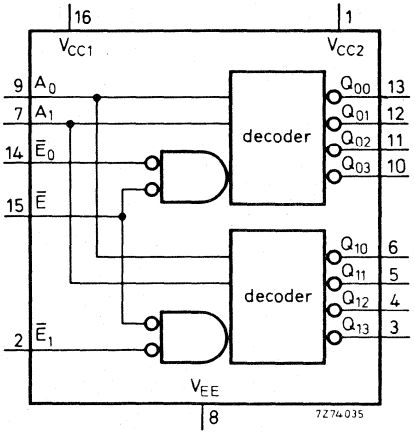
GXB10162



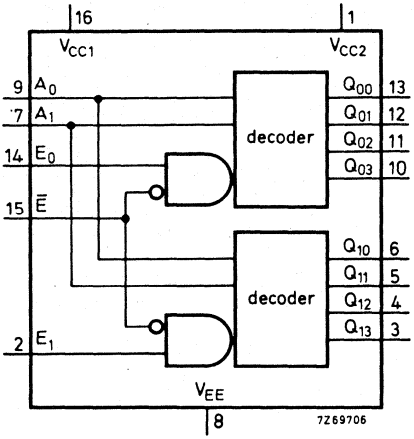
GXB10164



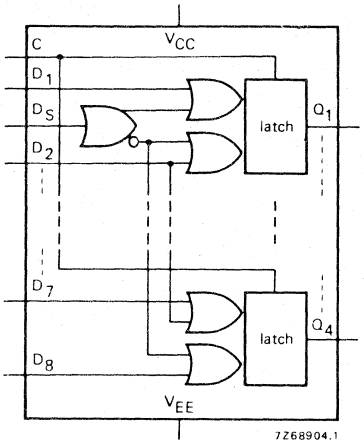
GXB10165



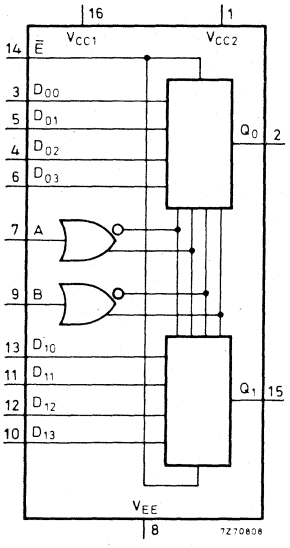
GXB10171



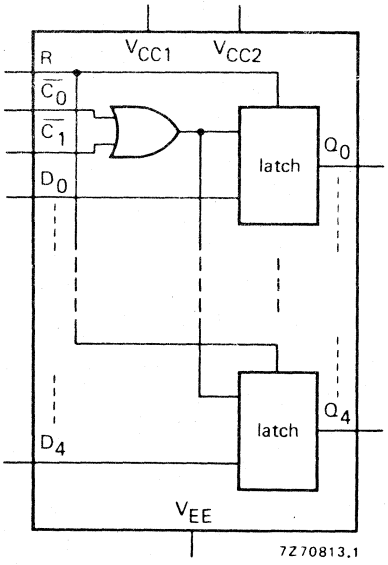
GXB10172



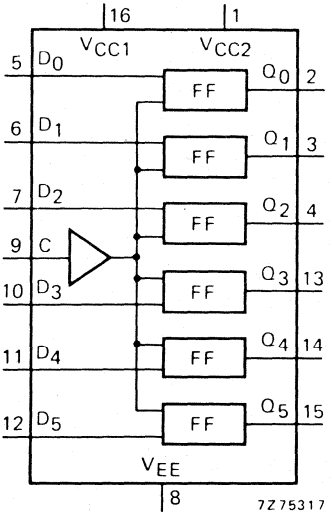
GXB10173



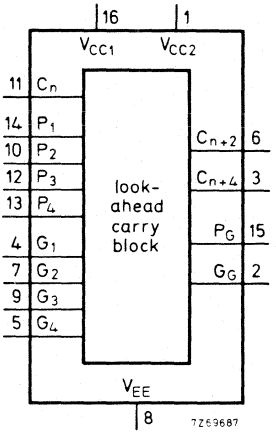
GXB10174



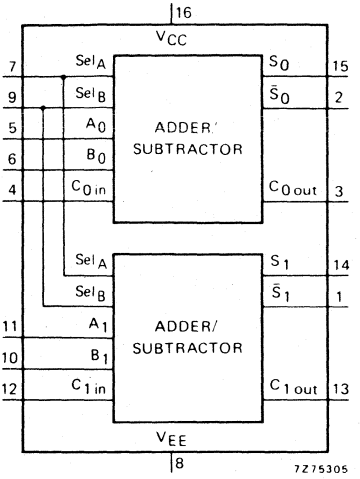
GXB10175



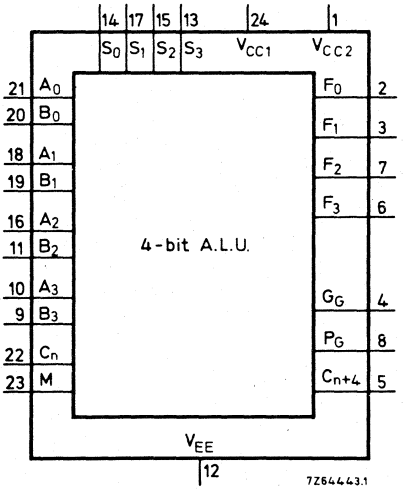
GXB10176



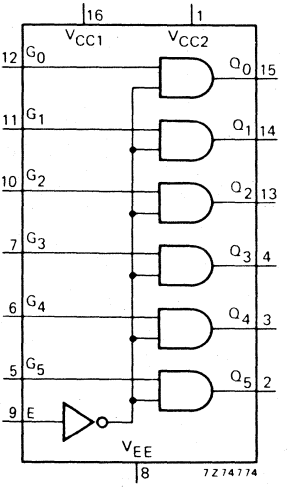
GXB10179



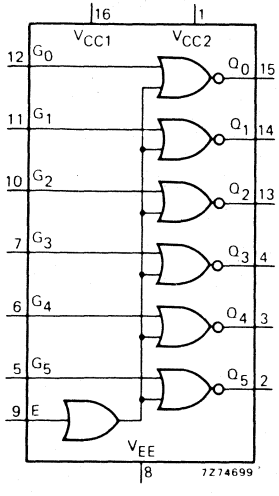
GXB10180



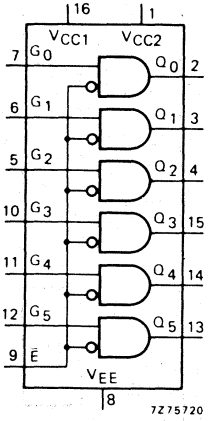
GXB10181



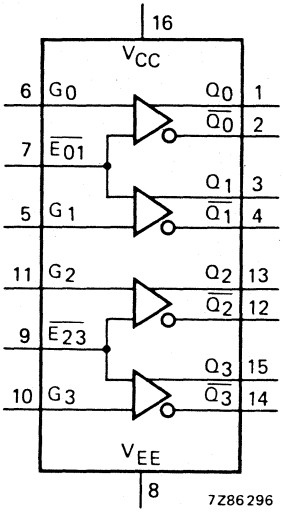
GXB10188



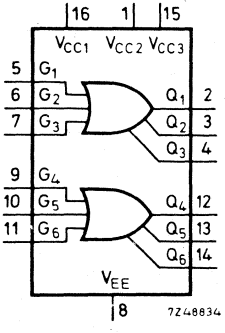
GXB10189



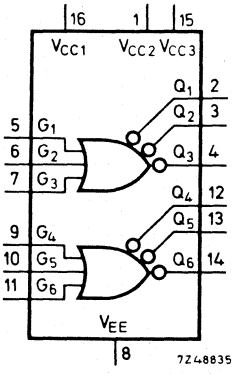
GXB10191



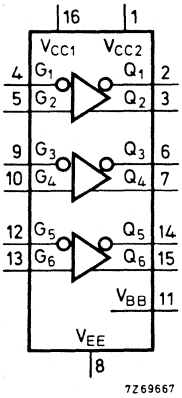
GXB10192



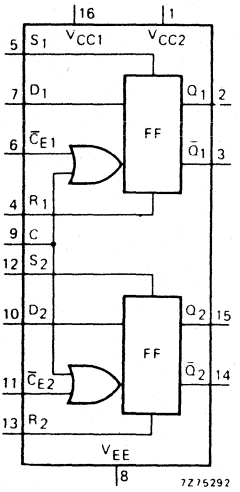
GXB10210



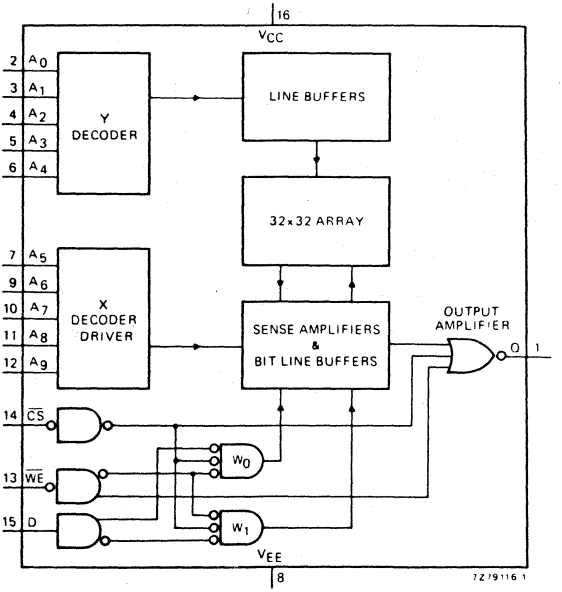
GXB10211



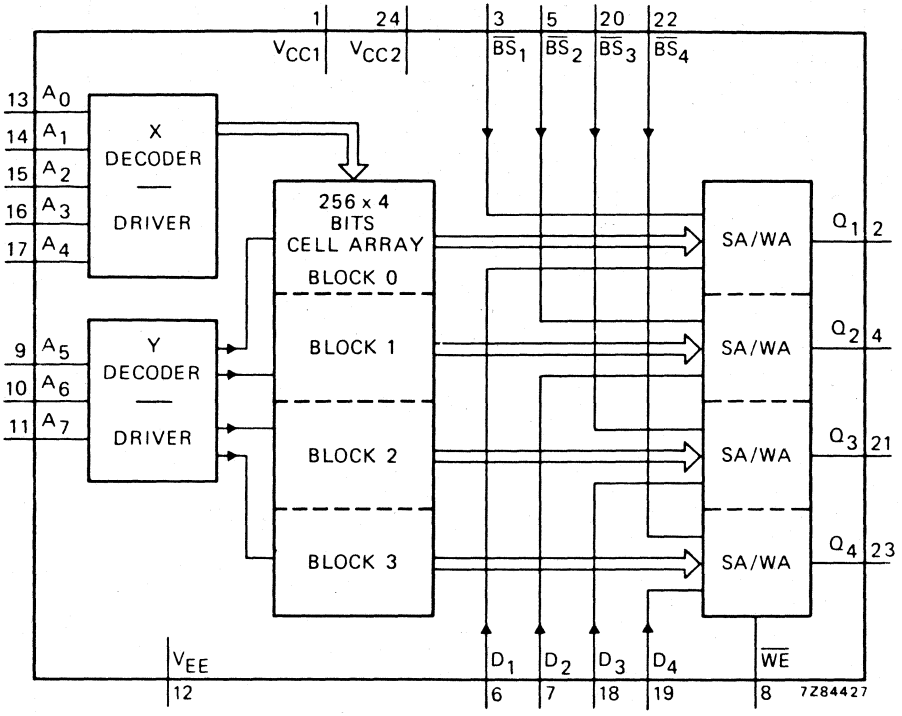
GXB10216



GXB10231



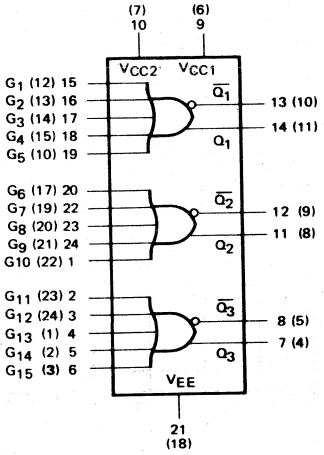
GXB10415; A


1
V_{CC1}
24
V_{CC2}
3
$\overline{BS}_1$
5
$\overline{BS}_2$
20
$\overline{BS}_3$
22
$\overline{BS}_4$
13 A_0
14 A_1
15 A_2
16 A_3
17 A_4
X DECODER — DRIVER
9 A_5
10 A_6
11 A_7
Y DECODER — DRIVER
256 x 4 BITS CELL ARRAY
BLOCK 0
BLOCK 1
BLOCK 2
BLOCK 3
SA/WA
SA/WA
SA/WA
SA/WA
Q_1 2
Q_2 4
Q_3 21
Q_4 23
V_{EE}
12
D_1 6
D_2 7
D_3 18
D_4 19
$\overline{WE}$ 8
7Z84427

GXB10422; A

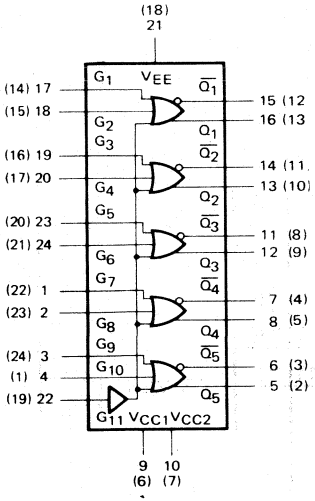
ECL 100 000 FAMILY LOGIC DIAGRAMS

100 101



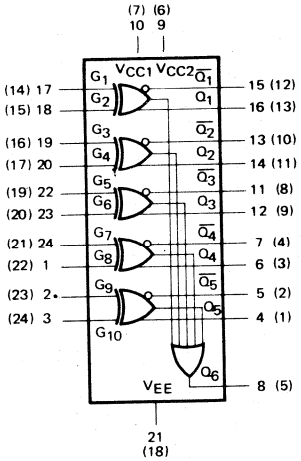
Triple 5 - input OR/NOR gate

100 102



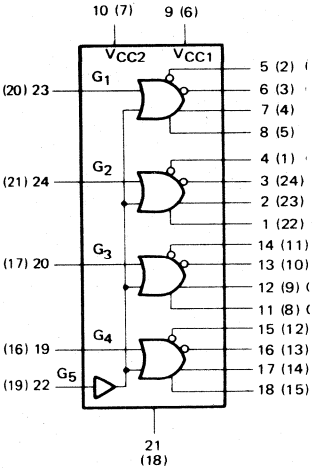
Quintuple 2 - Input OR/NOR gate w common enable

100 107



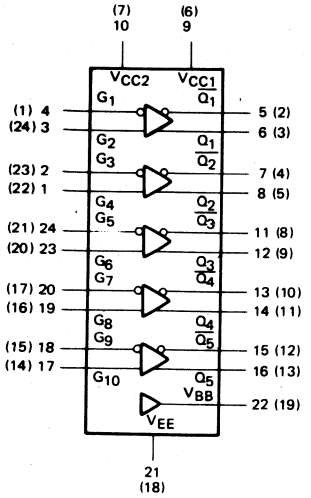
Quintuple exclusive OR/NOR gate with compare

100 112



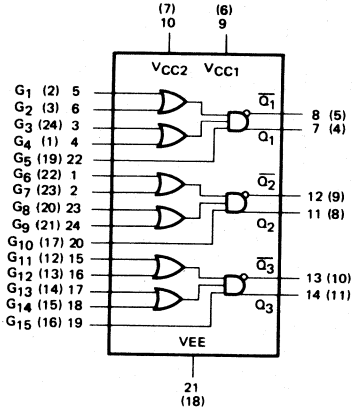
Quadruple fan-out OR/NOR gate

100 114



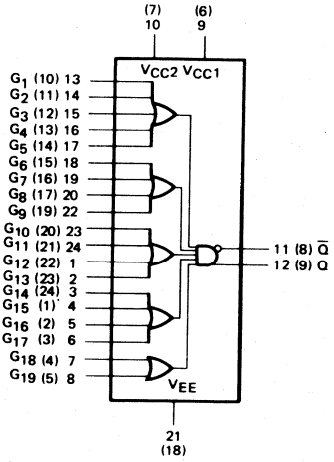
Quintuple differential line receiver

100 117



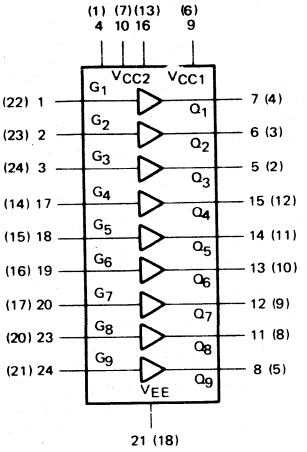
Triple 1-2-2 input OR/AND-OR/NAND gate

100 118



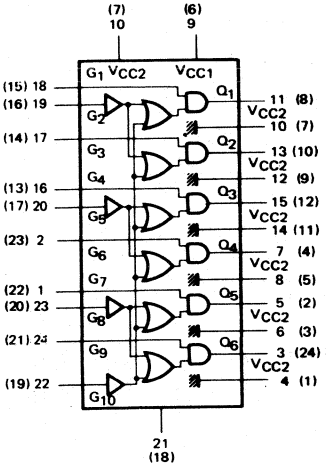
2-4-4-5 input OR/AND-OR/NAND gate

100 122



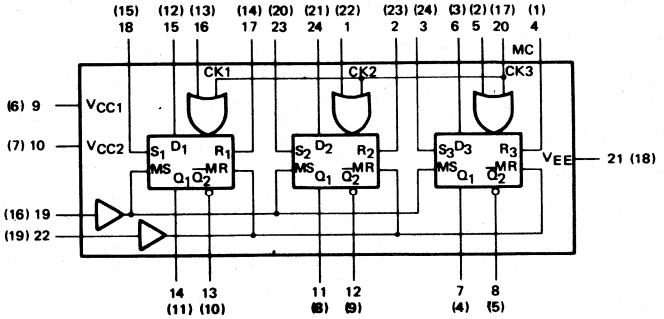
9 gate buffer

100 123

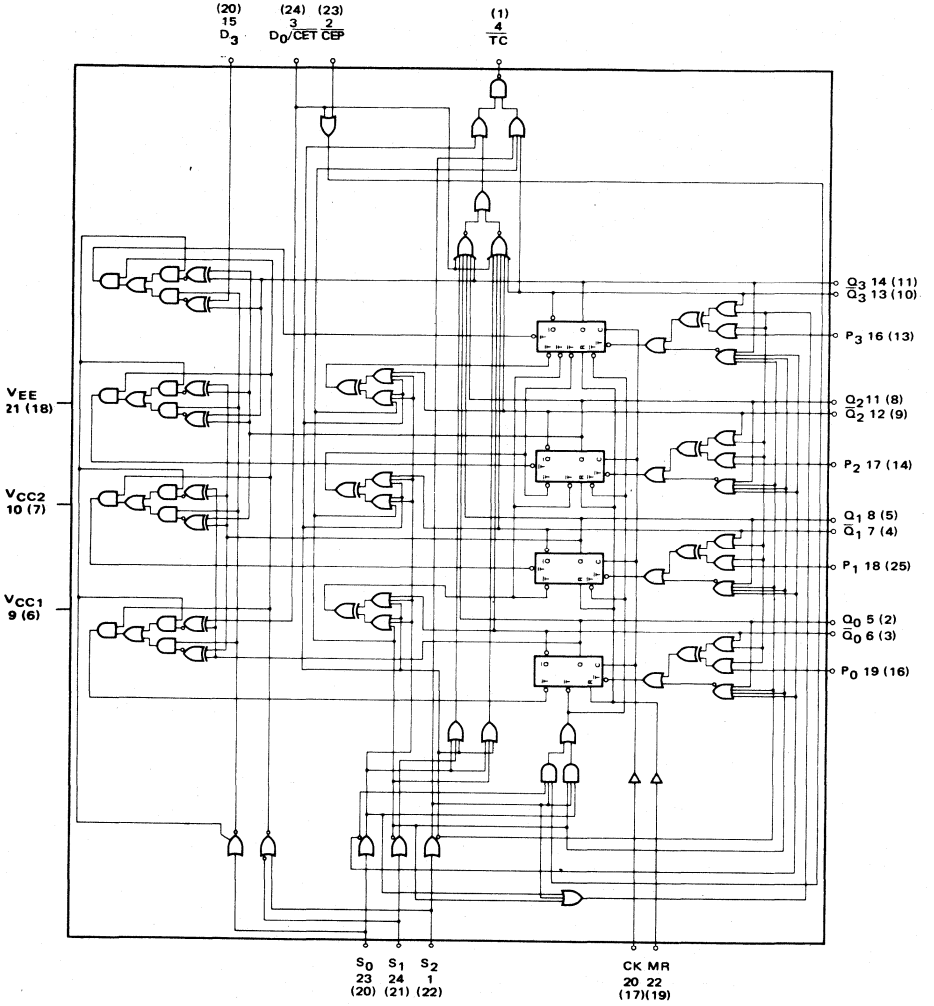


Hex bus driver

100 131

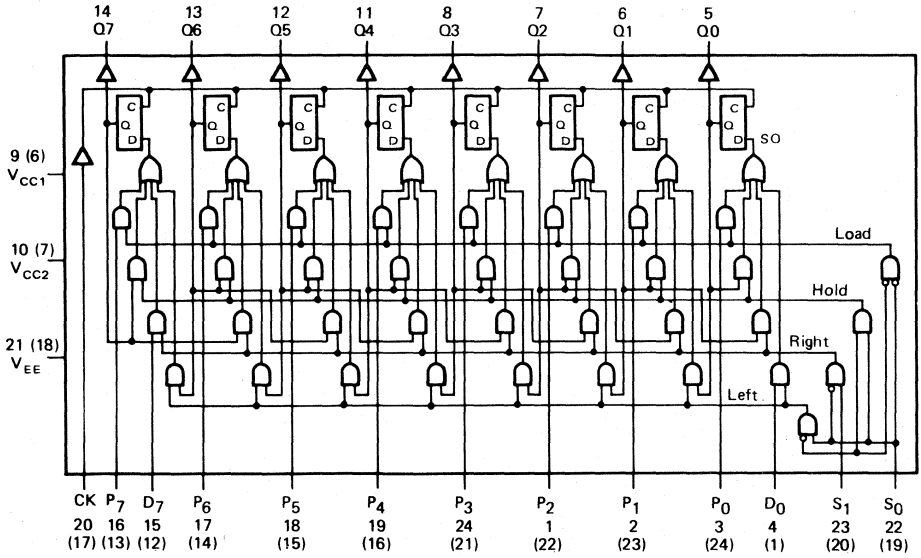


Triple D flip-flop



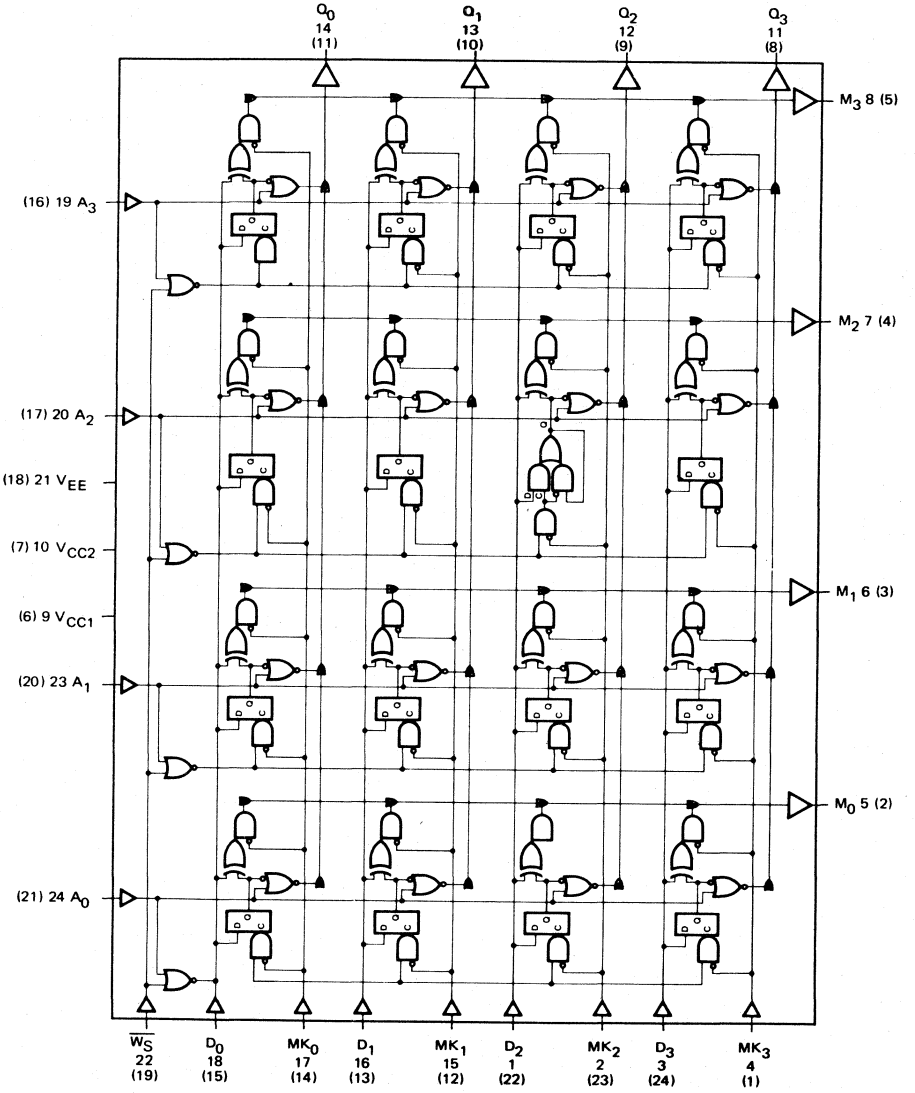
4-bit counter-shift register

100 141



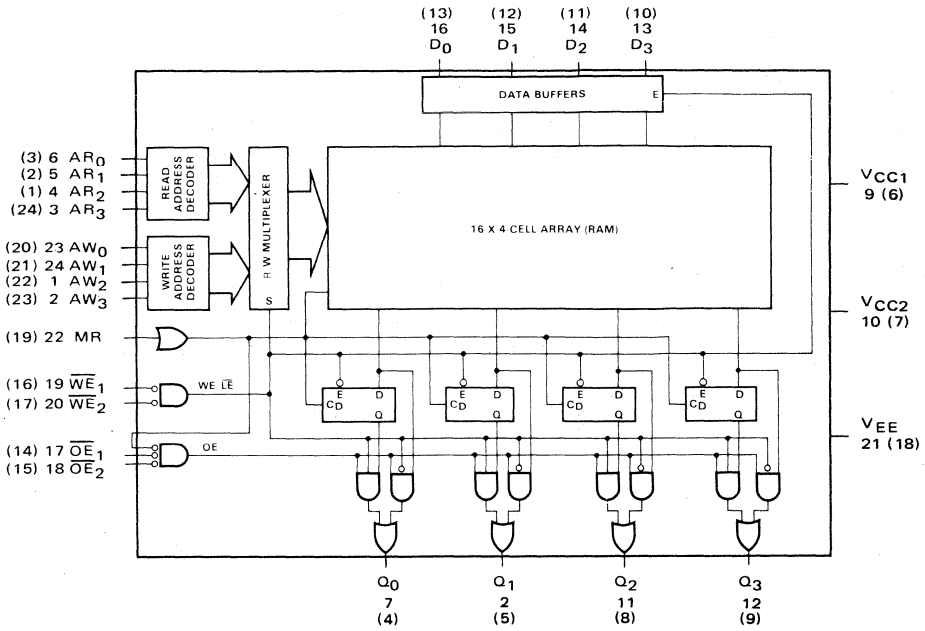
8-bit shift register

100 142



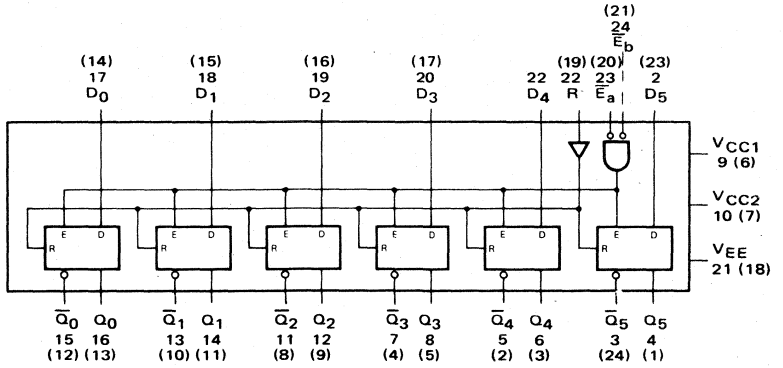
4 x 4 content adressable memory

100 145



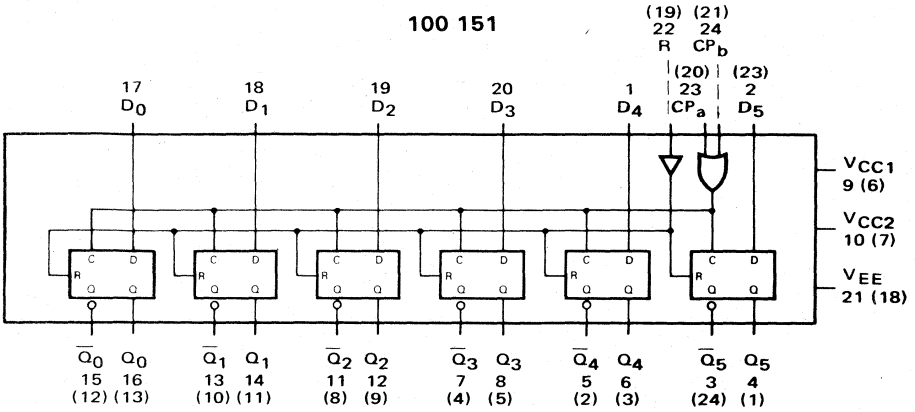
16 x 4 read while write register file

100 150



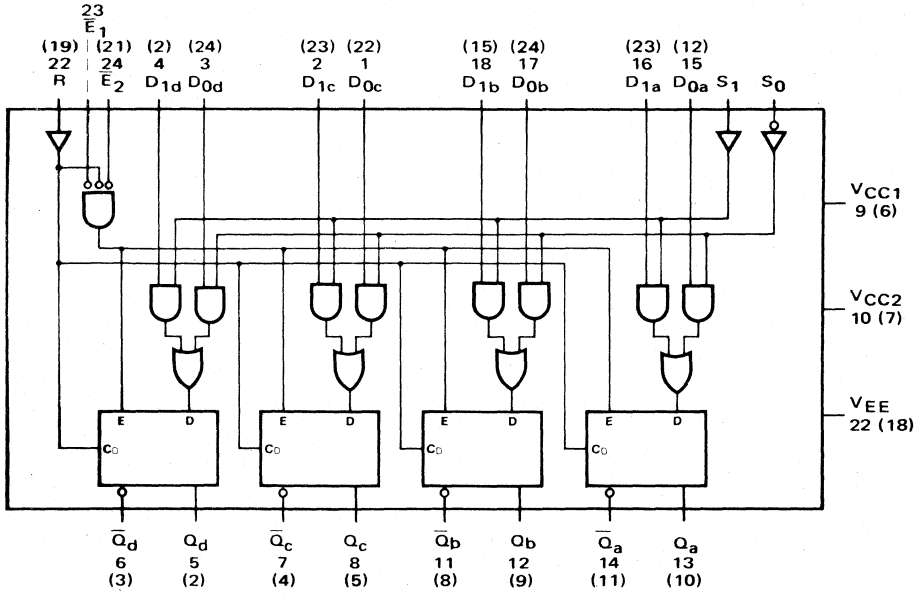
Hex D latch flip-flop

100 151

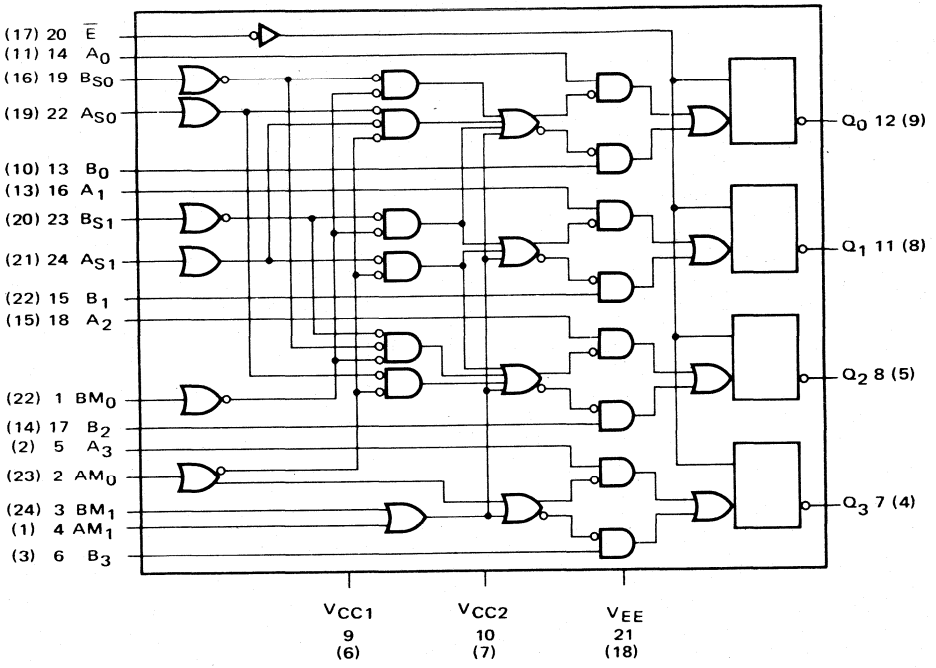


Hex D master slave flip-flop

100 155

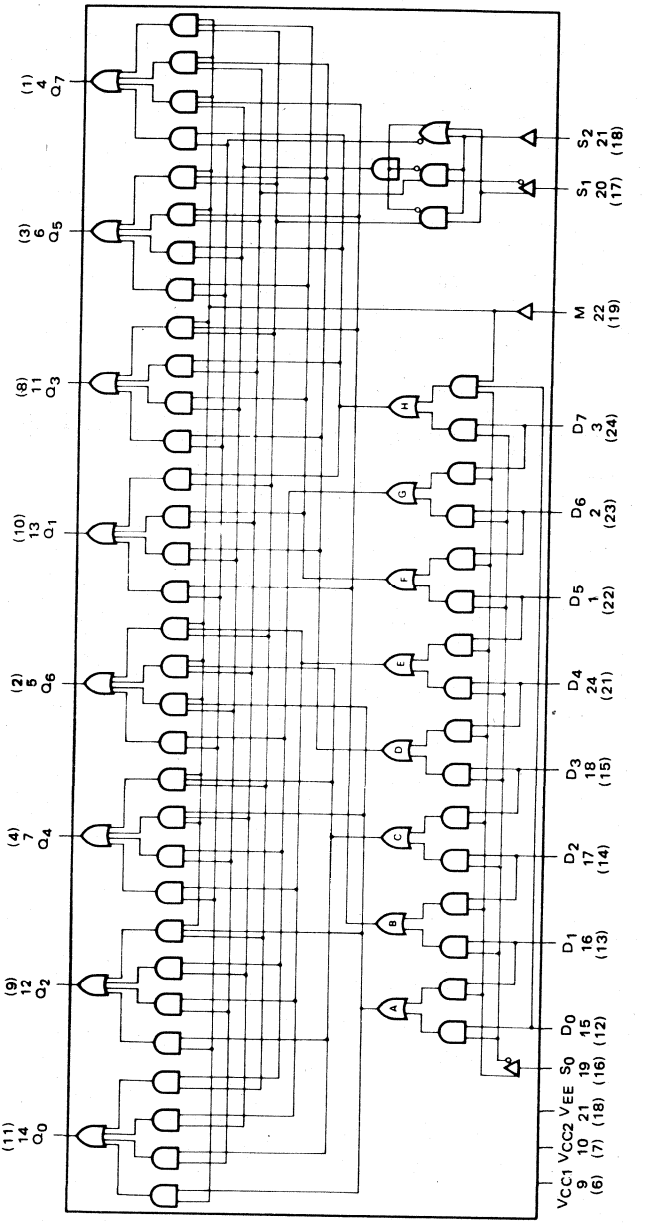


Quadruple 2 way multiplexer-latch

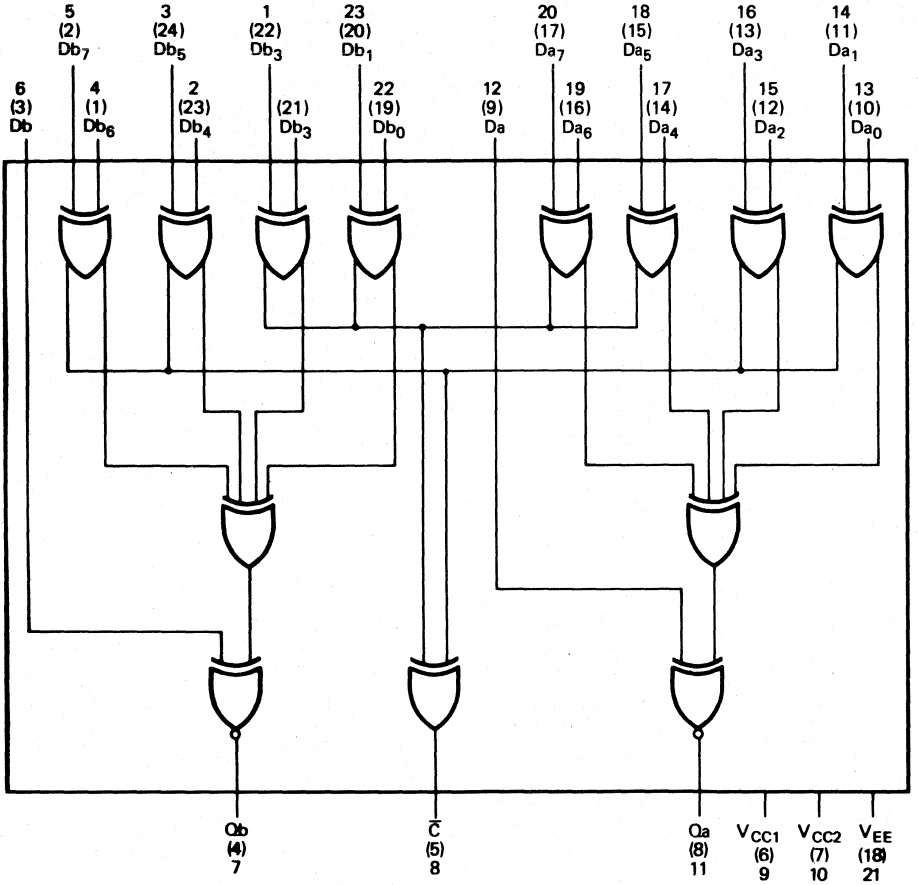


Mask-merge selector

100 158

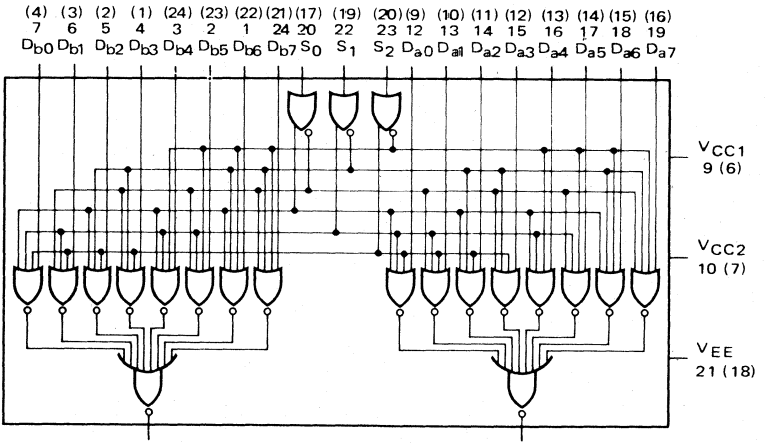


8-bit shift matrix



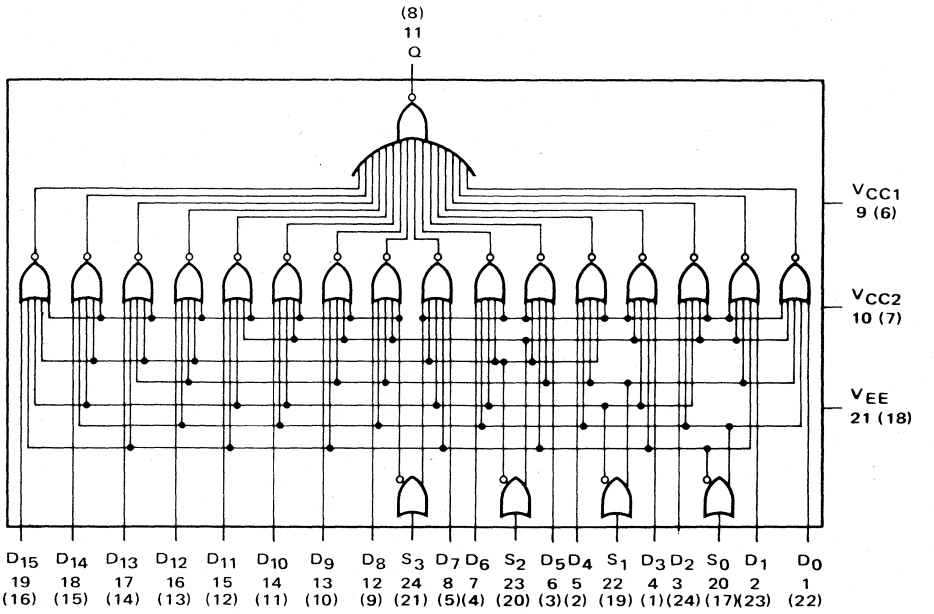
Dual 9-bit parity generator/8-bit comparator

100 163



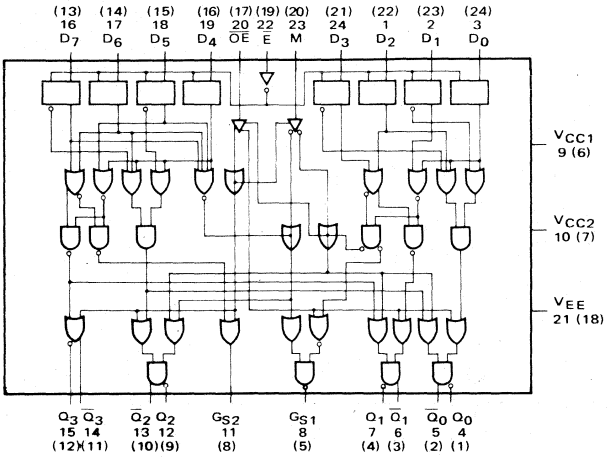
Dual 8-bit multiplexer

100 164



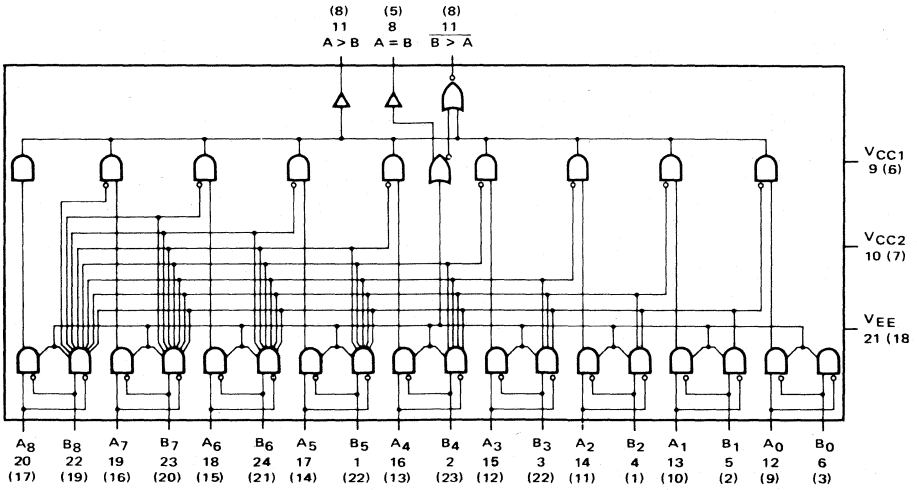
16 input multiplexer

100 165



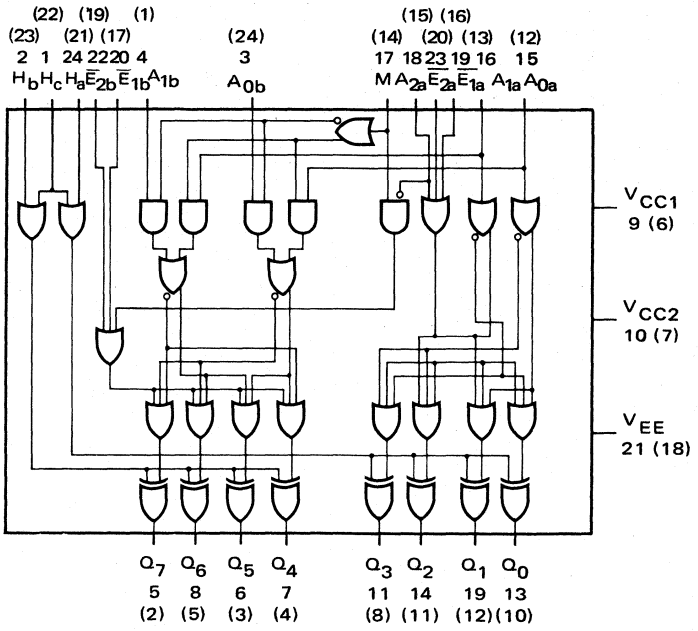
Universal priority encoder

100 166



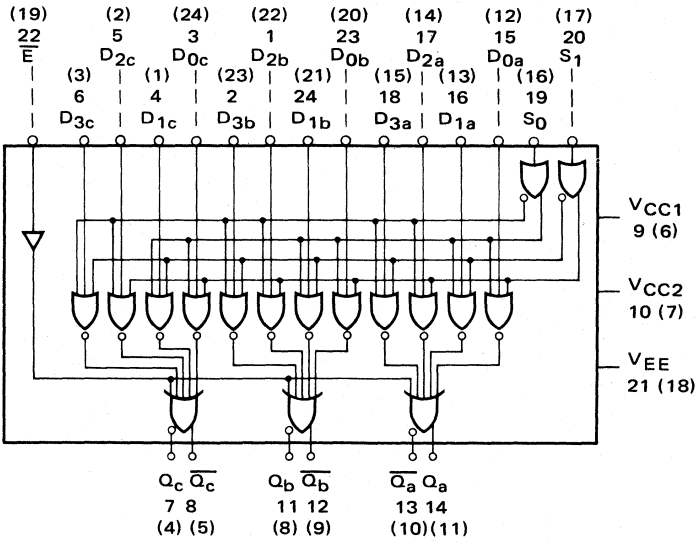
9-bit comparator

100 170

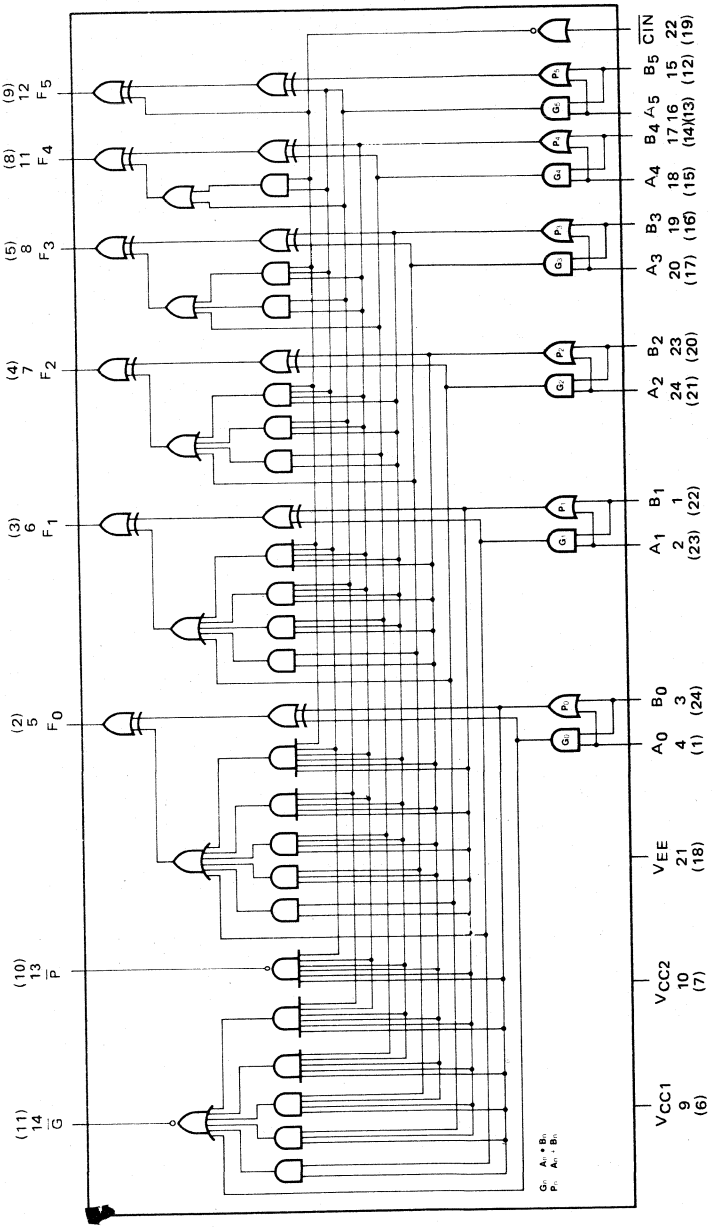


Universal demux/decoder

100 171

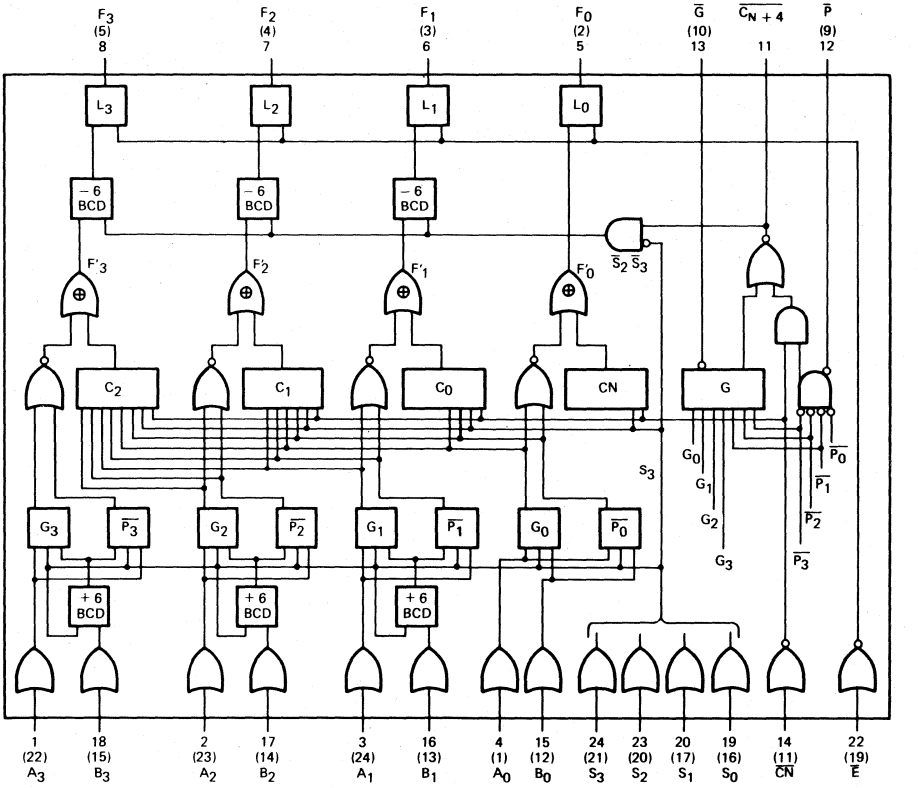


Three-bit 4 way multiplexer

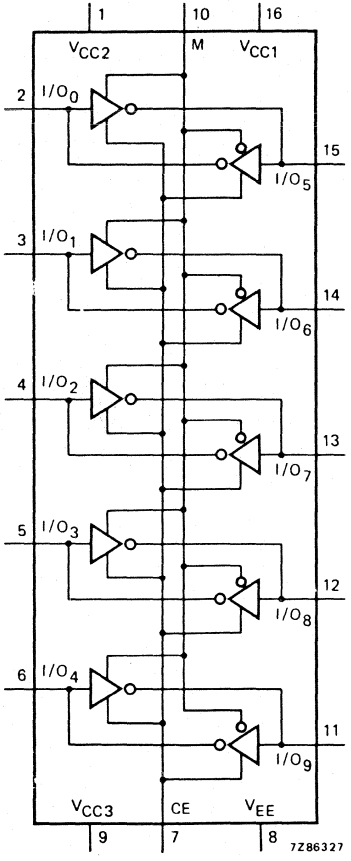


Fast 6-bit adder

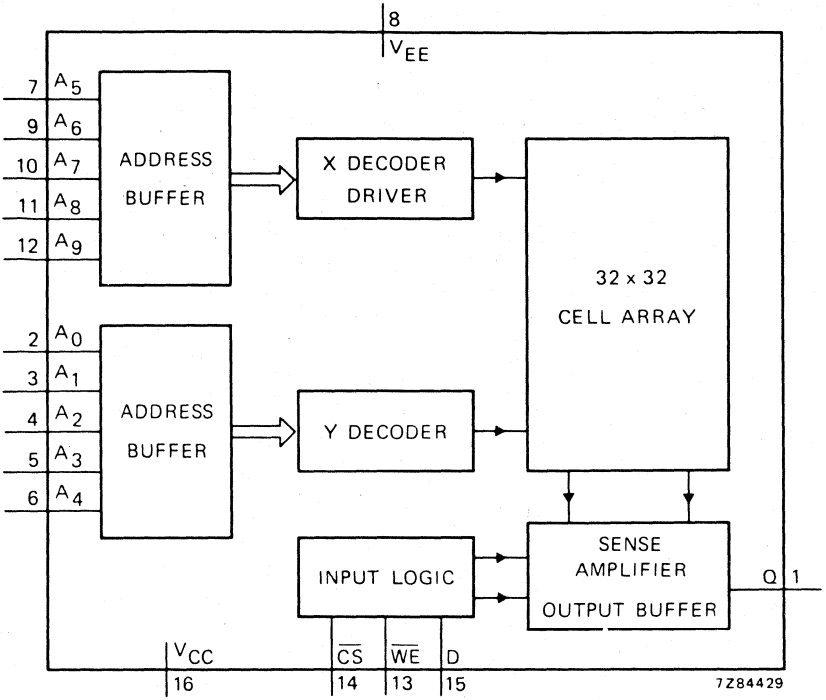
100 181



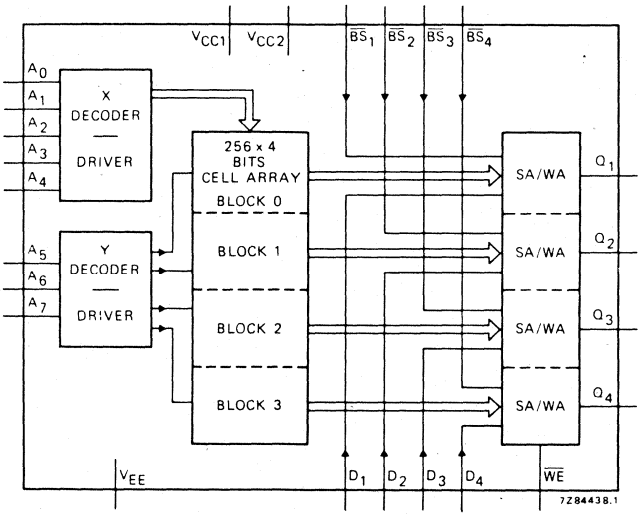
4-bit binary/BCD ALU


1
10
16
V_{CC2}
M
V_{CC1}
2
I/O_0
15
I/O_5
3
I/O_1
14
I/O_6
4
I/O_2
13
I/O_7
5
I/O_3
12
I/O_8
6
I/O_4
11
I/O_9
V_{CC3}
CE
V_{EE}
9
7
8
7Z86327

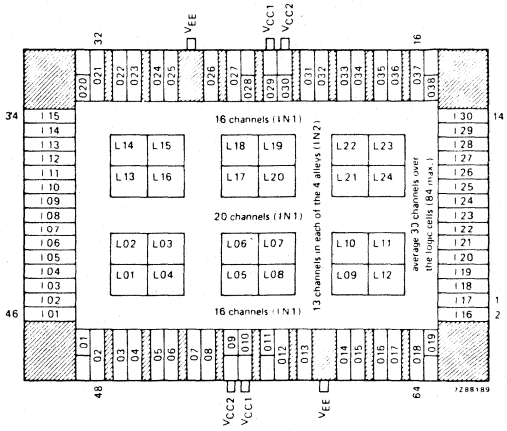
HXA100255



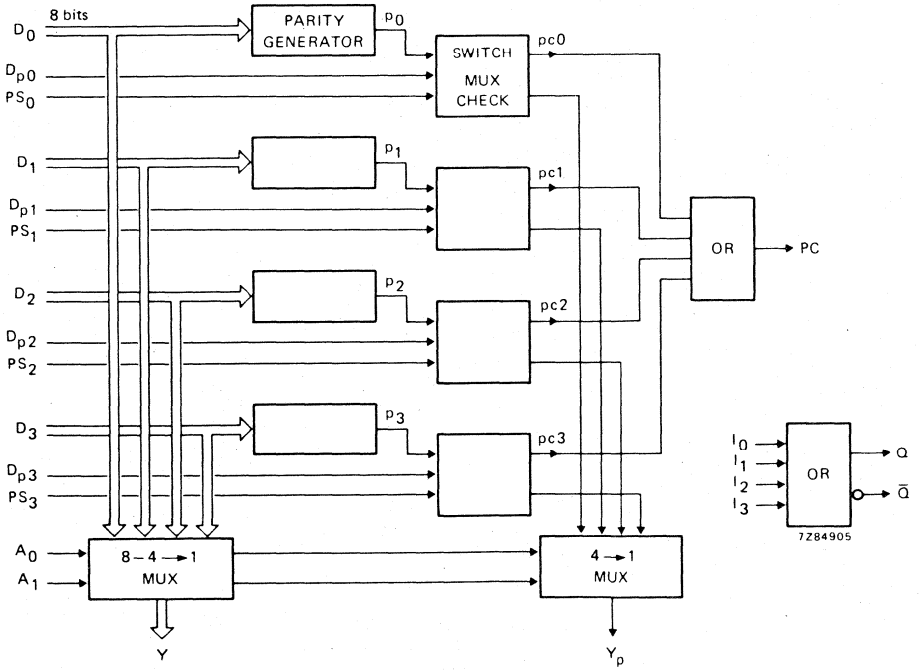
HXA100415; A



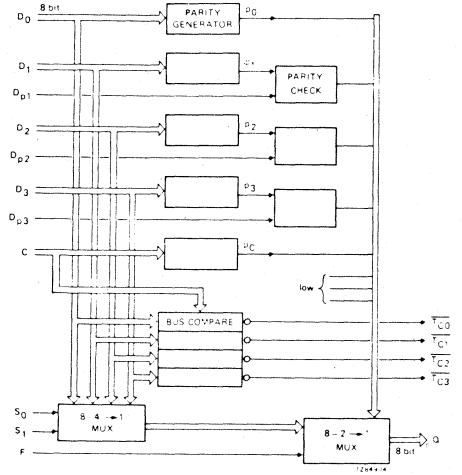
HXA100422; A



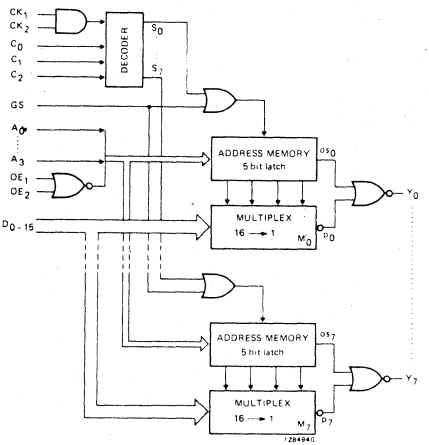
HXA220XXX



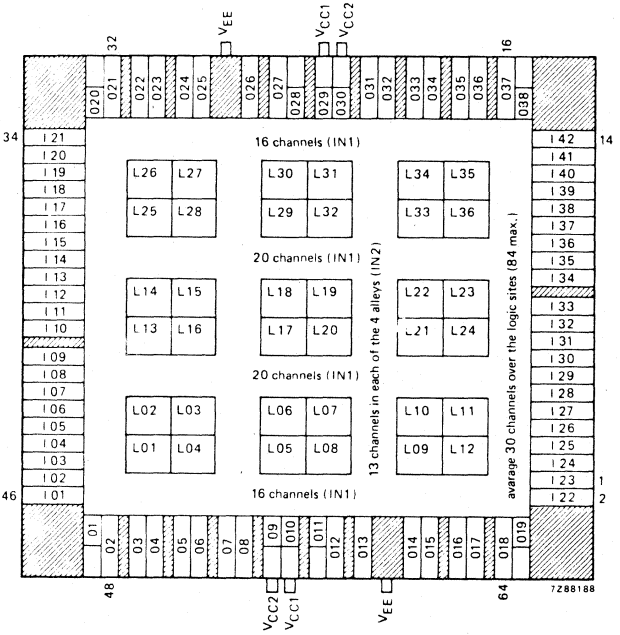
HXA220384



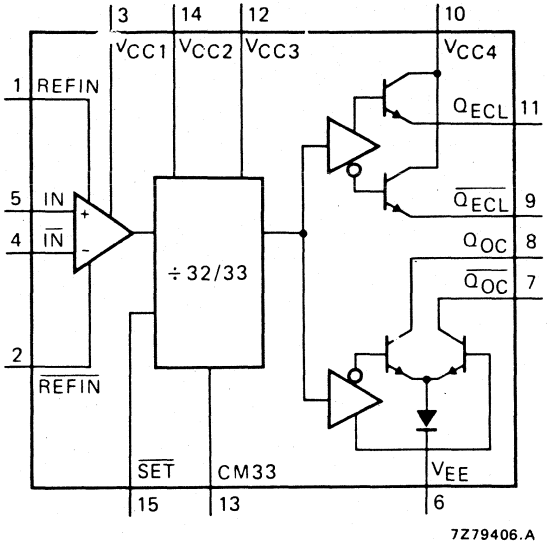
HXA220402



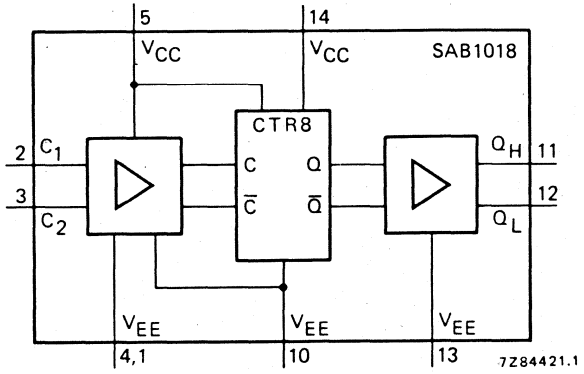
HXA230101



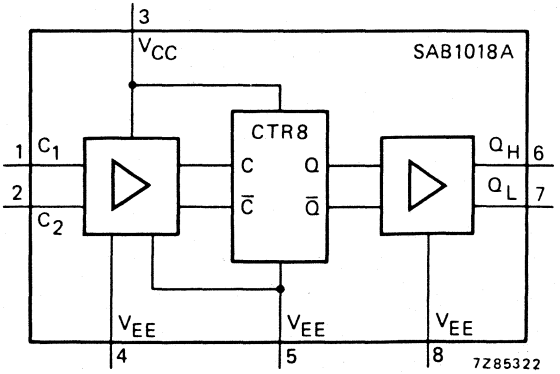
HXA230XXX



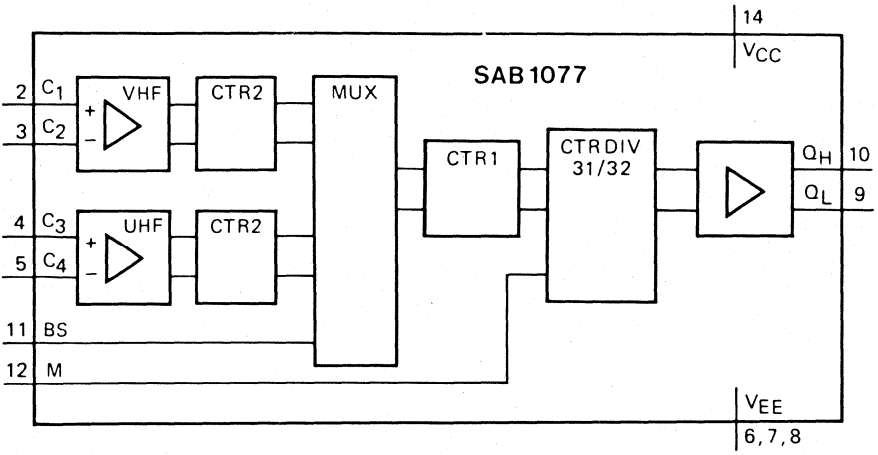
SAA1059



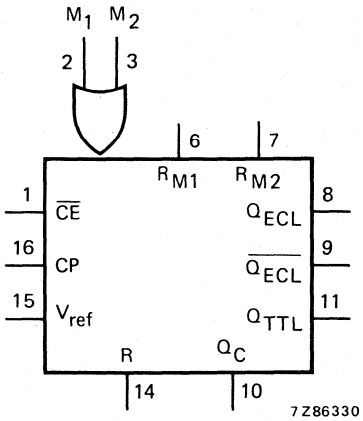
SAB1018



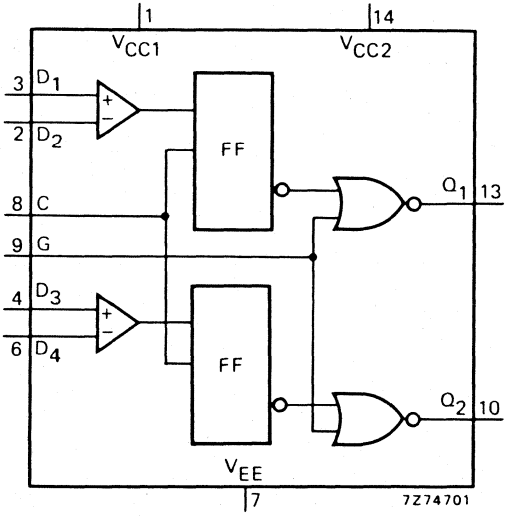
SAB1018A



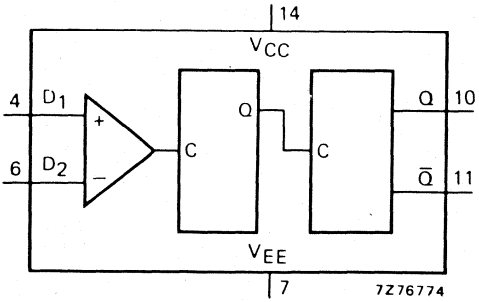
SAB1077



SAB1078



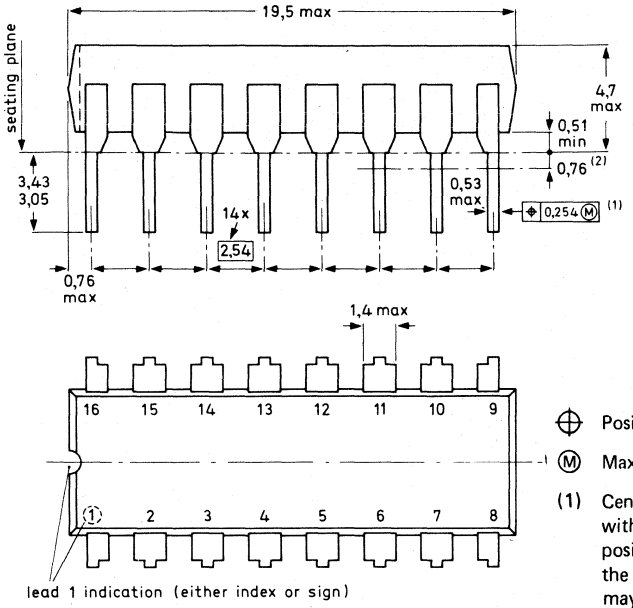
SAB1801D



SAF1034
SAF1534

PACKAGE OUTLINES

16-LEAD DUAL IN-LINE; PLASTIC (SOT-38Z)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

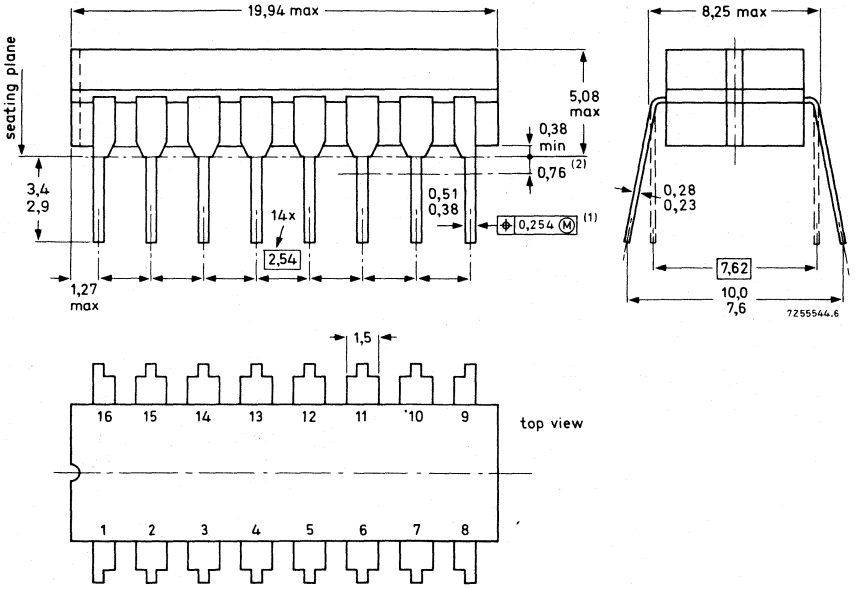
2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

16-LEAD DUAL IN-LINE; CERAMIC (SOT-74)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

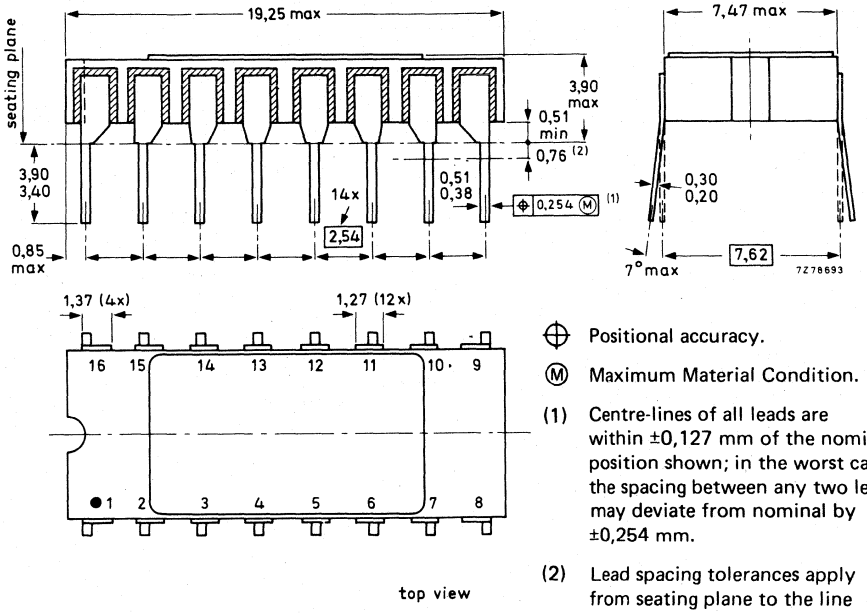
(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

Remarks

1. Leads are given positive misalignment so that they grip after insertion.
2. Leads are Ni-Fe, pure tin plated.

16-LEAD DUAL IN-LINE; METAL-CERAMIC (SOT-84B)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

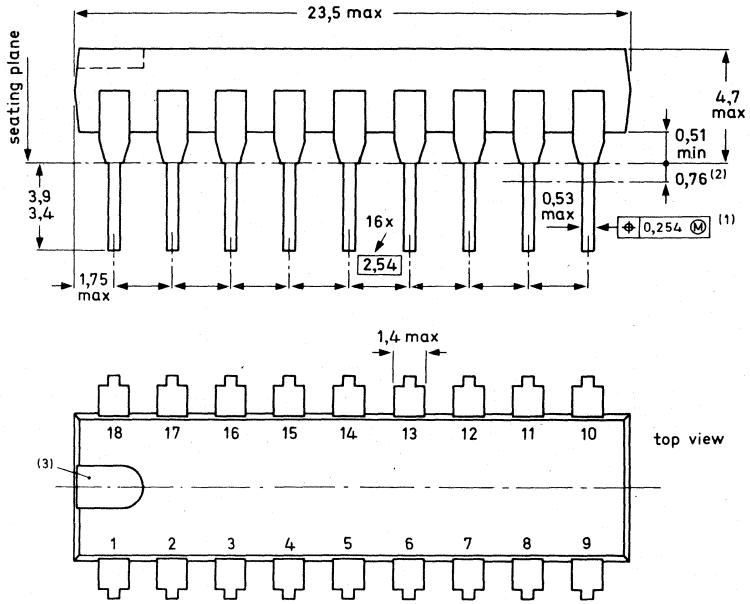
(2) Lead spacing tolerances apply from seating plane to the line indicated.

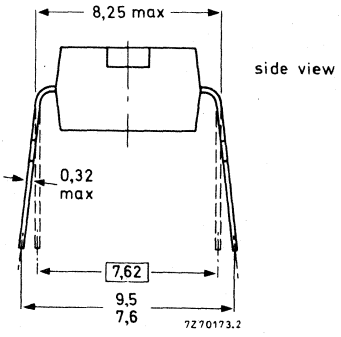
Dimensions in mm

Remarks

1. Leads are given positive misalignment so that they grip after insertion.
2. Leads are Ni-Fe, pure tin plated.

18-LEAD DUAL IN-LINE; PLASTIC (SOT-102A)





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

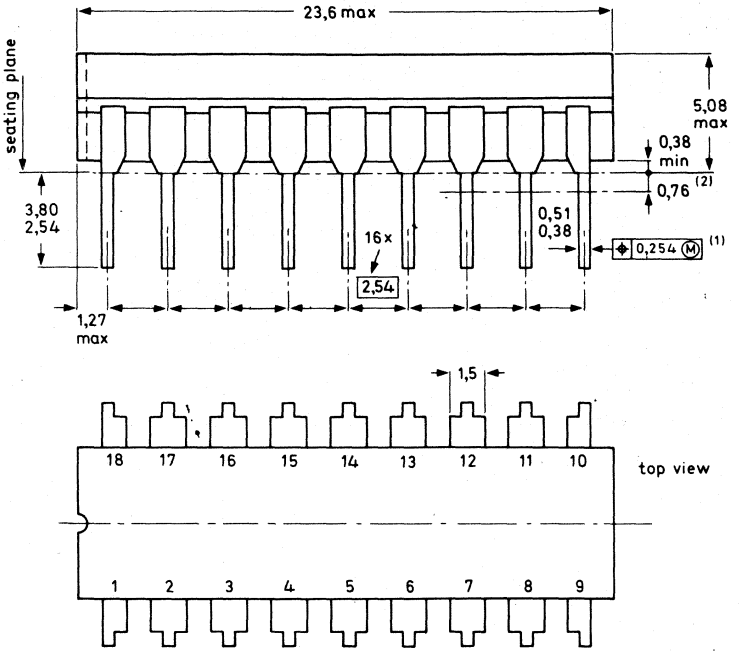
(3) Index may be horizontal as shown, or vertical.

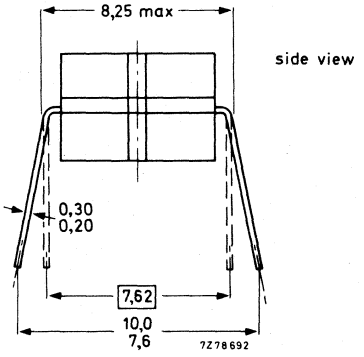
Dimensions in mm

SOLDERING

See SOT-38 (page 1).

18-LEAD DUAL IN-LINE; CERAMIC (SOT-133)





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

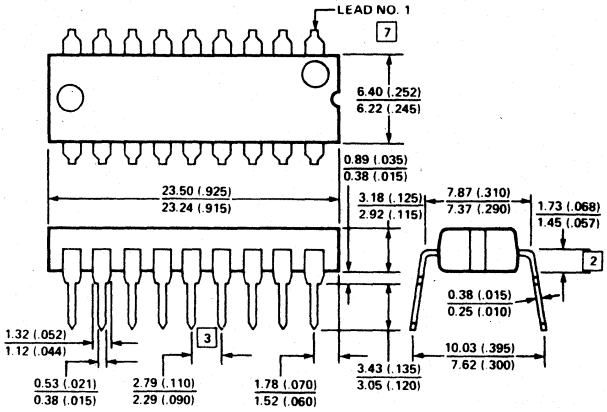
(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

Remarks

1. Leads are given positive misalignment so that they grip after insertion.
2. Leads are Ni-Fe, pure tin plated.

18-LEAD DUAL IN-LINE; PLASTIC (NK PACKAGE)



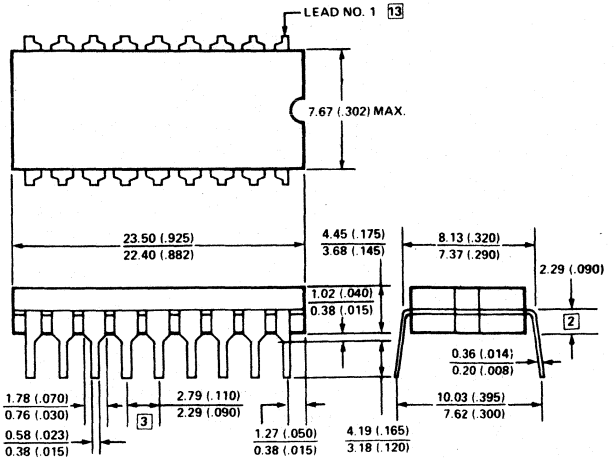
[2] Lead spacing shall be measured within this zone.
Shoulder and lead tip dimensions are to the centerline of leads.

[3] Tolerances non-cumulative.

[7] Round hole in top corner denotes lead number 1.

Dimensions in mm, except those in parentheses which are in inches.

18-LEAD DUAL IN-LINE; CERAMIC (FK PACKAGE)



2 Lead spacing shall be measured within this zone.
Shoulder and lead tip dimensions are to centerline of leads.

3 Tolerances non-cumulative.

13 Symbol, angle cut or lead tab denotes lead number 1.

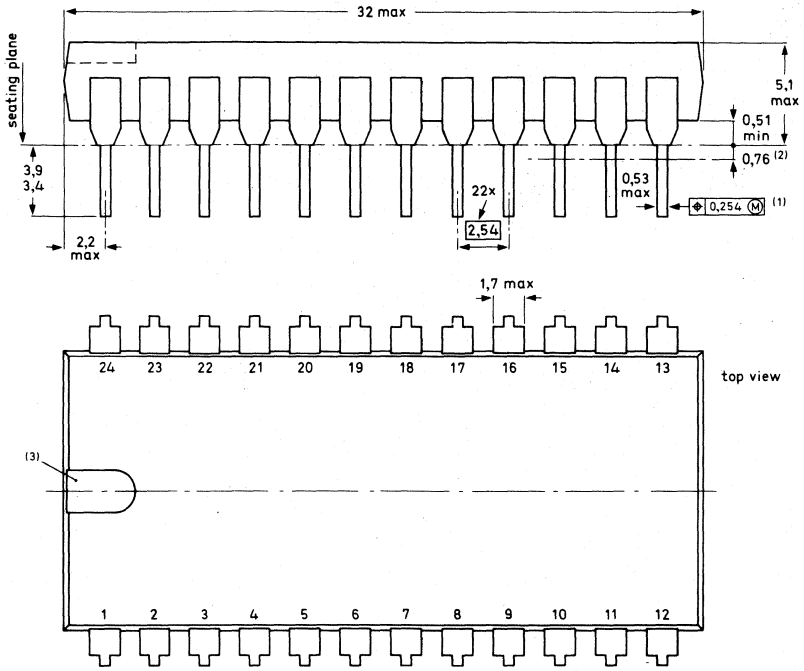
Lead material:
ASTM alloy F-30 (Alloy 42) or equivalent
tin plated; gold plated or solder tipped.

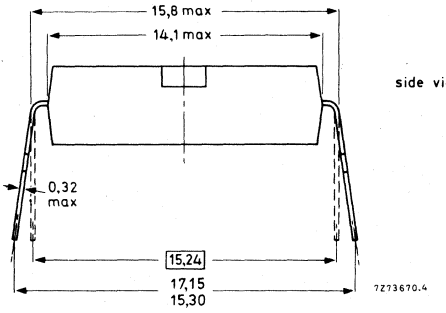
Body material: Ceramic with glass seal at leads.

Lid material: Ceramic; glass seal.

Dimensions in mm, except those in parentheses which are in inches.

24-LEAD DUAL IN-LINE; PLASTIC (SOT-101)





Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,125 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,25 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

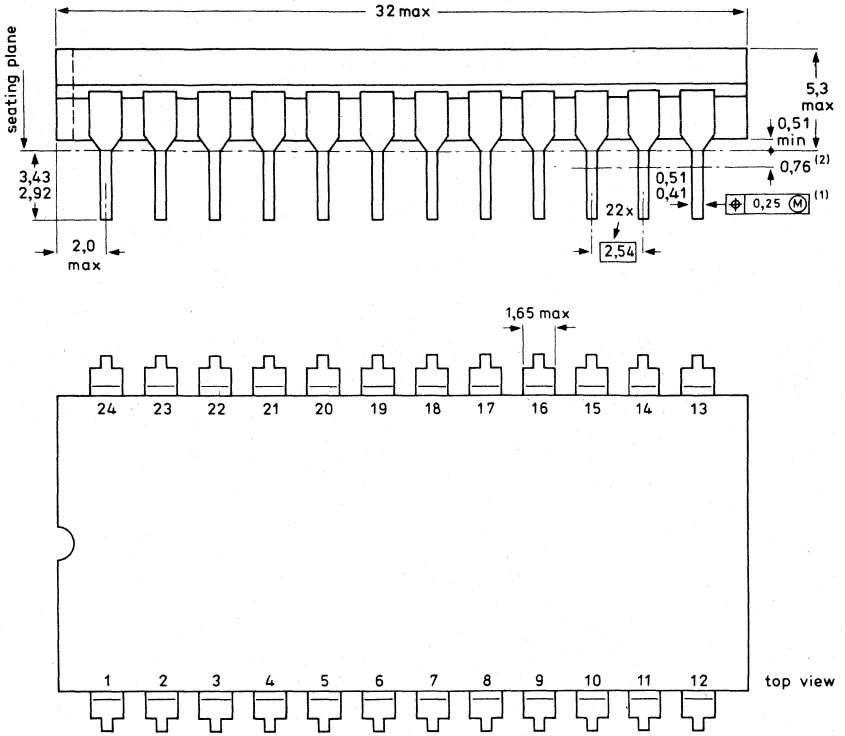
(3) Index may be horizontal as shown, or vertical.

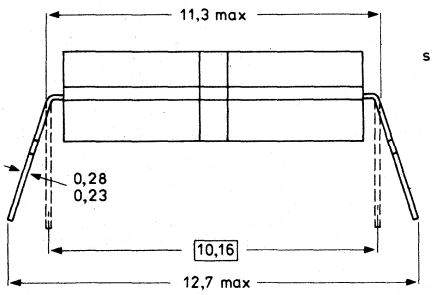
Dimensions in mm

Soldering

See SOT-38 (page 1).

24-LEAD DUAL IN-LINE; CERAMIC (SOT-149)





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,125 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,25 mm.

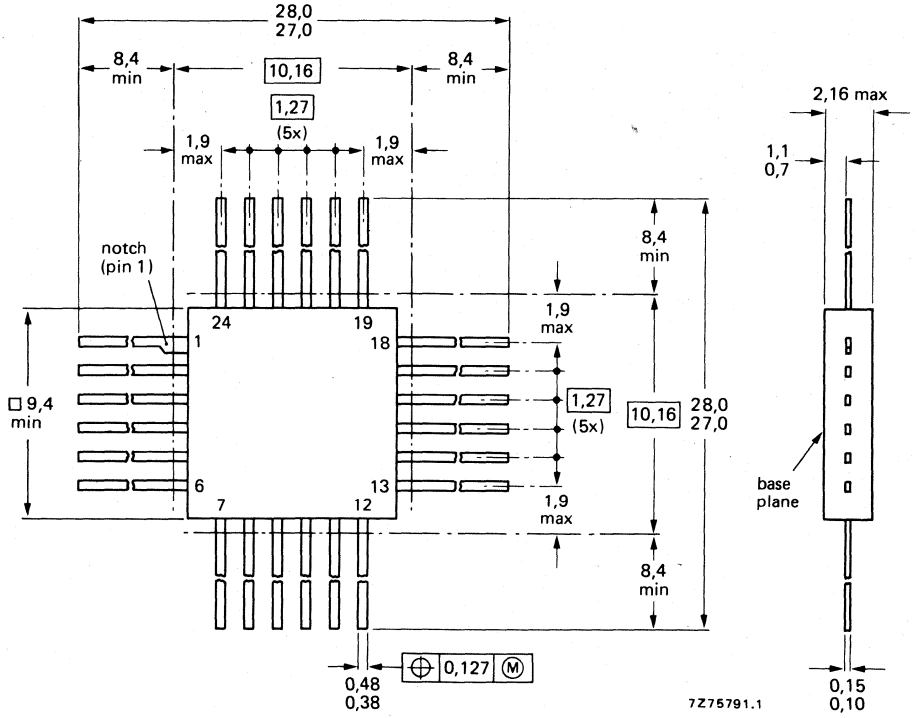
(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

Remarks

1. Leads are given positive misalignment so that they grip after insertion.
2. Leads are Ni-Fe, pure tin plated.

24-LEAD FLATPACK; CERAMIC (SOT-138)



Dimensions in mm

Pins are tin-plated nickel alloy.

Base is Al_2O_3 or BeO (toxic material).

Mass = 0,8 g.

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

DEVICE DATA

GX family (ECL10 000)

QUADRUPLE 2-INPUT NOR GATE WITH STROBE

The GXB10100 is a quadruple 2-input NOR gate with another input common to all gates.
Unused inputs can be left open due to integrated pull-down resistors, which avoids the need for a voltage supply.
Wire-ORing and direct connection to busses is possible due to open-emitter outputs.

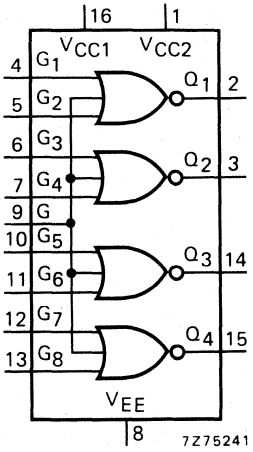


Fig. 1 Logic diagram.

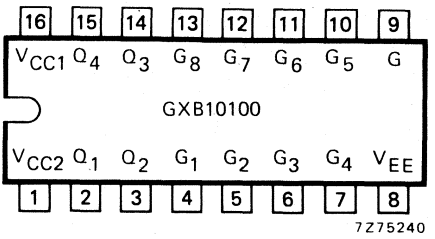


Fig. 2 Pin designation.
$V_{CC1} = V_{CC2} = 0$ V (ground)
$V_{EE} = -5{,}2$ V

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 ± 10% V
Operating ambient temperature range	T_{amb}		−30 to +85 °C
Average propagation delay	t_{PLH}; t_{PHL}	typ.	2,0 ns
Output voltage HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_{av}	typ.	100 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see chapter Package outlines)

GXB10100P: 16-lead DIL: plastic (SOT-38).
GXB10100D: 16-lead DIL: ceramic (SOT-74).

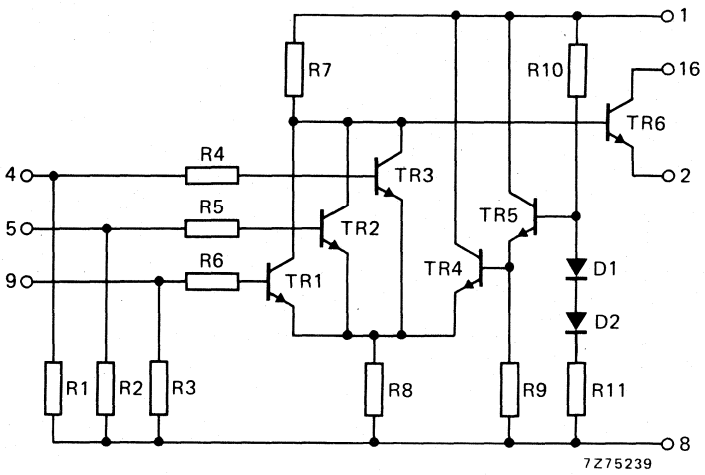
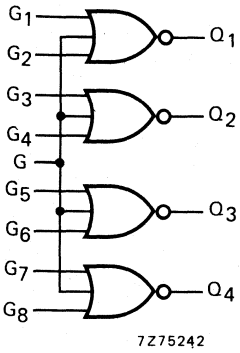


Fig. 3 Circuit diagram (one gate).



$Q_1 = \overline{G_1 + G_2 + G}$
$Q_2 = \overline{G_3 + G_4 + G}$
$Q_3 = \overline{G_5 + G_6 + G}$
$Q_4 = \overline{G_7 + G_8 + G}$

positive logic: HIGH state = 1
LOW state = 0

Fig. 4 Logic function.

RATINGS: see chapter FAMILY SPECIFICATIONS

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5,2 V

	symbol	pin under test	T_{amb} (°C)			conditions	
			−30	25	+85	pin	test voltage
Input current HIGH	I_{IH} max.	4*	390	245	245 μA	4	V_{IHmax}
		9	750	470	490 μA	9	
Input current LOW	I_{IL} min.	4*	−	0,5	− μA	4	V_{ILmin}
Supply current	I_{EE} max.	8	29	26	29 mA	8	V_{EE}

* Individually test each input applying the above-mentioned conditions.

A.C. CHARACTERISTICS

V_{CC1} = V_{CC2} = 0 V (ground); V_{EE} = −5,2 V.

	symbol		T_{amb} (°C)			unit	remarks
			−30	+25	+85		
Propagation delay times	t_{PLH}/t_{PHL}	min.	1,0	1,0	1,0	ns	
		max.	3,1	2,9	3,3	ns	
Transition times rise and fall	t_{TLH}/t_{THL}	min.	1,1	1,1	1,1	ns	20% to 80%
		max.	3,6	3,3	3,7	ns	

* Individually test each input applying the above-mentioned conditions.

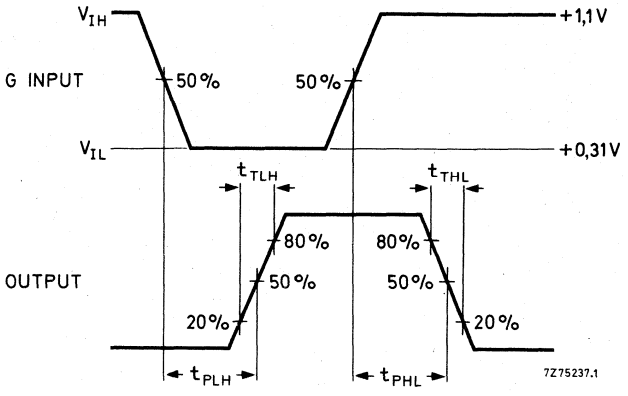


Fig. 5 Switching times testing waveforms.

QUADRUPLE OR/NOR GATE

The GXB10101 is a quadruple 2-input OR/NOR gate with one input from each gate common to pin 12.
Input pull-down resistors (50 kΩ) allow unused inputs to be left open.
The GX family corresponds to the ECL10000 series.

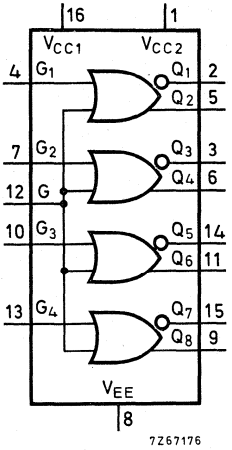


Fig. 1 Logic diagram.

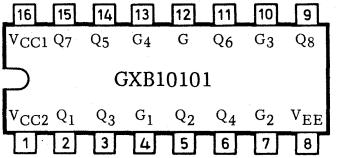


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 ± 10 % V
Operating ambient temperature range	T_{amb}		−30 to +85 °C
Average propagation delay	t_{pd}	typ.	2,0 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package	P_{av}	typ.	100 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINE (see Package outlines)

GXB10101P: plastic 16-lead dual in-line (SOT-38).
GXB10101D: ceramic 16-lead dual in-line (SOT-74).

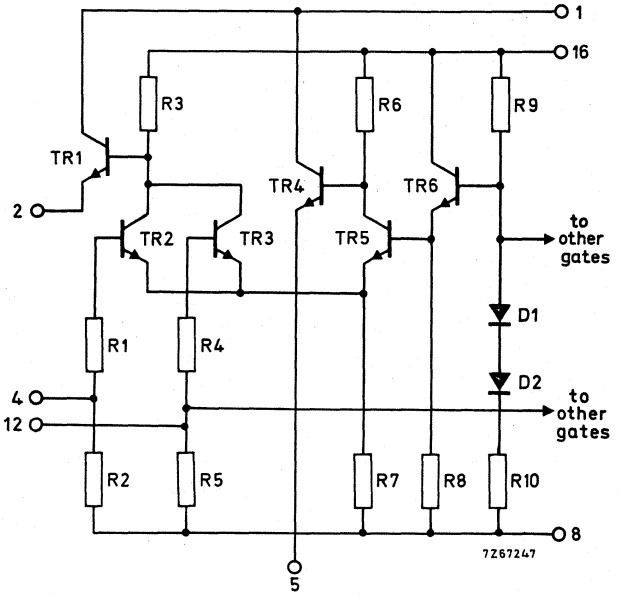
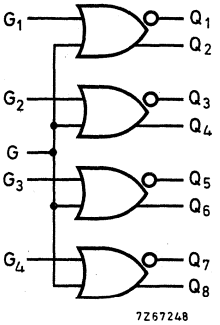


Fig. 3 Circuit diagram (one gate).



$Q_1 = \overline{G_1 + G}$ $\quad Q_5 = \overline{G_3 + G}$

$Q_2 = G_1 + G$ $\quad Q_6 = G_3 + G$

$Q_3 = \overline{G_2 + G}$ $\quad Q_7 = \overline{G_4 + G}$

$Q_4 = G_2 + G$ $\quad Q_8 = G_4 + G$

positive logic: HIGH state = 1
LOW state = 0

Fig. 4 Logic function.

RATINGS see Family Specifications

D.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = −5,2 V

	symbol		T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) +85	conditions
Input current HIGH	I_{IH}	pin 12 max.	850	535	535 μA	V_{IHmax} for input under test
		other inputs max.	425	265	265 μA	
Input current LOW	I_{IL}	min.	0,5	0,5	0,3 μA	V_{ILmin} for input under test
Supply current	I_{EE}	max.	29	26	29 mA	V_{ILmin} for all inputs

A.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = −5,2 V.

	symbol		T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) +85	conditions
Propagation delay time						
LOW → HIGH	t_{PLH}	min.	1,0	1,0	1,0 ns	
		max.	3,1	2,9	3,3 ns	
HIGH → LOW	t_{PHL}	min.	1,0	1,0	1,0 ns	
		max.	3,1	2,9	3,3 ns	
Rise time	t_r	min.	1,1	1,1	1,1 ns	20% to 80%
		max.	3,6	3,3	3,7 ns	
Fall time	t_f	min.	1,1	1,1	1,1 ns	80% to 20%
		max.	3,6	3,3	3,7 ns	

For **switching times test circuit** and **waveform** see Family Specifications.

QUADRUPLE NOR GATE

The GXB10102 is a quadruple 2-input NOR gate.
Input pull-down resistors (50 kΩ) allow unused inputs to be left open.

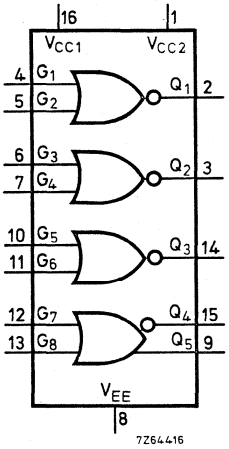


Fig. 1 Logic diagram.

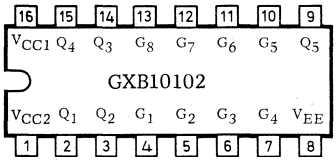


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	$-5{,}2 \pm 10$ %	V
Operating ambient temperature range	T_{amb}	-30 to $+85$	°C
Average propagation delay	t_{PLH}	typ. 2,0	ns
Output voltage			
HIGH state	V_{OH}	nom. -880	mV
LOW state	V_{OL}	nom. -1720	mV
Power consumption per package	P_{av}	typ. 100	mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINE (see Package Outlines)

GXB10102P: plastic 16-lead dual in-line (SOT-38).
GXB10102D: ceramic 16-lead dual in-line (SOT-74).

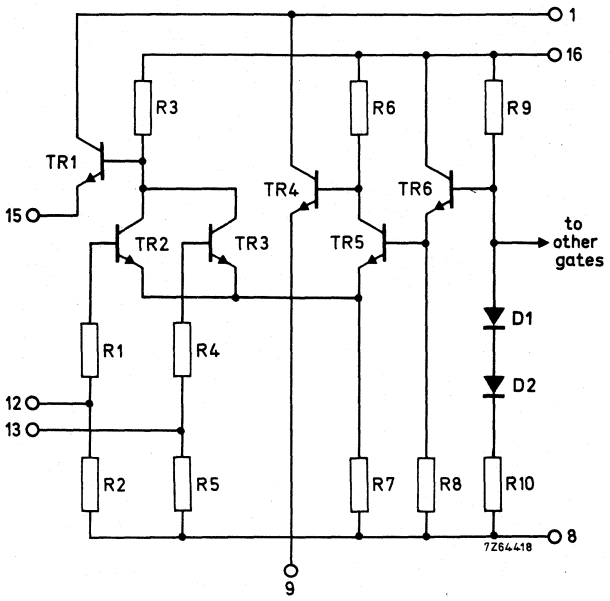
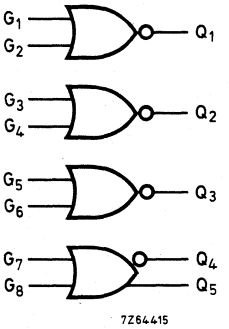


Fig. 3 Circuit diagram (one gate).



$Q_1 = \overline{G_1 + G_2}$
$Q_2 = \overline{G_3 + G_4}$
$Q_3 = \overline{G_5 + G_6}$
$Q_4 = \overline{G_7 + G_8}$
$Q_5 = \overline{Q_4}$

positive logic: HIGH state = 1
LOW state = 0

Fig. 4 Logic function.

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = –5,2 V.

	symbol		T_{amb} (°C) –30	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	conditions
Input current HIGH	I_{IH}	max.	425	265	265	μA	V_{IHmax} for input under test
Input current LOW	I_{IL}		0,5	0,5	0,3	μA	V_{ILmin} for input under test
Supply current	I_{EE}	max.	29	26	29	mA	V_{ILmin} for all inputs

A.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = –5,2 V.

	symbol		T_{amb} (°C) –30	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	conditions
Rise propagation delay time: LOW ⟶ HIGH	t_{PLH}	min.	1,0	1,0	1,0	ns	
		max.	3,1	2,9	3,3	ns	
HIGH ⟶ LOW	t_{PHL}	min.	1,0	1,0	1,0	ns	
		max.	3,1	2,9	3,3	ns	
Rise time	t_{TLH}	min.	1,1	1,1	1,1	ns	20% to 80%
		max.	3,6	3,3	3,7	ns	
Fall time	t_{THL}	min.	1,1	1,1	1,1	ns	20% to 80%
		max.	3,6	3,3	3,7	ns	

For **switching times test circuit** and **waveform** see Family Specifications.

QUADRUPLE 2-INPUT OR GATE

The GXB10103 is a quadruple 2-input 3 OR and 1 OR/NOR gate.
Input pull-down resistors (50 kΩ) allow unused inputs to be left open.

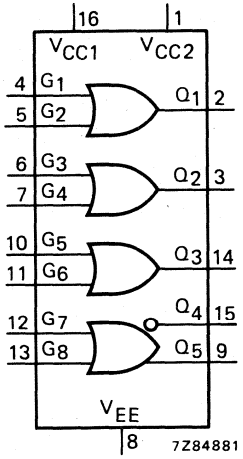


Fig. 1 Logic diagram.

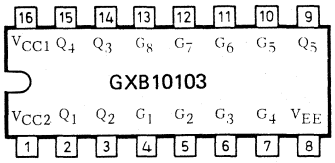


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 ± 10 % V
Operating ambient temperature range	T_{amb}		−30 to + 85 °C
Average propagation delay	t_{pd}	typ.	2,0 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package	P_{av}	typ.	100 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINE (see Package Outlines)

GXB10102P: plastic 16-lead dual in-line (SOT-38)
GXB10102D: ceramic 16-lead dual in-line (SOT-74).

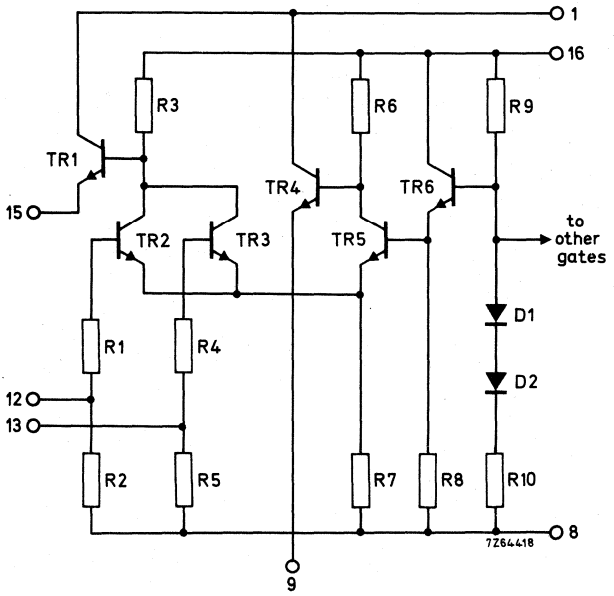
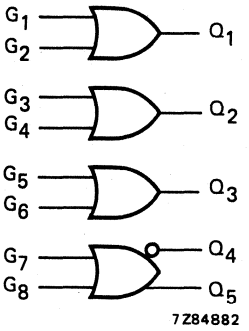


Fig. 3 Circuit diagram (one gate).



$Q_1 = G_1 + G_2$
$Q_2 = G_3 + G_4$
$Q_3 = G_5 + G_6$
$Q_5 = G_7 + G_8$
$Q_4 = \overline{Q_5}$

positive logic: HIGH state = 1
LOW state = 0

Fig. 4 Logic function.

RATINGS see Family Specifications

D.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = –5,2 V.

	symbol		T_{amb} (°C) –30	+25	+85	unit	conditions
Input current HIGH	I_{IH}	max.	390	245	245	μA	V_{IHA} for input under test
Input current LOW	I_{IL}		0,5	0,5	0,3	μA	V_{ILB} for input under test
Supply current	I_{EE}	max.	29	26	29	mA	V_{ILB} for all inputs

A.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = –5,2 V.

	symbol		T_{amb} (°C) –30	+25	+85	unit	conditions
Rise propagation delay time:	t_{PLH}	min.	1,0	1,0	1,0	ns	
		max.	3,1	2,9	3,3	ns	
Fall propagation delay time:	t_{PHL}	min.	1,0	1,0	1,0	ns	
		max.	3,1	2,9	3,3	ns	
Rise time	t_{TLH}	min.	1,1	1,1	1,1	ns	20% to 80%
		max.	3,6	3,3	3,7	ns	
Fall time	t_{THL}	min.	1,1	1,1	1,1	ns	
		max.	3,6	3,3	3,7	ns	

For **switching times test circuit** and **waveforms** see Family Specifications.

QUADRUPLE 2-INPUT AND GATE

The GXB10104 is a high-speed logic, low power, AND function.
Open emitter outputs feature:
- easy choice of interface techniques.
- low power consumption when loaded by transmission lines.
- wired-OR capability of the outputs makes the device suitable for control, bussing and communications in high-speed processors, high-speed peripherals, instrumentation and digital communication systems.

Input pull-down resistors allow unused inputs to be left open and provide high d.c. and a.c. fan-out.

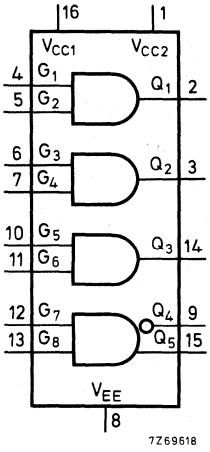


Fig. 1 Logic diagram.

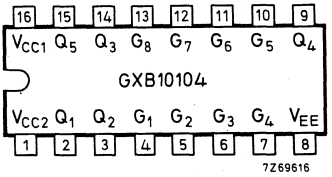


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	−5,2 ± 10%	V
Operating ambient temperature range	T_{amb}	−30 to + 85	°C
Average propagation delay	t_{PLH}	typ. 2,7	ns
Output voltage			
HIGH state	V_{OH}	nom. −880	mV
LOW state	V_{OL}	nom. −1720	mV
Power consumption per package	P_{av}	typ. 140	mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINE (see Package Outlines)

GXB10104P : plastic 16-lead dual in-line (SOT-38).
GXB10104D: ceramic 16-lead dual in-line (SOT-74).

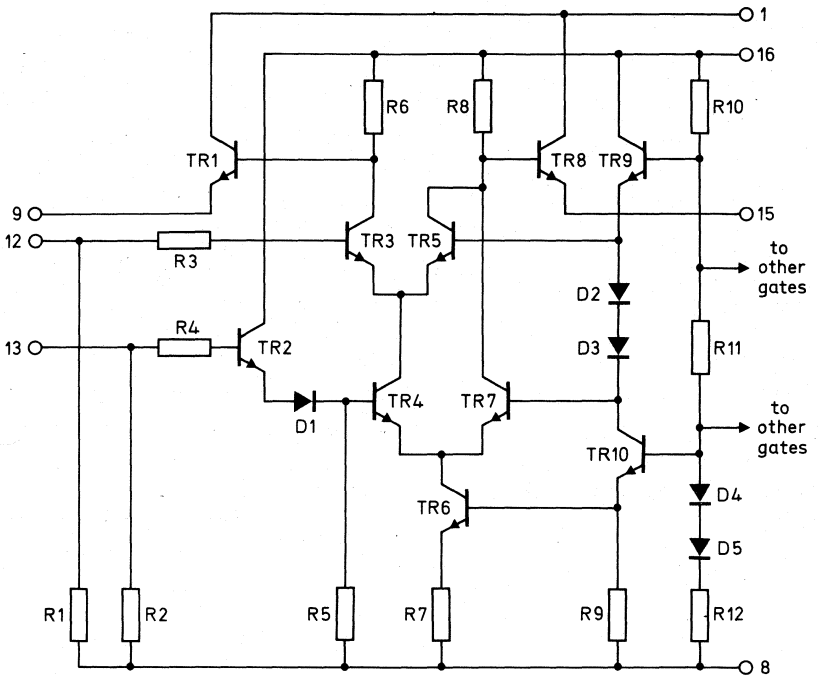
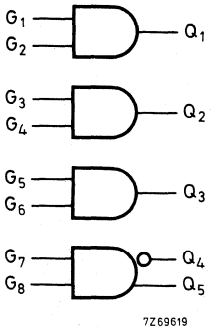


Fig. 3 Circuit diagram (one gate).



$Q_1 = G_1 \cdot G_2$
$Q_2 = G_3 \cdot G_4$
$Q_3 = G_5 \cdot G_6$
$Q_4 = \overline{Q_5}$
$Q_5 = G_7 \cdot G_8$

Positive logic:
H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0

Fig. 4 Logic function.

RATINGS see chapter Family Specifications

D.C. CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground; $V_{EE} = -5{,}2$ V; R_L 50 Ω to −2 V.

	symbol		pin under test	T_{amb} (°C) −30	+ 25	+ 85	unit	remarks
Supply current	I_{EE}	max.	8	39	35	39	mA	
Input current HIGH	I_{IH}	max.	4, 7 10, 13	425	265	265	μA	
Input current HIGH	I_{IH}	max.	5, 6 11, 12	350	220	220	μA	
Input current LOW	I_{IL}	min.	each input	0,5	0,5	0,3	μA	

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2$ V; $V_{EE} = -3{,}2$ V; $T_{amb} = 25$ °C

	symbol		T_{amb} (°C) −30	+ 25	+ 85	unit	remarks
Rise propagation delay time LOW ⟶ HIGH	t_{PLH}	min.	1,0	1,0	1,0	ns	
		max.	4,3	4,0	4,2	ns	
Fall propagation delay time HIGH ⟶ LOW	t_{PHL}	min.	1,0	1,0	1,0	ns	
		max.	4,3	4,0	4,2	ns	
Rise time	t_{TLH}	min.	1,1	1,1	1,1	ns	20% to 80%
		max.	3,7	3,5	3,6	ns	
Fall time	t_{THL}	min.	1,1	1,1	1,1	ns	20% to 80%
		max.	3,7	3,5	3,6	ns	

For **switching times test circuit** and **waveforms** see Family Specifications.

TRIPLE OR/NOR GATE

The GXB10105 is a triple 2-3-2 input OR/NOR gate.
Input pull-down resistors (50 kΩ) allow unused inputs to be left open.

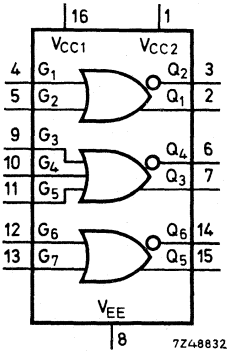


Fig. 1 Logic diagram.

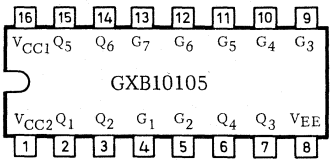


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 ± 10 % V
Operating ambient temperature range	T_{amb}		−30 to +85 °C
Average propagation delay	t_{pd}	typ.	2,0 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package	P_{AV}	typ.	75 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINE (see Package Outlines)

GXB10105P: plastic 16-lead dual in-line (SOT-38).
GXB10105D: ceramic 16-lead dual in-line (SOT-74).

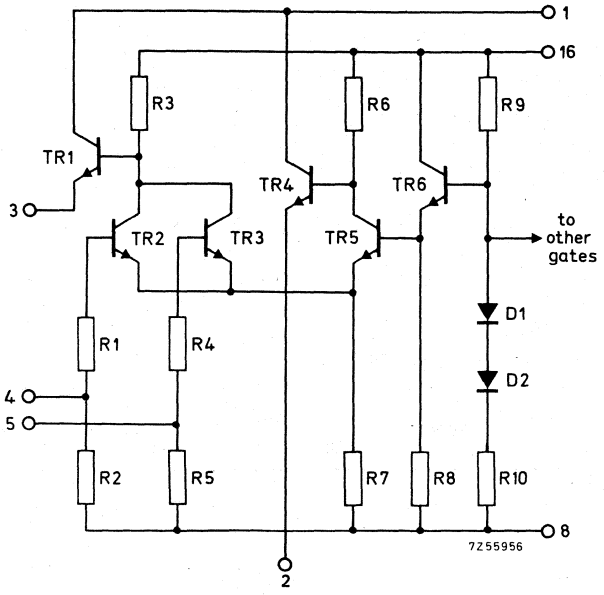
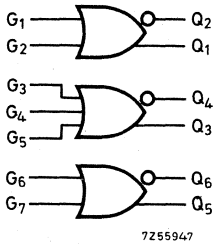


Fig. 3 Circuit diagram (one gate).



$Q_1 = G_1 + G_2$ $\quad Q_2 = \overline{G_1 + G_2}$

$Q_3 = G_3 + G_4 + G_5$ $\quad Q_4 = \overline{G_3 + G_4 + G_5}$

$Q_5 = G_6 + G_7$ $\quad Q_6 = \overline{G_6 + G_7}$

positive logic: HIGH state = 1
LOW state = 0

Fig. 4 Logic function.

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = −5,2 V

	symbol		T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Input current HIGH	I_{IH}	max.	425	265	265	μA	
Input current LOW	I_{IL}	min.	0,5	0,5	0,3	μA	
Supply current	I_{EE}	max.	23	21	23	mA	

A.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = −5,2 V; T_{amb} = 25 °C

	symbol		T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Rise propagation delay time:	t_{PLH}	min.	1,0	1,0	1,0	ns	
		max.	3,1	2,9	3,3	ns	
Fall propagation delay time:	t_{PHL}	min.	1,0	1,0	1,0	ns	
		max.	3,1	2,9	3,3	ns	
Rise time	t_{TLH}	min.	1,1	1,1	1,1	ns	20% to 80%
		max.	3,6	3,3	3,7	ns	
Fall time	t_{THL}	min.	1,1	1,1	1,1	ns	20% to 80%
		max.	3,6	3,3	3,7	ns	

For **switching times test circuit** and **waveforms** see Family Specifications.

TRIPLE NOR GATE

The GXB10106 is a triple 4-3-3 input NOR gate.
Input pull-down resistors (50 kΩ) allow unused inputs to be left open.

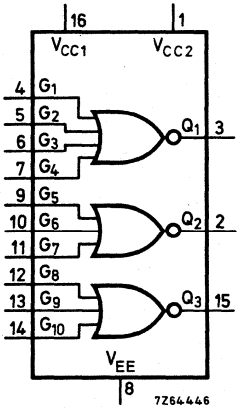
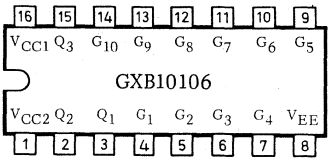


Fig. 1 Logic diagram.



Pin 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 ± 10 % V
Operating ambient temperature range	T_{amb}		−30 to +85 °C
Average propagation delay	t_{PLH}/t_{PHL}	typ.	2,0 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package	P_{av}	typ.	75 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINE (see Package Outlines)

GXB10106P: plastic 16-lead dual in-line (SOT-38).
GXB10106D: ceramic 16-lead dual in-line (SOT-74).

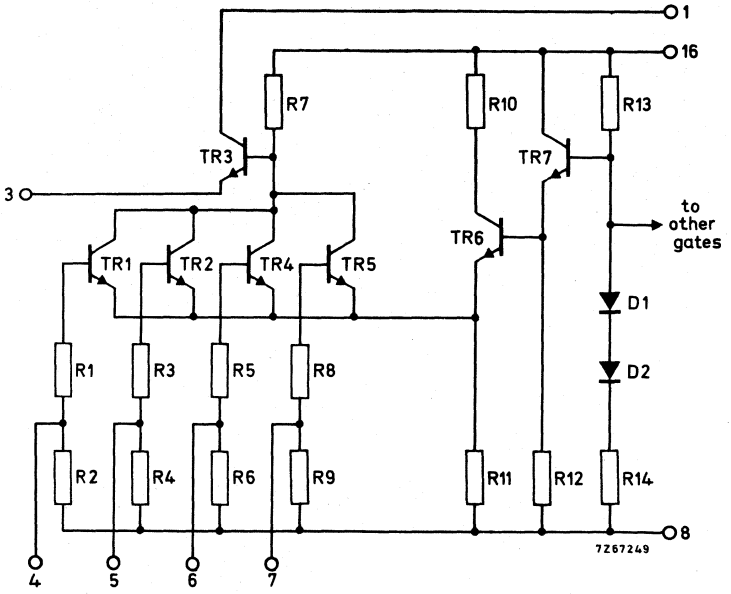
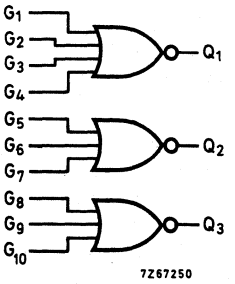


Fig. 3 Circuit diagram (one gate).



$$Q_1 = \overline{G_1 + G_2 + G_3 + G_4}$$
$$Q_2 = \overline{G_5 + G_6 + G_7}$$
$$Q_3 = \overline{G_8 + G_9 + G_{10}}$$

positive logic: HIGH state = 1
LOW state = 0

Fig. 4 Logic functions.

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = −5,2 V

	symbol		T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Input current HIGH	I_{IH}	max.	425	265	265	μA	
Input current LOW	I_{IL}	min.	0,5	0,5	0,3	μA	
Supply current	I_{EE}	max.	23	21	23	mA	

A.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = −5,2 V

	symbol		T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Rise propagation delay time:	t_{PLH}	min.	1,0	1,0	1,0	ns	
		max.	3,1	2,9	3,3	ns	
Fall propagation delay time:	t_{PHL}	min.	1,0	1,0	1,0	ns	
		max.	3,1	2,9	3,3	ns	
Rise time	t_{TLH}	min.	1,1	1,1	1,1	ns	20% to 80%
		max.	3,6	3,3	3,7	ns	
Fall time	t_{THL}	min.	1,1	1,1	1,1	ns	
		max.	3,6	3,3	3,7	ns	

For **switching times test circuit** and **waveforms** see Family Specifications.

TRIPLE EXCLUSIVE OR/EXCLUSIVE NOR GATE

The GXB10107 is a three gate array designed to provide the positive EXCLUSIVE OR and NOR functions. Input pull-down resistors (50 kΩ) allow unused inputs to be left open.

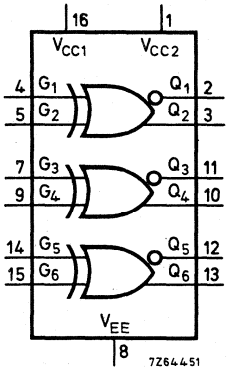


Fig. 1 Logic diagram.

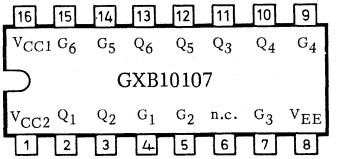


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	−5,2 ± 10	% V
Operating ambient temperature	T_{amb}	−30 to +85	°C
Average propagation delay	t_{PLH}	typ. 2,4	ns
Output voltage			
HIGH state	V_{OH}	nom. −880	mV
LOW state	V_{OL}	nom. −1720	mV
Power consumption per package	P_{av}	typ. 115	mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINE (see Package Outlines)

GXB10107P: plastic 16-lead dual in-line (SOT-38).
GXB10107D: ceramic 16-lead dual in-line (SOT-74).

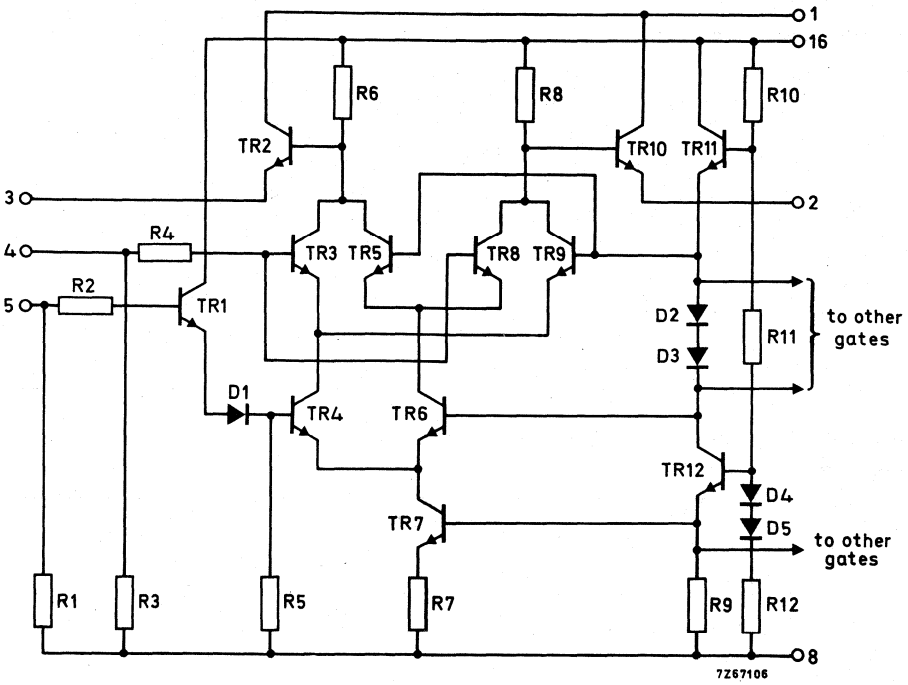
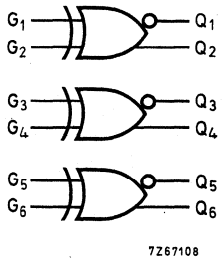


Fig. 3 Circuit diagram (one gate).



$Q_1 = \overline{G_1} \cdot \overline{G_2} + G_1 \cdot G_2$

$Q_2 = G_1 \cdot \overline{G_2} + \overline{G_1} \cdot G_2$

$Q_3 = \overline{G_3} \cdot \overline{G_4} + G_3 \cdot G_4$

$Q_4 = G_3 \cdot \overline{G_4} + \overline{G_3} \cdot G_4$

$Q_5 = \overline{G_5} \cdot \overline{G_6} + G_5 \cdot G_6$

$Q_6 = G_5 \cdot \overline{G_6} + \overline{G_5} \cdot G_6$

positive logic: HIGH state = 1
LOW state = 0

Fig. 4 Logic functions.

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = −5,2 V

	symbol		T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Input current HIGH							
pins 4, 9, 14	I_{IH}	max.	425	265	265	μA	
pins 5, 7, 15	I_{IH}	max.	350	220	220	μA	
Input current LOW	I_{IL}	min.	0,5	0,5	0,3	μA	
Supply current	I_{EE}	max.	31	28	31	mA	

A.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = −5,2 V.

	symbol		T_{amb} (°C) −35	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Rise propagation delay times	t_{PLH}	min.	1,1	1,1	1,1	ns	
		max.	3,8	3,7	4,0	ns	
Fall propagation delay times	t_{PHL}	min.	1,1	1,1	1,1	ns	
		max.	3,8	3,7	4,0	ns	
Rise time	t_{TLH}	min.	1,1	1,1	1,1	ns	20% to 80%
		max.	3,5	3,5	3,8	ns	
Fall time	t_{THL}	min.	1,1	1,1	1,1	ns	20% to 80%
		max.	3,5	3,5	3,8	ns	

For **switching times test circuit** and **waveforms** see Family Specifications.

DUAL 4-INPUT AND/NAND GATE

The GXB10108 is a dual AND/NAND gate. Featuring:

- Fast propagation delay
- High fanout capability
- High impedance inputs with 50 kΩ pull down resistors

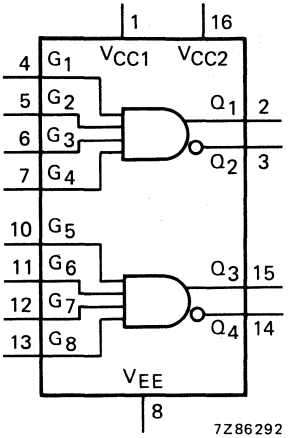


Fig. 1 Logic diagram.

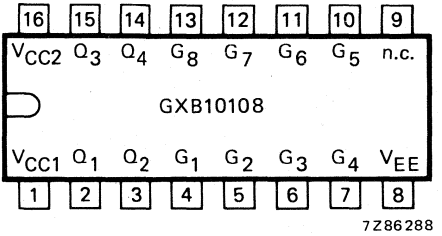


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	−5,2 ± 5%	V
Operating ambient temperature	T_{amb}	−30 to + 85	°C
Average propagation delay			
AND output	t_{PLH}/t_{PHL}	typ. 2,3	ns
NAND output	t_{PLH}/t_{PHL}	typ. 2,8	ns
Power consumption per package (no load)	P_{av}	typ. 145	mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (see Package Outlines)

GXB10108P : plastic 16-lead dual-in-line (SOT-38).
GXB10108D: ceramic 16-lead dual-in-line (SOT-74).

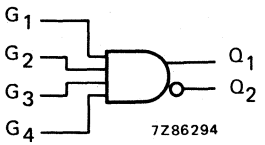


Fig. 3 Logic function
(one AND/NAND gate).

$Q_1 = G_1 \cdot G_2 \cdot G_3 \cdot G_4$
$Q_2 = \overline{Q}_1$

Positive logic
H = HIGH state
(the more positive voltage) = 1
L = LOW state
(the more negative voltage) = 0

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground; $V_{EE} = -5{,}2$ V; R_L 50 Ω to −2 V.

	symbol		T_{amb} (°C) −30	+ 25	+ 85	unit	remarks
Supply current	I_{EE}	max.	40	36	40	mA	
Input current HIGH	I_{IH}	max.	425	265	265	μA	
Input current LOW	I_{IL}	min.	0,5	0,5	0,3	μA	

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2$ V; $V_{EE} = -3{,}2$ V; $T_{amb} = 25$ °C

	symbol		T_{amb} (°C) −30	+ 25	+ 85	unit	remarks
Rise and fall propagation delay time							
LOW → HIGH	t_{PLH}	min.	1,4	1,4	1,4	ns	
HIGH → LOW	t_{PHL}	max.	4,1	3,7	4,1	ns	
Transition rise and fall time	t_{TLH} / t_{THL}	min.	1,1	1,1	1,1	ns	between 20% to 80%
		max.	4,5	4,0	4,5	ns	

For **switching times test circuit** and **waveforms** see Family Specifications.

DUAL OR/NOR GATE

The GXB10109 is a dual 4-5 input OR/NOR gate.
Input pull-down resistors (50 kΩ) allow unused inputs to be left open.

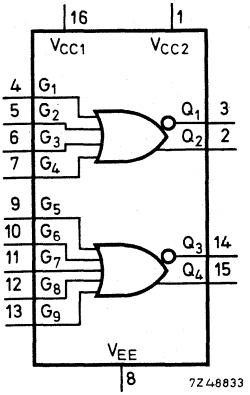


Fig. 1 Logic diagram.

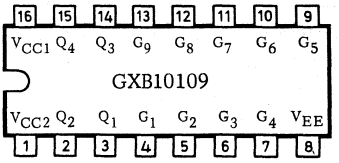


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 ± 10 % V
Operating ambient temperature range	T_{amb}		−30 to + 85 °C
Average propagation delay	t_{PLH}	typ.	2,0 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package	P_{av}	typ.	50 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINE (see Package Outlines).

GXB10109P: plastic 16-lead dual in-line (SOT-38).
GXB10109D: ceramic 16-lead dual in-line (SOT-74).

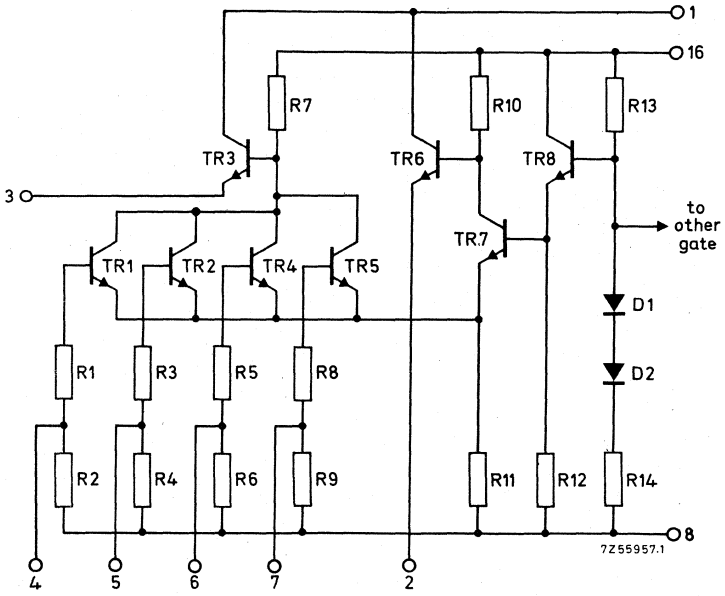
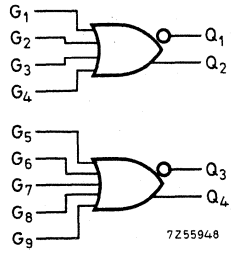


Fig. 3 Circuit diagram (one gate).



$$Q_1 = \overline{G_1 + G_2 + G_3 + G_4}$$

$$Q_3 = \overline{G_5 + G_6 + G_7 + G_8 + G_9}$$

$$Q_2 = G_1 + G_2 + G_3 + G_4$$

$$Q_4 = G_5 + G_6 + G_7 + G_8 + G_9$$

Positive logic: HIGH state = 1
LOW state = 0

Fig. 4 Logic functions.

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = −5,2 V.

	symbol		T_{amb} (°C) −30	+25	+85	unit	remarks
Input current HIGH	I_{IH}	max.	425	265	265	μA	
Input current LOW	I_{IL}	min.	0,5	0,5	0,3	μA	
Supply current	I_{EE}	max.	15	14	15	mA	

A.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = −5,2 V.

	symbol		T_{amb} (°C) −30	+25	+85	unit	remarks
Rise propagation delay time	t_{PLH}	min.	1,0	1,0	1,0	ns	
		max.	3,1	2,9	3,3	ns	
Fall propagation delay time	t_{PHL}	min.	1,0	1,0	1,0	ns	
		max.	3,1	2,9	3,3	ns	
Rise time	t_{TLH}	min.	1,1	1,1	1,1	ns	20% to 80%
		max.	3,6	3,3	3,7	ns	
Fall time	t_{THL}	min.	1,1	1,1	1,1	ns	
		max.	3,6	3,3	3,7	ns	

For **switching times test circuit** and **waveforms** see Family Specifications.

DUAL 3-INPUT/3-OUTPUT OR LINE DRIVER

The GXB10110 is a dual 3-input/3-output OR gate intended to drive up to three transmission lines simultaneously. This feature makes the device particularly useful in clock distribution applications.

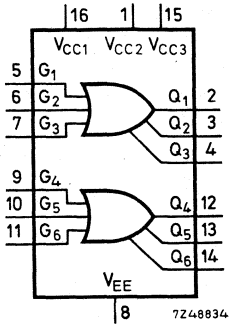


Fig. 1 Logic diagram.

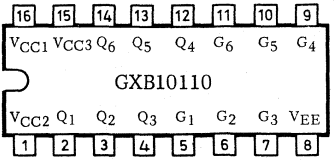


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = V_{CC3} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	−5,2 ± 10%	V
Operating ambient temperature range	T_{amb}	−30 to + 85	°C
Average propagation delay	t_{PLH}	typ. 2,4	ns
Output voltage			
HIGH state	V_{OH}	nom. −880	mV
LOW state	V_{OL}	nom. −1720	mV
Power consumption per package	P_{av}	typ. 150	mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see Package Outlines)

GXB10110P : plastic 16-lead dual in-line (SOT-38).
GXB10110D: ceramic 16-lead dual in-line (SOT-74).

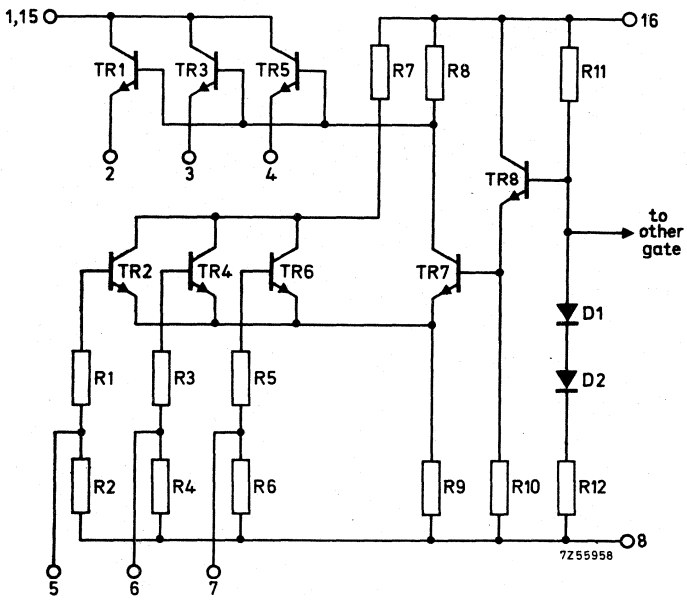
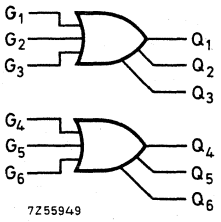


Fig. 3 Circuit diagram (one gate).



$Q_1 = Q_2 = Q_3 = G_1 + G_2 + G_3$

$Q_4 = Q_5 = Q_6 = G_4 + G_5 + G_6$

Positive logic: HIGH state = 1
LOW state = 0

Fig. 4 Logic function.

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = −5,2 V.

	symbol		T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Input current HIGH	I_{IH}	max.	680	425	425	μA	
Input current LOW	I_{IL}	min.	0,5	0,5	0,3	μA	
Supply current	I_{EE}	max.	42	38	42	mA	

A.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = −5,2 V

	symbol		T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Rise propagation delay time	t_{PLH}	min.	1,4	1,4	1,5	ns	
		max.	3,5	3,5	3,8	ns	
Fall propagation delay time	t_{PHL}	min.	1,4	1,4	1,5	ns	
		max.	3,5	3,5	3,8	ns	
Rise time	t_{TLH}	min.	1,0	1,1	1,2	ns	between 20% and 80%
		max.	3,5	3,5	3,8	ns	
Fall time	t_{THL}	min.	1,0	1,1	1,2	ns	between 20% and 80%
		max.	3,5	3,5	3,8	ns	

For **switching times test circuit** and **waveforms** see Family Specifications.

DUAL 3-INPUT/3-OUTPUT NOR LINE DRIVER

The GXB10111 is a dual 3-input/3-output NOR gate intended to drive up to three transmission lines simultaneously. The ability to control three parallel lines makes this device particularly useful in clock distribution applications.

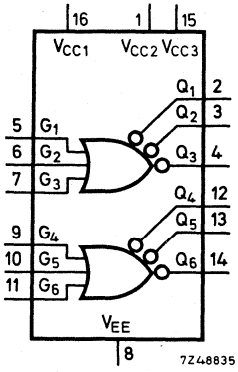


Fig. 1 Logic diagram.

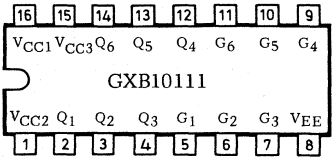


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = V_{CC3} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	$-5{,}2 \pm 10$ %	V
Operating ambient temperature range	T_{amb}	-30 to $+85$	°C
Average propagation delay	t_{PLH}	typ. 2,4	ns
Output voltage			
HIGH state	V_{OH}	nom. -880	mV
LOW state	V_{OL}	nom. -1720	mV
Power consumption per package	P_{av}	typ. 150	mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (see Package Outlines)

GXB10111P: plastic 16-lead dual in-line (SOT-38).
GXB10111D: ceramic 16-lead dual in-line (SOT-74).

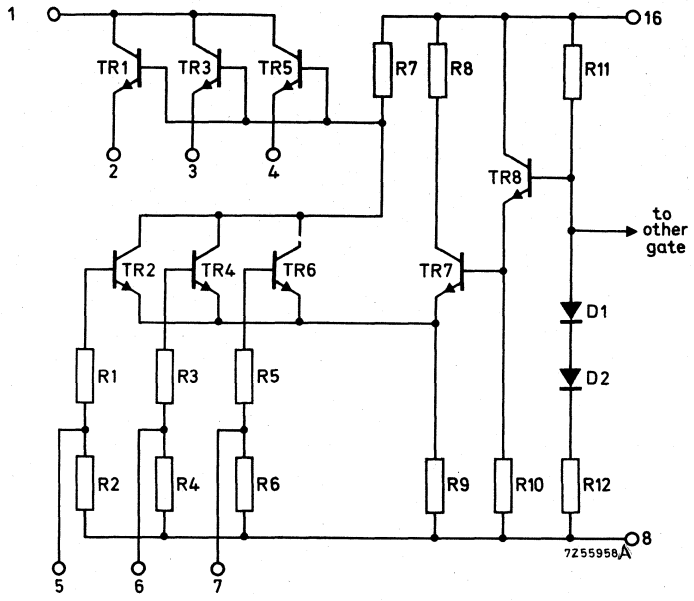


Fig. 3 Circuit diagram (one gate).

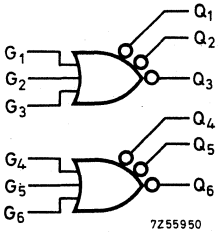


Fig. 4 Logic function.

$$Q_1 = Q_2 = Q_3 = \overline{G_1 + G_2 + G_3}$$
$$Q_4 = Q_5 = Q_6 = \overline{G_4 + G_5 + G_6}$$

Positive logic: HIGH state = 1
LOW state = 0

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = −5,2 V.

	symbol		T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Input current HIGH	I_{IH}	max.	680	425	425	μA	
Input current LOW	I_{IL}	min.	0,5	0,5	0,3	μA	
Supply current	I_{EE}	max.	42	38	42	mA	

A.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = −5,2 V.

	symbol		T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Rise propagation delay time:	t_{PLH}	min.	1,4	1,4	1,5	ns	
		max.	3,5	3,5	3,8	ns	
Fall propagation delay time	t_{PHL}	min.	1,4	1,4	1,5	ns	
		max.	3,5	3,5	3,8	ns	
Rise time	t_{TLH}	min.	1,0	1,1	1,2	ns	between 20% and 80%
		max.	3,5	3,5	3,8	ns	
Fall time	t_{THL}	min.	1,0	1,1	1,2	ns	
		max.	3,5	3,5	3,8	ns	

For **switching times test circuit** and **waveforms** see Family Specifications.

DUAL 3-INPUT 1-OR/2-NOR GATE

The GXB10112 is a three input single OR/double NOR gate outputs. Input pull-down resistors (50 kΩ) allow unused inputs to be left open.

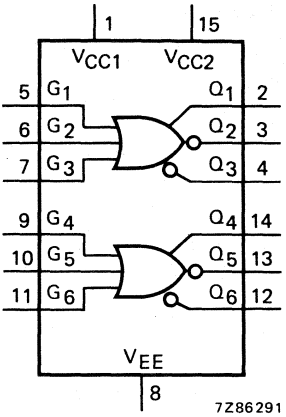


Fig. 1 Logic diagram.

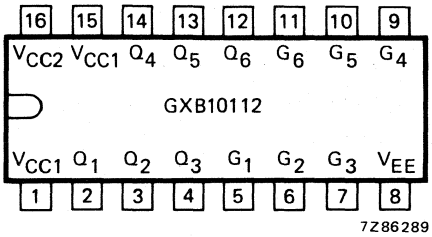


Fig. 2 Pin designation.

$V_{CC2} = V_{CC1} = 0$ V (ground); $V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	−5,2 ± 5%	V
Operating ambient temperature	T_{amb}	−30 to + 85	°C
Average propagation delay	t_{PHL}/t_{PLH}	typ. 2,4	ns
Power consumption per package (no load)	P_{av}	typ. 150	mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (see Package Outlines)

GXB10112P : plastic 16-lead dual in-line (SOT-38).
GXB10112D: ceramic 16-lead dual in-line (SOT-74).

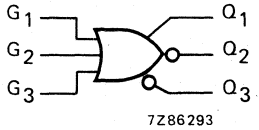


Fig. 3 Logic function.

Function table

$Q_1 = G_1 \cdot G_2 \cdot G_3$

$Q_2 = \overline{Q_1}$

$Q_3 = \overline{Q_1}$

Positive logic:

H = HIGH state = the more positive voltage = 1
L = LOW state = the more negative voltage = 0

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = –5,2 V.

	symbol		T_{amb} (°C) –30	+ 25	+ 85	unit	remarks
Input current HIGH	I_{IH}	max.	680	425	425	μA	
Input current LOW	I_{IL}	min.	0,5	0,5	0,3	μA	
Supply current	I_{EE}	max.	42	38	42	mA	

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = + 2,0 V; V_{EE} = –3,2 V

	symbol		T_{amb} (°C) –35	+ 25	+ 85	unit	remarks
Propagation delay rise and fall times	t_{PLH}	min.	1,4	1,4	1,5	ns	
	$\overline{PHL}$	max.	3,5	3,5	3,8	ns	
Transition rise and fall times	t_{TLH}	min.	1,0	1,1	1,2	ns	between
	$\overline{THL}$	max.	3,5	3,5	3,8	ns	20% and 80%

QUADRUPLE EXCLUSIVE-OR GATE

The GXB10113 is a quadruple EXCLUSIVE-OR gate with an enable input common to all gates. Unused inputs need not be tied to V_{EE} since input pull-down resistors are integrated in the circuit. The enable is active in LOW state. A 4-bit comparison function (A = B) can be obtained by wire-ORing the four outputs together. Direct connection to busses is possible thanks to open emitter outputs.

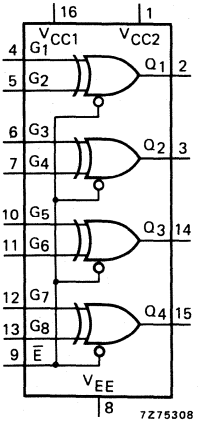


Fig. 1 Logic diagram.

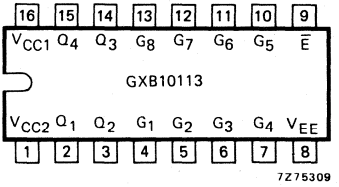


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 ± 10 % V
Operating ambient temperature range	T_{amb}		−30 to +85 °C
Average propagation delay	t_{PHL}	typ.	3,0 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_{av}	typ.	175 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (see Package Outlines)

GXB10113P: 16-lead DIL: plastic (SOT-38).
GXB10113D: 16-lead DIL: ceramic (SOT-74).

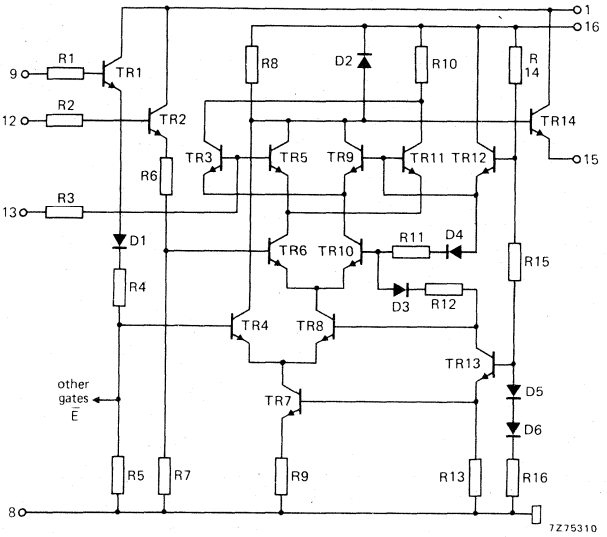


Fig. 3 Circuit diagram (one gate).

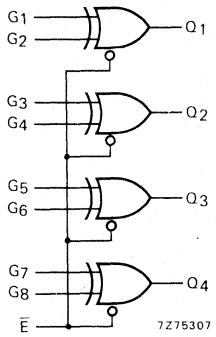


Fig. 4 Logic function.

$$Q_1 = \overline{G_1 + G_2 + \bar{E}}$$

$$Q_2 = \overline{G_3 + G_4 + \bar{E}}$$

$$Q_3 = \overline{G_5 + G_6 + \bar{E}}$$

$$Q_4 = \overline{G_7 + G_8 + \bar{E}}$$

FUNCTION TABLE

G_1	G_2	$\bar{E}$	Q_1
L	L	L	L
L	H	L	H
H	L	L	H
H	H	L	L
X	X	H	L

Positive logic: HIGH state = 1
LOW state = 0

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS see Family Specifications

D.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = −5,2 V.

	symbol		pin under test	T_{amb} (°C) −30	+25	+85	unit	remarks
Input current HIGH	I_{IH}	max.	4,7,10,13	425	265	265	μA	
			5,6,11,12	350	220	220	μA	
			9	870	545	545	μA	
Input current LOW	I_{IL}	min.	each data input	0,5	0,5	0,3	μA	
Supply current	I_{EE}	max.		46	42	46	mA	

A.C. CHARACTERISTICS

V_{CC1} = V_{CC2} = 2,0 V; V_{EE} = −3,2 V.

	symbol		T_{amb} (°C) −30	+25	+85	unit	remarks
Rise propagation delay time	t_{PLH}	min.	1,1	1,3	1,3	ns	independent inputs
		max.	4,7	4,5	5,0	ns	
	t_{PLH}	min.	1,3	1,5	1,5	ns	enable input
		max.	5,2	5,0	5,5	ns	
Fall propagation delay time	t_{PLH}	min.	1,1	1,3	1,3	ns	independent inputs
		max.	4,7	4,5	5,0	ns	
	t_{PLH}	min.	1,3	1,5	1,5	ns	enable input
		max.	5,2	5,0	5,5	ns	
Rise time	t_{TLH}	min.	1,1	1,1	1,1	ns	between 20% and 80%
		max.	4,2	3,9	4,4	ns	
Fall time	t_{TLH}	min.	1,1	1,1	1,1	ns	
		max.	4,2	3,9	4,4	ns	

For **switching times test circuit** and **waveforms** see Family Specifications.

TRIPLE LINE RECEIVER

The GXB10114 is a triple line receiver with low impedance emitter follower complementary outputs. With translated emitter follower inputs and an active current source, it features a common mode rejection peak voltage of ± 1 V. Furthermore, the OR outputs keep a LOW logic level, whenever the inputs are left floating. Intended primarily to receive data from balanced twisted-pair lines, this device is also suitable for minicomputers, testing and instrumentation. It can also be used as a sense amplifier for MOS RAMs as a MOS-to-ECL interface circuit; as a high speed comparator and, having an internal reference supply voltage (V_{BB}), it can operate as a Schmitt trigger.

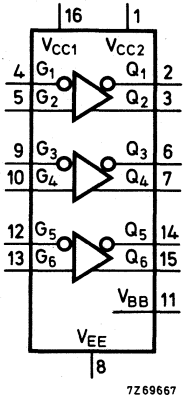


Fig. 1 Logic diagram

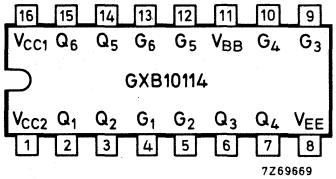


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 ± 10 % V
Operating ambient temperature range	T_{amb}		30 to +85 °C
Average propagation delay			
single-ended input	t_{PHL}	typ.	2,4 ns
differential input	t_{PHL}	typ.	2,0 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package	P_{av}	typ.	145 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see Package Outlines)

GXB10114P: plastic 16-lead dual in-line (SOT-38)
GXB10114D: ceramic 16-lead dual in-line (SOT-74).

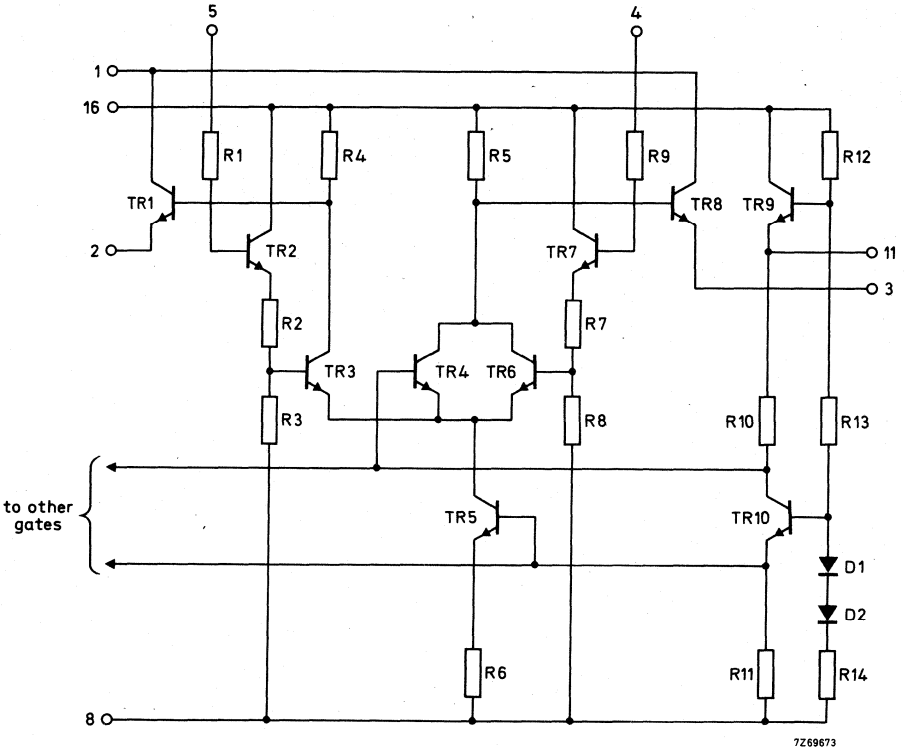
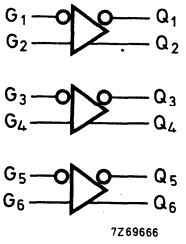


Fig. 3 Circuit diagram (one gate).



With inputs G_2, G_4 and G_6 connected to V_{BB} (pin 11)

$Q_1 = G_1$
$Q_2 = \overline{G_1}$
$Q_3 = G_3$
$Q_4 = \overline{G_3}$
$Q_5 = G_5$
$Q_6 = \overline{G_5}$

Positive logic:
H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0

Fig. 4 Logic function.

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground; $V_{EE} = -5{,}2$ V.

	symbol		T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Input current	I_{IH}	max.	70	45	45	μA	For pins 4,9,12 $V_i = V_{IHA}$
Supply current	I_{EE}	max.	39	35	39	mA	For pins 5,10,13 $V_i = V_{ILB}$
Input current	I_{CBO}	max.	1,5	1,0	1,0	μA	Test one input at a time $V_i = V_{EE}$
Reference voltage	V_{BB}	min.	−1420	−1350	−1295	mV	one input from each gate tied to V_{BB}
		max.	−1280	−1230	−1150	mV	

TEST PARAMETERS

To meet V_{OH} and V_{OL} specificications $V_i = V_{IHH}$ or V_{IHL} to one input of each gate under test and V_{ILH} or V_{ILL}, respectively to the other input of each gate.

symbol	T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
V_{IHH}	+110	+190	+300	mV	shifted +1 V
V_{IHA}	−890	−810	−700	mV	
V_{IHL}	−1890	−1810	−1700	mV	shifted −1 V
V_{IHB}	−1205	−1105	−1035	mV	
V_{ILA}	−1500	−1475	−1440	mV	
V_{ILH}	−890	−850	−825	mV	shifted +1 V
V_{ILB}	−1890	−1850	−1825	mV	
V_{ILL}	−2890	−2850	−2825	mV	shifted −1 V

$V_{IHH} = V_{IHA}$ shifted *positive* one volt for CMR tests.

$V_{IHL} = V_{IHA}$ shifted *negative* one volt for CMR tests.

$V_{ILH} = V_{ILB}$ shifted *positive* one volt for CMR tests.

$V_{ILL} = V_{ILB}$ shifted *negative* one volt for CMR tests.

* CMR = Common Mode Rejection.

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2$ V; $V_{EE} = -3{,}2$ V.

	symbol		T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Rise propagation delay time	t_{PLH}	min.	1,0	1,0	0,9	ns	For single-ended input testing one input from each gate must be tied to V_{BB}.
		max.	4,4	4,0	4,3	ns	
Fall propagation delay time	t_{PHL}	min.	1,0	1,0	0,9	ns	
		max.	4,4	4,0	4,3	ns	
Rise time	t_{TLH}	min.	1,5	1,5	1,5	ns	between 20% and 80%
		max.	3,8	3,5	3,7	ns	
Fall time	t_{THL}	min.	1,5	1,5	1,5	ns	
		max.	3,8	3,5	3,7	ns	

QUADRUPLE LINE RECEIVER

The GXB10115 is a quadruple differential amplifier intended for use in sensing signals over long lines. The base bias supply makes the device useful in other applications where a stable reference voltage is necessary.

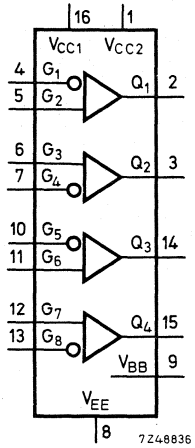


Fig. 1 Logic diagram.

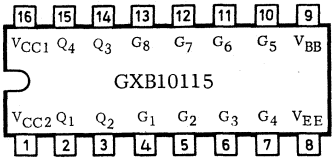


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	−5,2 ± 10	% V
Operating ambient temperature range	T_{amb}	−30 to +85	°C
Average propagation delay	t_{PLH}	typ. 2,0	ns
Output voltage			
HIGH state	V_{OH}	nom. −880	mV
LOW state	V_{OL}	nom. −1720	mV
Power consumption per package	P_{av}	typ. 95	mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see Package Outlines)

GXB10115P: plastic 16-lead dual in-line (SOT-38).
GXB10115D: ceramic 16-lead dual in-line (SOT-74).

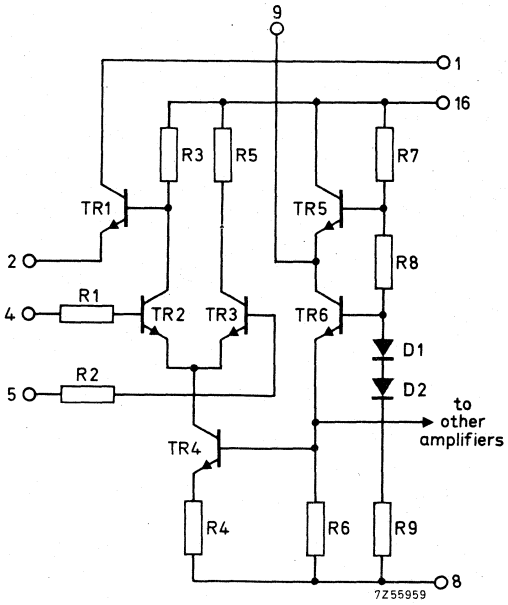


Fig. 3 Circuit diagram (one amplifier).

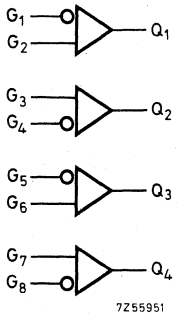


Fig. 4 Logic function.

With inputs G_2, G_3, G_6, G_7 connected to V_{BB}.

$Q_1 = \overline{G_1}$ $\quad Q_3 = \overline{G_5}$

$Q_2 = \overline{G_4}$ $\quad Q_4 = \overline{G_8}$

Positive logic: HIGH state = 1
LOW state = 0

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = −5,2 V.

	symbol		T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Input current HIGH	I_{IH}	max.	150	95	95	μA	V_{IHA}
	I_{CBO}	max.	1,5	1,0	1,0	μA	V_{ILB}
Supply current	I_{EE}	max.	29	26	29	mA	
Reference voltage	V_{BB}	min.	−1280	−1350	−1295	V	
		max.	−1420	−1230	−1150	V	

A.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = −5,2 V.

	symbol		T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Rise propagation delay time	t_{PLH}	min.	1,0	1,0	1,0	ns	
		max.	3,1	2,9	3,3	ns	
Fall propagation delay time	t_{PHL}	min.	1,0	1,0	1,0	ns	
		max.	3,1	2,9	3,3	ns	
Rise time	t_{TLH}	min.	1,1	1,1	1,1	ns	between 20% and 80%
		max.	3,6	3,3	3,7	ns	
Fall time	t_{THL}	max.	1,1	1,1	1,1	ns	
		min.	3,6	3,3	3,7	ns	

For **switching times test circuit** and **waveforms** see Family Specifications.

TRIPLE LINE RECEIVER

The GXB10116 is a triple line receiver with low impedance emitter follower complementary outputs. With translated emitter follower inputs and an active current source, it features a common mode rejection peak voltage of ±1 V. Intended primarily to receive data from balanced twisted-pair lines, this device is also suitable for minicomputers, testing and instrumentation. It can also be used as a sense amplifier for MOS RAMs as a MOS-to-ECL interface circuit; as a high speed comparator and, having an internal reference supply voltage (V_{BB}), it can operate as a Schmitt trigger.

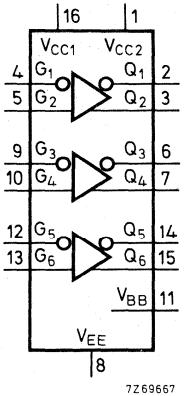


Fig. 1 Logic diagram.

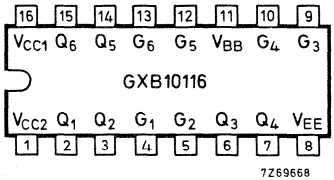


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = 5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 ± 10 % V
Operating ambient temperature range	T_{amb}		−30 to +85 °C
Average propagation delay			
single-ended input	t_{PLH}	typ.	2,4 ns
differential input	t_{PLH}	typ.	2,0 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package	P_{av}	typ.	85 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (see Package Outlines)

GXB10116P: plastic 16-lead dual in-line (SOT-38).
GXB10116D: ceramic 16-lead dual in-line (SOT-74).

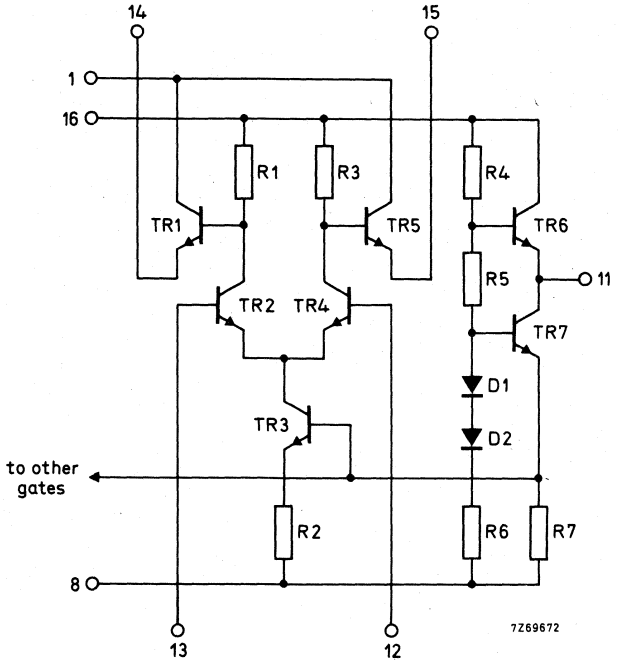


Fig. 3 Circuit diagram (one amplifier).

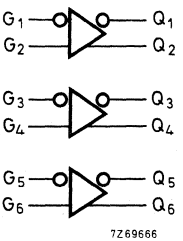


Fig. 4 Logic function.

With inputs G_2, G_4 and G_6 connected to V_{BB} (pin 11)

$Q_1 = G_1$
$Q_2 = \overline{G}_1$
$Q_3 = G_3$
$Q_4 = \overline{G}_3$
$Q_5 = G_5$
$Q_6 = \overline{G}_5$

Positive logic:

H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground: $V_{EE} = -5{,}2$ V.

	symbol		T_{amb} (°C) −30	+25	+85	unit	remarks
Input currents	I_{IH}	max.	150	95	95	μA	V_{IHA}
	I_{CBO}	max.	1,5	1,0	1,0	μA	V_{ILB}
Supply current	I_{EE}	max.	23	21	23	mA	
Reference voltage	V_{BB}	min.	−1420	−1350	−1295	V	
		max.	−1280	−1230	−1150	V	

A.C, CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2$ V; $V_{EE} = -3{,}2$ V.

	symbol		T_{amb} (°C) −−30	+25	+85	unit	remarks
Rise propagation delay time	t_{PLH}	min.	1,0	1,0	1,0	ns	
		max.	3,1	2,9	3,3	ns	
Fall propagation delay time	t_{PHL}	min.	1,0	1,0	1,0	ns	
		max.	3,1	2,9	3,3	ns	
Rise time	t_{TLH}	min.	1,1	1,1	1,1	ns	between 20% and 80%
		max.	3,6	3,3	3,7	ns	
Fall time	t_{THL}	min.	1,1	1,1	1,1	ns	
		max.	3,6	3,3	3,7	ns	

For **switching time test circuit** and **waveforms** see Family Specifications.

DUAL OR-AND/OR-AND-INVERT GATE

The GXB10117 is a dual 2-wide 2-3 input OR-AND/OR-AND-INVERT gate designed for use in data control as a general purpose logic element.

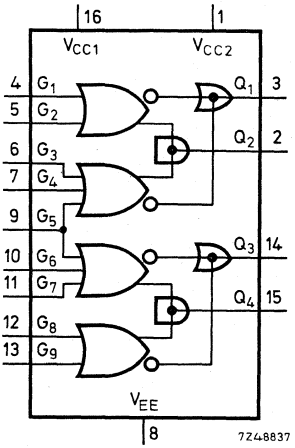


Fig. 1 Logic diagram.

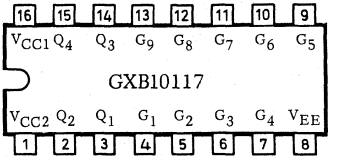


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 ± 10 % V
Operating ambient temperature range	T_{amb}		−30 to +85 °C
Average propagation delay	t_{PLH}	typ.	2,3 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package	P_{av}	typ.	100 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (see Package Outlines).

GXB10117P: plastic 16-lead dual in-line (SOT-38).
GXB10117D: ceramic 16-lead dual in-line (SOT-74).

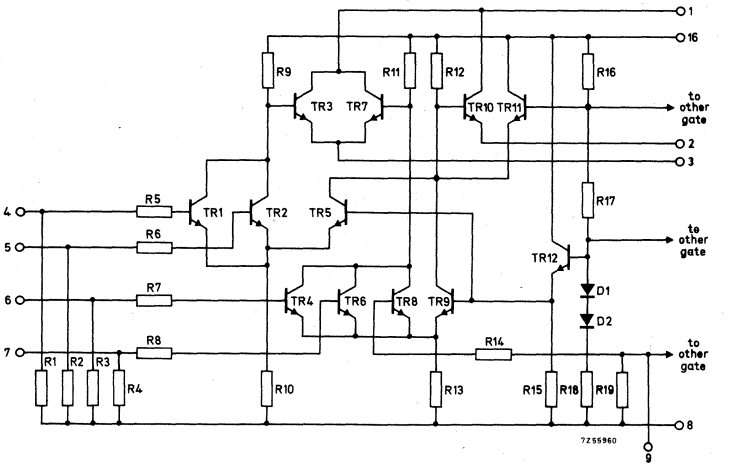


Fig. 3 Circuit diagram.

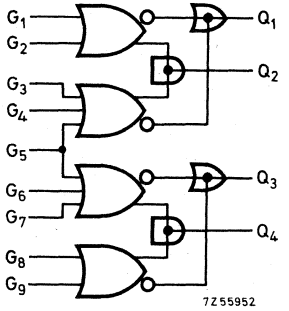


Fig. 4 Logic function.

$$Q_1 = \overline{(G_1 + G_2) \cdot (G_3 + G_4 + G_5)}$$
$$Q_2 = (G_1 + G_2) \cdot (G_3 + G_4 + G_5)$$
$$Q_3 = \overline{(G_8 + G_9) \cdot (G_5 + G_6 + G_7)}$$
$$Q_4 = (G_8 + G_9) \cdot (G_5 + G_6 + G_7)$$

Positive logic: HIGH state = 1
LOW state = 0

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = −5,2 V

	symbol		T_{amb} (°C) −30	+25	+85	unit	remarks
Input current HIGH	I_{IH}	max.	390	245	245	μA	pin 4,5,12,13
	I_{IH}	max.	425	265	265	μA	pin 6,7,10,11
	I_{IH}	max.	560	350	350	μA	pin 9
Input current LOW	I_{IL}	min.	0,5	0,5	0,3	μA	
Supply current	I_{EE}	max.	29	26	29	mA	

A.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = −5,2 V.

	symbol		T_{amb} (°C) −30	+25	+85	unit	remarks
Rise propagation delay time	t_{PLH}	min.	1,4	1,4	1,4	ns	
		max.	3,9	3,4	3,8	ns	
Fall propagation delay time	t_{PHL}	min.	1,4	1,4	1,4	ns	
		max.	3,9	3,4	3,8	ns	
Rise time	t_{TLH}	min.	0,9	1,1	1,1	ns	between 20% and 80%
		max.	4,1	4,0	4,6	ns	
Fall time	t_{THL}	min.	0,9	1,1	1,1	ns	between 20% and 80%
		max.	4,1	4,0	4,6	ns	

For **switching times test circuit** and **waveforms** see Family Specifications.

DUAL OR-AND GATE

The GXB10118 is a dual 2-wide 3-input OR-AND gate designed for use in data control as a general purpose logic element.

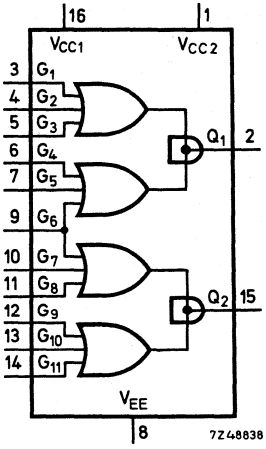


Fig. 1 Logic diagram.

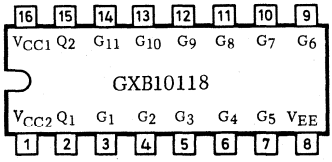


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 ± 10 % V
Operating ambient temperature range	T_{amb}		−30 to +85 °C
Average propagation delay	t_{PLH}	typ.	2,3 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package	P_{av}	typ.	100 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (see Package Outlines).

GXB10118P: plastic 16-lead dual in-line (SOT-38).
GXB10118D: ceramic 16-lead dual in-line (SOT-74).

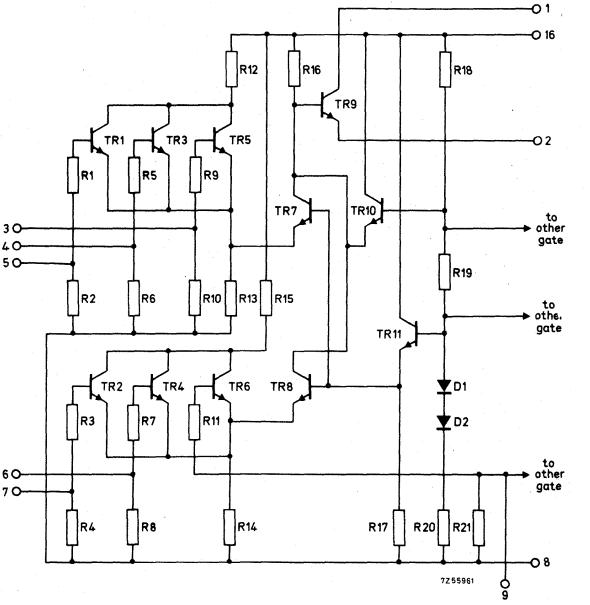


Fig. 3 Circuit diagram (one gate).

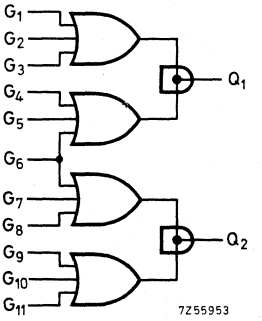


Fig. 4 Logic function.

$Q_1 = (G_1 + G_2 + G_3) \cdot (G_4 + G_5 + G_6)$

$Q_2 = (G_6 + G_7 + G_8) \cdot (G_9 + G_{10} + G_{11})$

Positive logic: HIGH state = 1
LOW state = 0

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = −5,2 V.

	symbol		T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Input current HIGH	I_{IH}	max.	390	245	245	μA	pins 3,4,5,12,13,14
	I_{IH}	max.	425	265	265	μA	pins 6,7,10,11
	I_{IH}	max.	560	350	350	μA	pin 9
Input current LOW	I_{IL}	min.	0,5	0,5	0,3	μA	
Supply current	I_{EE}	max.	29	26	29	mA	
Output voltage LOW	V_{OLA}		−1675	−1650	−1615	mV	
	V_{OLB}		−2000	−1990	−1920	mV	

A.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = −5,2 V

	symbol		T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Rise propagation delay time	t_{PLH}	min.	1,4	1,4	1,4	ns	
		max.	3,9	3,4	3,8	ns	
Fall propagation delay time	t_{PHL}	min.	1,4	1,4	1,4	ns	
		max.	3,9	3,4	3,8	ns	
Rise time	t_{TLH}	min.	0,8	1,1	1,1	ns	between 20% and 80%
		max.	4,1	4,0	4,6	ns	
Fall time	t_{THL}	min.	0,8	1,1	1,1	ns	
		max.	4,1	4,0	4,6	ns	

For **switching times test circuit** and **waveforms** see Family Specifications.

OR-AND GATE

The GXB10119 is a 4-wide 4-3-3-3-input OR-AND gate designed for use in data control as a general purpose logic element.

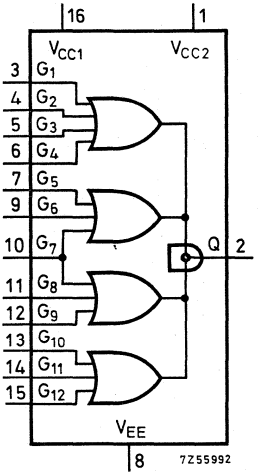


Fig. 1 Logic diagram.

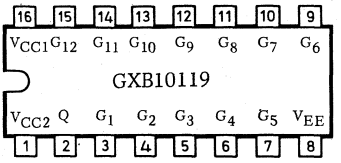


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 ± 10 % V
Operating ambient temperature range	T_{amb}		−30 to +85 °C
Average propagation delay	t_{PLH}	typ.	2,3 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package	P_{av}	typ.	100 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (see Package Outlines)

GXB10119P: plastic 16-lead dual in-line (SOT-38).
GXB10119D: ceramic 16-lead dual in-line (SOT-74).

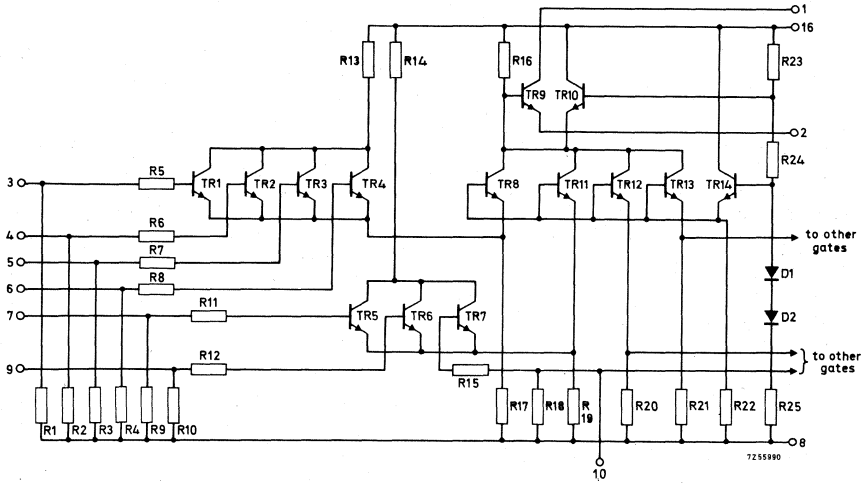


Fig. 3 Circuit diagram.

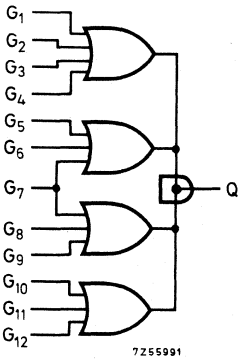


Fig. 4 Logic function.

$$Q = (G_1 + G_2 + G_3 + G_4) \cdot (G_5 + G_6 + G_7) \cdot (G_7 + G_8 + G_9) \cdot (G_{10} + G_{11} + G_{12}).$$

Positive logic: HIGH state = 1
LOW state = 0

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = −5,2 V.

	symbol		T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Input current HIGH							
pin 10	I_{IH}	max.	560	350	350	μA	
other pins	I_{IH}	max.	390	245	245	μA	
Input current LOW	I_{IL}	min.	0,5	0,5	0,3	μA	
Supply current	I_{EE}	max.	29	26	29	mA	
Output voltage LOW	V_{OLB}		−2000	−1990	−1920	mV	

A.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = −5,2 V.

	symbol		T_{amb} (°C) −35	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Rise propagation delay time	t_{PLH}	min.	1,4	1,4	1,4	ns	
		max.	3,9	3,4	3,8	ns	
Fall propagation delay time	t_{PHL}	min.	1,4	1,4	1,4	ns	
		max.	3,9	3,4	3,8	ns	
Rise time	t_{TLH}	min.	0,8	1,5	1,5	ns	between 20% and 80%
		max.	4,1	4,0	4,6	ns	
Fall time	t_{THL}	min.	0,8	1,5	1,5	ns	
		max.	4,1	4,0	4,6	ns	

For **switching times test circuit** and **waveforms** see Family Specifications.

4-WIDE OR-AND/OR-AND-INVERT GATE

The GXB10121 is a 4-wide OR-AND/OR-AND-INVERT gate designed for use in data control as a general purpose logic element. Input pull-down resistors (50 kΩ) allow unused inputs to be left open.

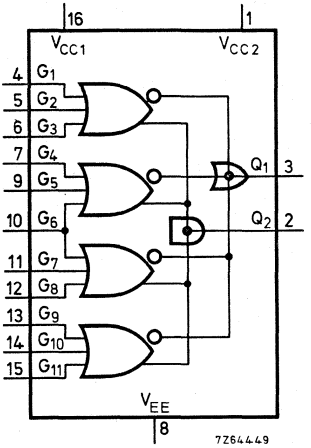


Fig. 1 Logic diagram.

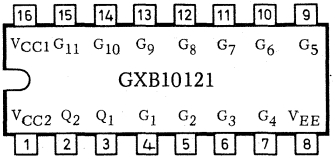


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	−5,2 ± 10%	V
Operating ambient temperature range	T_{amb}	−30 to + 85	°C
Average propagation delay	t_{PLH}	typ. 2,3	ns
Output voltage			
HIGH state	V_{OH}	nom. −880	mv
LOW state	V_{OL}	nom. −1720	mV
Power consumption per package	P_{av}	100	mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see Package Outlines)

GXB10121P : plastic 16-lead dual in-line (SOT-38).
GXB10121D: ceramic 16-lead dual in-line (SOT-74).

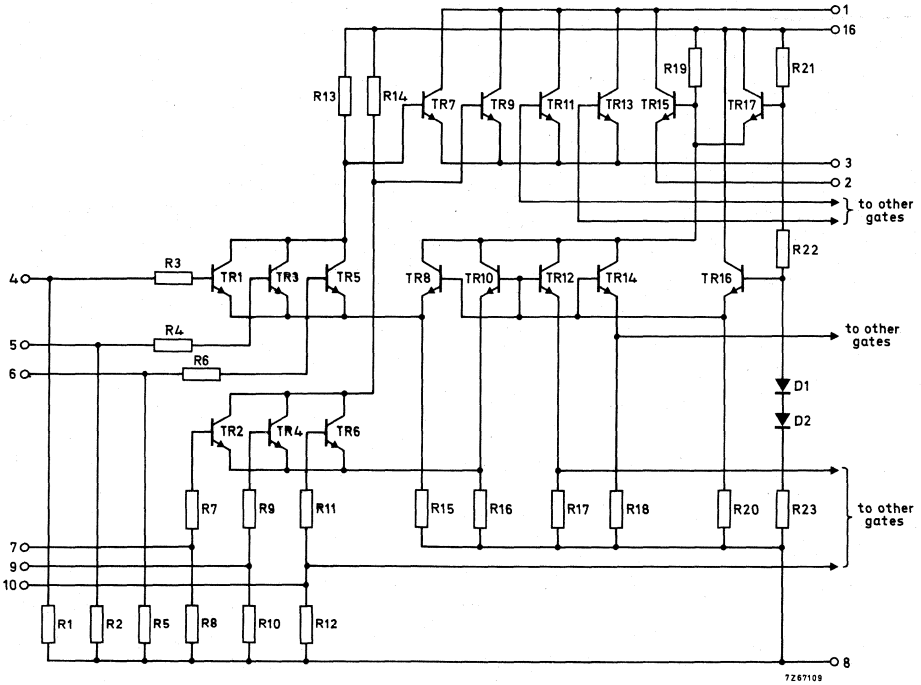
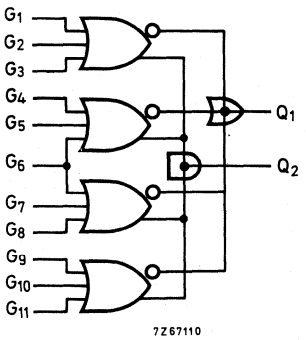


Fig. 3 Circuit diagram.



$$Q_1 = \overline{G_1 + G_2 + G_3} + \overline{G_4 + G_5 + G_6} + \overline{G_6 + G_7 + G_8} + \overline{G_9 + G_{10} + G_{11}}$$

$$Q_2 = \overline{Q_1}$$

positive logic: HIGH state = 1
LOW state = 0

Fig. 4 Logic function.

RATINGS see Family Specifications

D.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = −5,2 V.

	symbol		T_{amb} (°C) −30	+ 25	+ 85	unit	remarks
Output voltage HIGH maximum	V_{OHA}		780	700	590	mV	
Output voltage LOW minimum	V_{OLB}		2000	1990	1920	mV	
Input current HIGH							
pin 10	I_{IH}	max.	560	350	350	μA	
other pins	I_{IH}	max.	390	245	245	μA	
Input current LOW	I_{IL}	min.	0,5	0,5	0,3	μA	
Supply current	I_{EE}	max.	29	26	29	mA	

A.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = −5,2 V.

	symbol		T_{amb} (°C) −30	+ 25	+ 85	unit	remarks
Rise propagation delay times	t_{PLH}	min.	1,4	1,4	1,4	ns	
		max.	3,9	3,4	3,8	ns	
Fall propagation delay times	t_{PHL}	min.	1,4	1,4	1,4	ns	
		max.	3,9	3,4	3,8	ns	
Rise time	t_{TLH}	min.	0,9	1,1	1,1	ns	between 20% and 80%
		max.	4,1	4,0	4,6	ns	
Fall time	t_{THL}	min.	0,9	1,1	1,1	ns	
		max.	4,1	4,0	4,6	ns	

For **switching times test circuit** and **waveforms** see Family Specifications.

TRIPLE NOR GATE

The GXB10123 consists of three NOR gates for use as a driver. It can drive a bus with a characteristic impedance of not less than 25 Ohms. When the output is LOW it presents a high impedance to the bus so that its characteristic impedance is not reduced.

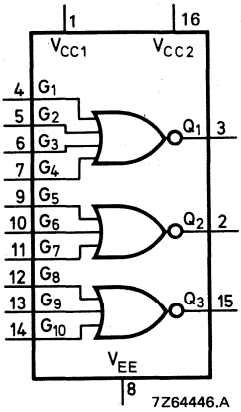


Fig. 1 Logic diagram.

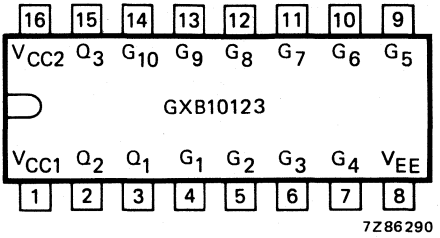


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0V$ (ground);
$V_{EE} = -5,2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	$-5,2 \pm 10\%$	V
Operating ambient temperature	T_{amb}	-30 to $+85$	°C
Average propagation delay	t_{PLH}/t_{PHL}	typ. 3,0	ns
Power consumption per package (no load)	P_{av}	typ. 310	mW

FAMILY DATA
RATINGS
see Family Specifications.

PACKAGE OUTLINES (see Package Outlines)

GXB10123P : plastic 16-lead dual in-line (SOT-38).
GXB10123D: ceramic 16-lead dual in-line (SOT-74).

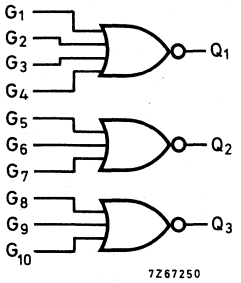


Fig. 3 Logic functions.

$Q_1 = \overline{G_1 + G_2 + G_3 + G_4}$

$Q_2 = \overline{G_5 + G_6 + G_7}$

$Q_3 = \overline{G_8 + G_9 + G_{10}}$

positive logic: HIGH state = 1
(the more positive voltage)
LOW state = 0
(the more negative voltage)

D.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = – 5,2 V.

	symbol		T_{amb} (°C) –30	+ 25	+ 85	unit	remarks
Input current HIGH	I_{IH}	max.	350	220	220	μA	
Input current LOW	I_{IL}	min.	0,5	0,5	0,3	μA	
Supply current	I_{EE}	max.	82	75	82	mA	
Output voltage LOW	V_{OLB}		–2100	–2100	–2100	mV	R_L = 25 Ω to –2,1 V
	V_{OLA}		–2030	–2030	–2030	mV	
threshold	V_{OLC}		–2010	–2010	–2010	mV	
Output voltage HIGH	V_{OHA}		–890	–810	–700	mV	R_L = 25 Ω to –2,0 V
	V_{OHB}		–1060	–960	–890	mV	
threshold	V_{OHC}		–1080	–980	–910	mV	

A.C. CHARACTERISTICS

V_{CC} = + 2,0 V; V_{EE} = –3,2 V; R_L = 25 Ω to –2,1 V.

	symbol		T_{amb} (°C) –30	+ 25	+ 85	unit	remarks
Propagation delay rise and fall time	t_{PLH}	min.	1,2	1,2	1,2	ns	
	t_{PHL}	max.	4,6	4,4	4,8	ns	
Transition rise and fall time	t_{THL}	min.	1,0	1,0	1,0	ns	between 20% and 80%
	t_{TLH}	max.	3,7	3,5	3,9	ns	

For **switching times test circuit** and **waveforms** see Family Specifications.

TTL-TO-ECL TRANSISTOR

The GXB10124 is a quadruple TTL-to-ECL transistor with individual and common TTL-compatible inputs on each gate. When the common input is in the LOW state, all ECL direct outputs are in a LOW state and inverting outputs in a HIGH state.

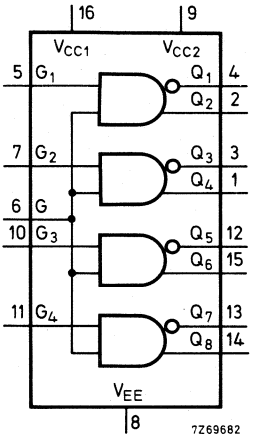


Fig. 1 Logic diagram.

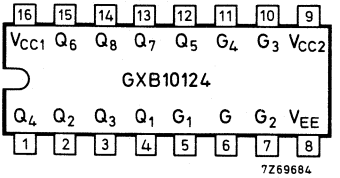


Fig. 2 Pin designation.

V_{CC1} = 0 V (ground);
V_{CC2} = +5 V;
V_{EE} = −5,2 V.

QUICK REFERENCE DATA

Supply voltages	V_{EE}		−5,2 ± 10 % V
	V_{CC2}		+5,0 ± 10 % V
Operating ambient temperature range	T_{amb}		−30 to +85 °C
Average propagation delay	t_{PLH}	typ.	3,5 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package	P_{av}	typ.	380 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (see Package Outlines)

GXB10124P: plastic 16-lead dual in-line (SOT-38).
GXB10124D: ceramic 16-lead dual in-line (SOT-74).

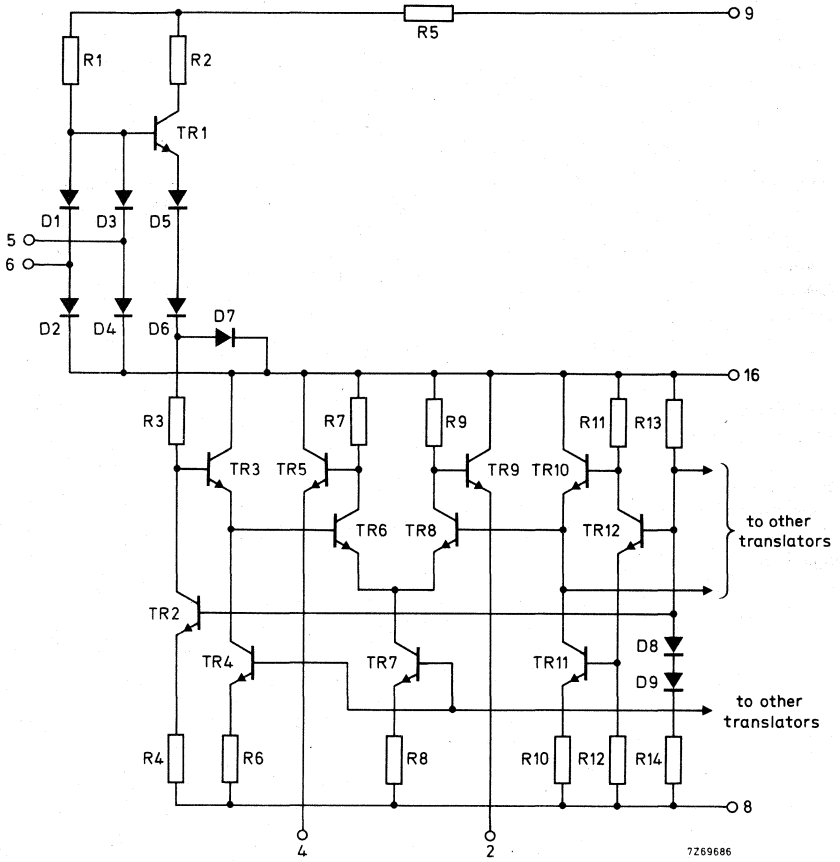


Fig. 3 Circuit diagram.

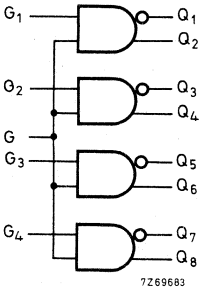


Fig. 4 Logic function.

$Q_1 = \overline{G_1 \cdot G}$ $\quad Q_5 = \overline{G_3 \cdot G}$

$Q_2 = G_1 \cdot G$ $\quad Q_6 = G_3 \cdot G$

$Q_3 = \overline{G_2 \cdot G}$ $\quad Q_7 = \overline{G_4 \cdot G}$

$Q_4 = G_2 \cdot G$ $\quad Q_8 = G_4 \cdot G$

Positive logic

H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0.

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{CC1} = ground; V_{CC2} = +5,0 V; V_{EE} = −5,2 V.

	symbol	T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Input voltage						
HIGH max.	V_{IHA}	4,0	4,0	4,0	V	
HIGH min.	V_{IHB}	2,0	1,8	1,8	V	
Input voltage						
LOW min.	V_{ILB}	0,4	0,4	0,4	V	
LOW max.	V_{ILA}	1,1	1,1	0,8	V	
Reverse voltage	V_R	2,4	2,4	2,4	V	
	V_{RH}	4,0	4,0	4,0	V	
Supply current	I_{EE} max.	72	66	72	mA	
	I_{CCH} max.	16	16	18	mA	$V_I = V_{RH}$ (all inputs)
	I_{CCL}	25	25	25	mA	V_I strobe = V_{ILB}
Reverse current strobe input	I_{SR}	200	200	200	μA	$V_I = V_R$ (strobe) V_{ILB} single inputs)
single inputs	I_{IR}	50	50	50	μA	$V_I = V_{ILB}$ (strobe) V_R (P.U.T.)
Forward current strobe input	I_{SF}	−12,8	−12,8	−12,8	mA	$V_I = V_{ILB}$ (strobe) V_R (single inputs)
single inputs	I_{IF}	−3,2	−3,2	−3,2	mA	$V_I = V_R$ (strobe) V_{ILB} (P.U.T.)
Input breakdown voltage	$V_{I(BR)}$ min.	5,5	5,5	5,5	V	I_I strobe = 1 mA $V_I = V_{ILB}$ while testing single inputs
Input clamping voltage	$V_{I(CL)}$ max.	−1,5	−1,5	−1,5	V	test one input at a time.

A.C. CHARACTERISTICS

V_{CC1} = +2 V; V_{CC2} = +7 V; V_{EE} = −32 V.

	symbol		T_{amb} (°C) −35	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Rise propagation delay time	t_{PLH}	min.	1,0	1,0	1,0	ns	V_I (+1,5 V) to V_O (50%)
		max.	6,8	6,0	6,8	ns	
Fall propagation delay time	t_{PHL}	min.	1,0	1,0	1,0	ns	
		max.	6,8	6,0	6,8	ns	
Rise time	t_{TLH}	min.	1,0	1,1	1,1	ns	between 20% and 80%
		max.	4,2	3,9	4,3	ns	
Fall time	t_{THL}	min.	1,0	1,1	1,1	ns	
		max.	4,2	3,9	4,3	ns	

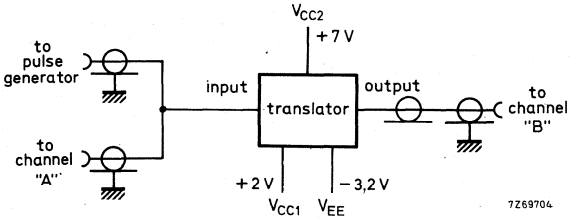


Fig. 5 Switching times test circuit.

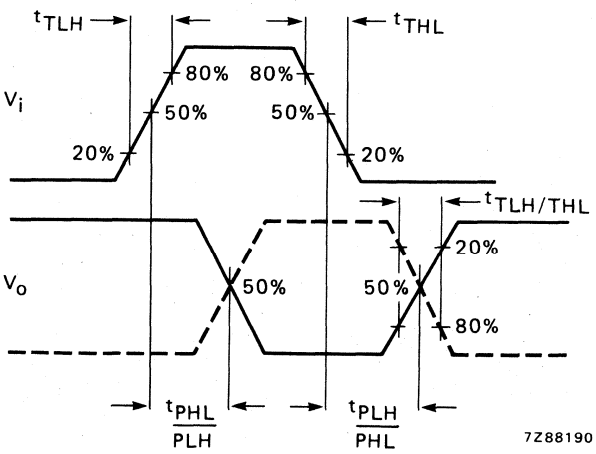


Fig.6 Switching times waveforms.

V_{IH} = +5,5 V; V_{IL} = 2,0 V.

ECL-to-TTL TRANSLATOR

The GXB10125 is a quadruple ECL-to-TTL translator for interfacing data between two different logic systems. It provides also a separate reference voltage (V_{BB}) to be used in case of single ended input biasing. Input and output levels are respectively ECL10 000 and TTL Schottky.

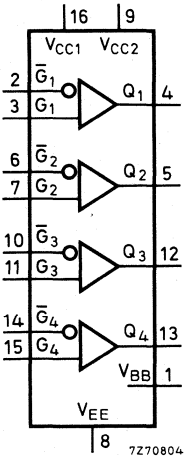


Fig. 1 Logic diagram.

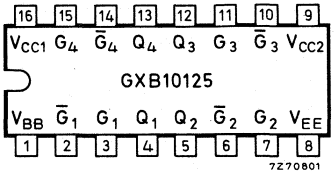


Fig. 2 Pin designation.

V_{CC1} = 0 V (ground);
V_{CC2} = + 5 V;
V_{EE} = −5,2 V.

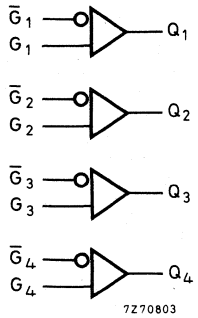
QUICK REFERENCE DATA

Supply voltages	V_{EE}		−5,2 ± 10% V
	V_{CC2}		+ 5,0 V
Operating ambient temperature range	T_{amb}		−30 to + 85 °C
Average propagation delay	t_{PLH}	typ.	4,5 ns
Output voltage			
HIGH state	V_{OH}	nom.	3,5 V
LOW state	V_{OL}	nom.	0,3 V
Power consumption per package	P_{av}	typ.	380 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (see Package Outlines)

GXB10125P : plastic 16-lead dual in-line (SOT-38).
GXB10125D: ceramic 16-lead dual in-line (SOT-74).



$Q_1 = G_1$
$Q_2 = G_2$
$Q_3 = G_3$
$Q_4 = G_4$

Positive logic
H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0

Fig. 3 Logic function.

RATINGS see Family Specifications

TEST PARAMETERS

To meet V_{OH} and V_{OL} specifications $V_i = V_{IHH}$ or V_{IHL} to one input of each gate under test and V_{ILH} or V_{ILL}, respectively to the other input of each gate.

symbol	T_{amb} (°C) −30	+ 25	+ 85	unit	remarks
V_{IHH}	+ 110	+ 190	+ 300	mV	shifted + 1 V
V_{IHA}	−890	−810	−700	mV	
V_{IHL}	−1890	−1810	−1700	mV	shifted −1 V
V_{IHB}	−1205	−1105	−1035	mV	
V_{ILA}	−1500	−1475	−1440	mV	
V_{ILH}	−890	−850	−825	mV	shifted + 1 V
V_{ILB}	−1890	−1850	−1825	mV	
V_{ILL}	−2890	−2850	−2825	mV	shifted −1 V

$V_{IHH} = V_{IHA}$ shifted *positive* one volt for CMR tests.
$V_{IHL} = V_{IHA}$ shifted *negative* one volt for CMR tests.
$V_{ILH} = V_{ILB}$ shifted *positive* one volt for CMR tests.
$V_{ILL} = V_{ILB}$ shifted *negative* one volt for CMR tests.

* CMR = Common Mode Rejection.

D.C. CHARACTERISTICS

V_{CC1} = 0 V (ground); V_{EE} = −5,2 V; V_{CC2} = + 5 V

	symbol		T_{amb} (°C) −30	+ 25	+ 85	unit	remarks
Input current	I_{IH}	max.	180	115	115	μA	$V_i = V_{IHA}$*
Input current	I_{CBO}	max.	1,5	1,0	1,0	μA	$V_i = V_{EE}$*
Supply current	I_{EE}	max.	44	40	44	mA	For pins 3,7,11,15 $V_i = V_{BB}$ For pins 2,6,10,14 $V_i = V_{EE}$
Supply current	I_{CCH}	max.	52	52	52	mA	For pins 3,7,11,15 $V_i = V_{BB}$ For pins 2,6,10,14 $V_i = V_{IHA}$
	I_{CCL}	max.	39	39	39	mA	For pins 3,7,11,15 $V_i = V_{BB}$ For pins 2,6,10,14 $V_i = V_{EE}$
Short-circuit output current	I_{OS}	min.	40	40	40	mA	For pins 3,7,11,15 $V_i = V_{BB}$
		max.	100	100	100	mA	For pins 2,6,10,14 $V_i = V_{ILB}$ Connect outputs to ground, one at a time.
Output voltage HIGH min.	V_{OHB}		2,5	2,5	2,5	V	Pins 2,6,10,14 $V_i = V_{ILB}$ Pins 3,7,11,15 $V_i = V_{IHA}$
Output voltage LOW max.	V_{OLA}		0,5	0,5	0,5	V	Pins 2,6,10,14 $V_i = V_{IHA}$ Pins 3,7,11,15 $V_i = V_{ILB}$
Threshold voltage HIGH	V_{OHC}		2,5	2,5	2,5	V	Pins 2,6,10,14 $V_i = V_{ILA}$ (one input at a time); Pins 3,7,11,15 $V_i = V_{BB}$
Threshold voltage LOW	V_{OLC}		0,5	0,5	0,5	V	Pins 2,6,10,14 $V_i = V_{IHB}$ (one input at a time); Pins 3,7,11,15 $V_i = V_{BB}$
Indeterminate input protection	V_{OLS1}	max.	0,5	0,5	0,5	V	to both inputs of a gate one at a time $V_i = V_{EE}$
	V_{OLS2}	max.	0,5	0,5	0,5	V	all inputs open
Reference voltage	V_{BB}	min.	−1280	−1230	−1150	mV	One input of each gate connected to V_{BB} (pin 1)
		max.	−1420	−1350	−1295	mV	
Common mode rejection tests	V_{OHB}		2,5	2,5	2,5	V	$V_i = V_{IHH}$ or V_{IHL} to one input of each gate under test and $V_i = V_{ILH}$ or V_{ILL} respectively to the other input of each gate.
	V_{OLA}		0,5	0,5	0,5	V	

* One input of each gate connected to V_{BB}. The other inputs tested one at a time.

A.C. CHARACTERISTICS

V_{CC1} = 0 V (ground); V_{EE} = −5,2 V; V_{CC2} = + 5 V.

	symbol		T_{amb} (°C) −30	+ 25	+ 85	unit	conditions
Rise propagation delay time	t_{PLH}	min.	1,0	1,0	1,0	ns	V_i 50% to V_o = 1,5 V For single-ended input testing, one input from each gate must be tied to V_{BB} (pin 1).
		max.	6,0	6,0	6,0	ns	
Fall propagation delay time	t_{PHL}	min.	1,0	1,0	1,0	ns	
		max.	6,0	6,0	6,0	ns	
Rise time	t_{TLH}	max.	3,3	3,3	3,3	ns	(+ 1 V to + 2 V)
Fall time	t_{THL}	max.	3,3	3,3	3,3	ns	

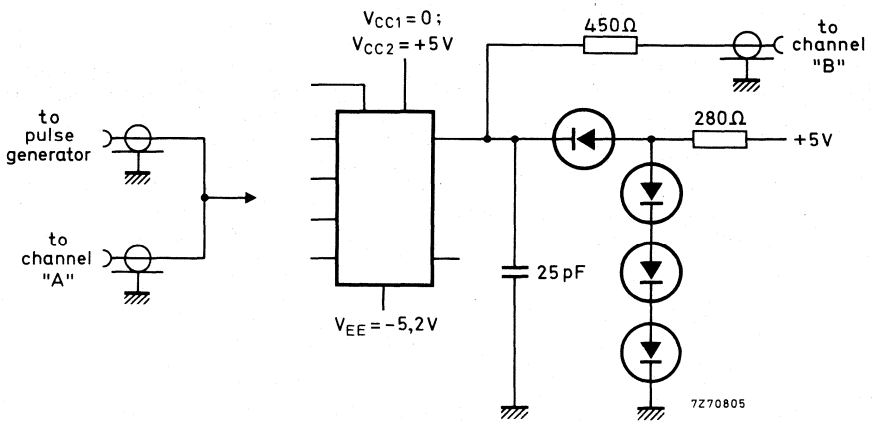


Fig. 4 Switching times test circuit.

QUADRUPLE TTL/IBM BUS RECEIVER/LATCH

The GXB10129, associated with the GXB10128, is intended to allow interfacing of GX family types with other logic devices or systems. All inputs, data, clock, reset and strobe, are compatible with GX family logic levels whereas data inputs accept TTL logic levels and levels compatible with IBM-type busses. The information received from the bus is stored temporarily in latch storage elements.

The strobe input is useful to provide accurate synchronization of signals and/or connection to GX family type level busses. When the clock is LOW, the reset input is disabled and the inputs will follow the data inputs. The latches are capable of storing the data on the rising edge of the clock. Unused data inputs must be tied to V_{CC2} or ground. On the other hand, clock, strobe and reset inputs may be left open if not used due to 50 kΩ pull-down resistors to V_{EE}.

The outputs are enabled when the strobe input is HIGH. Two modes of operation are provided. In the first mode, obtained by tying the hysteresis control input to V_{EE}, the input threshold points of the D inputs are fixed. In the second mode this hysteresis control input is connected to ground which gives an hysteresis input effect (see test table) useful for increasing the D input noise margin.

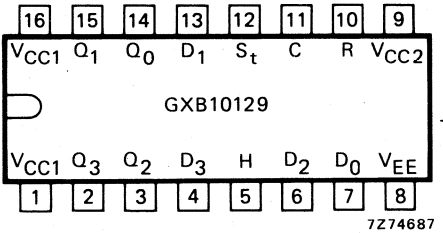


Fig. 1 Pin designation.

QUICK REFERENCE DATA

Supply voltages	V_{EE}		−5,2 ± 10% V
	V_{CC2}		+ 5,0 V
Operating ambient temperature range	T_{amb}		−30 to + 85 °C
Average propagation delay	t_{PLH}	typ.	10 ns
Output voltage HIGH state	V_{OH}	nom.	−880 mV
Output voltage LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_{av}	typ.	750 mW

FAMILY DATA see Family Sepcifications

PACKAGE OUTLINES (see Package Outlines)

GXB10129P: 16-lead DIL; plastic (SOT-38Z).
GXB10129D: 16-lead DIL; ceramic (SOT-74).

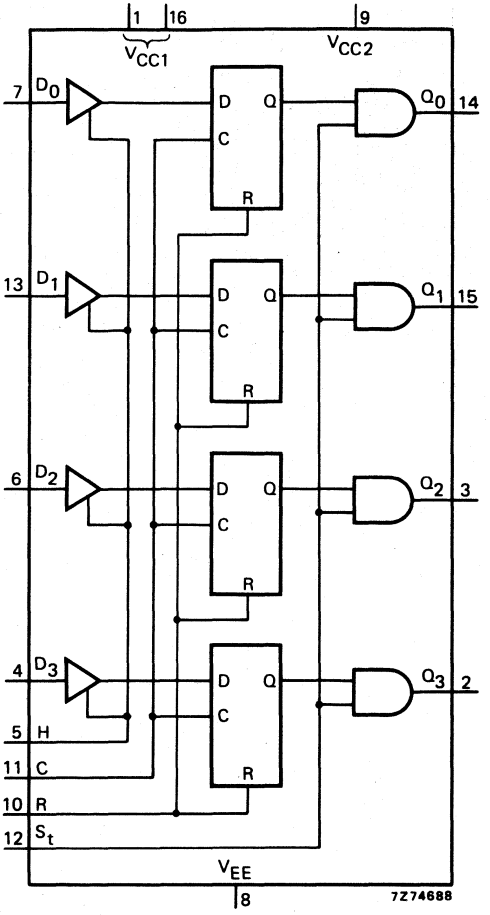


Fig. 2 Logic diagram.

D_0 to D_3	data inputs
H	hysteresis control
C	clock input
R	reset
S_t	strobe input
Q_0 to Q_3	outputs

inputs				output
D_n	C	S_t	R	$Q_n + 1$
X	X	L	X	L
X	H	X	H	L
L	L	H	X	L
X	H	H	L	Q_n
H	L	H	X	H

Positive logic:

H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0
X = state is immaterial

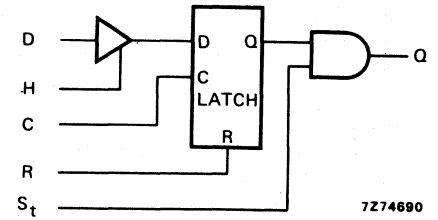


Fig. 3 Function table (one latch).

RATINGS see Family Sepcifications

TEST PARAMETERS

TTL input levels

T_{amb}	= −30	+ 25	+ 85	°C
V_{IHA}	= 3,000	3,000	3,000	V
V_{IHB}	= 2,000	2,000	2,000	V
V_{ILA}	= 0,800	0,800	0,800	V
V_{ILB}	= 0,400	0,400	0,400	V

Hysteresis mode threshold voltages

T_{amb}	= −30	+ 25	+ 85	°C	
V_{IHA}''	= 2,900	2,600	2,300	V	L → H
V_{ILA}''	= 2,000	1,700	1,400	V	L → H
V_{IHA}'''	= 2,200	1,900	1,600	V	H → L
V_{ILA}'''	= 1,300	1,000	0,700	V	H → L

V_{IHA}'', V_{ILA}'', V_{IHA}''' and V_{ILA}''' are logic "1" and "0" threshold voltages in the hysteresis mode as shown in fig. 4.

ECL input levels

T_{amb}	= −35	+ 25	+ 85	°C
V_{IHA}	= −890	−810	−700	mV
V_{IHB}	= −1205	−1105	−1035	mV
V_{ILA}	= −1500	−1475	−1440	mV
V_{ILB}	= −1890	−1850	−1825	mV

IBM input levels

T_{amb}	= −30	+ 25	+ 85	°C
V_{IHA}	= 3,11	3,110	3,11	V
V_{IHB}	= −	1,700	−	V
V_{ILA}	= −	1,100	−	V
V_{ILB}	= 0,15	0,150	0,15	V

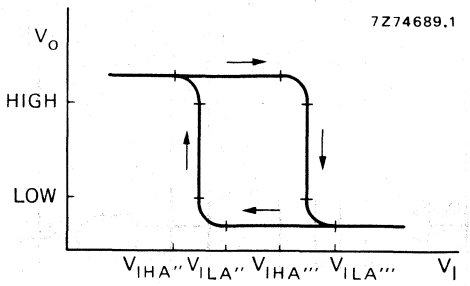


Fig. 4 Hysteresis mode threshold voltage.

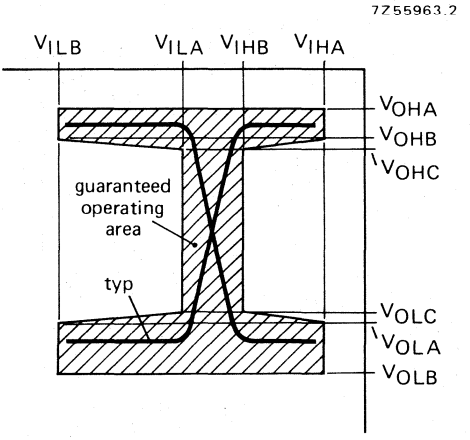


Fig. 5 Transfer characteristics.

D.C. CHARACTERISTICS

V_{CC1} = (ground); V_{EE} = −5,2 V; V_{CC2} = + 5 V.

	symbol		T_{amb} (°C) −30	+ 25	+ 85	unit	remarks
Supply current negative	I_{EE}	max.	167 189	152 172	167 189	mA mA	Pin 5 to ground* Pin 5 to V_{EE}*
Supply current positive	I_{CC}	max.	8	8	8	mA	Pin 5 to V_{EE}; V_{IL} to all data inputs
Input current data (pins 4,6,7,13)	I_{CBO}	min.	1,5	1,0	1,0	μA	Pin 5 to V_{EE} V_{IL} to data inputs one at a time
data (4,6,7,13) reset (pin 10) clock (pin 11) strobe (pin 12)	I_{IH}	max.	150 720 390 390	95 450 245 245	95 450 245 245	μA μA μA μA	pin 5 to V_{EE} V_{IH} to the pin under test, one at a time.
Input current LOW pins 10,11,12	I_{IL}	min.	0,5	0,5	0,3	μA	Pin 5 to V_{EE}; V_{IH} to all other inputs; V_{IL} to the pin under test; one at a time.

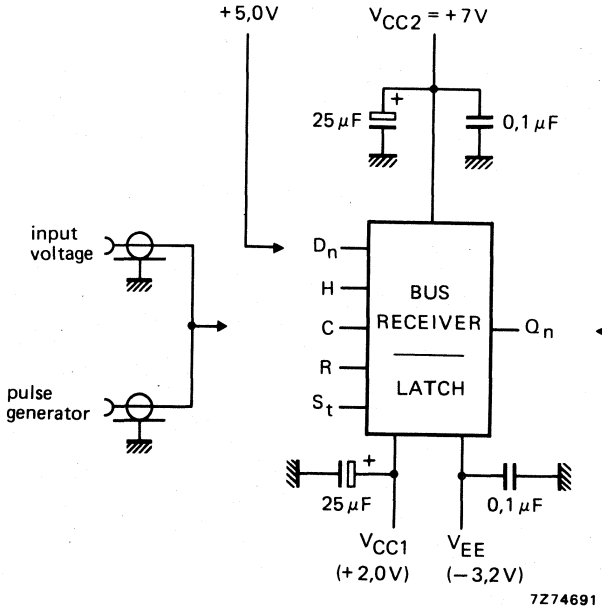


Fig. 6 Switching times test circuit.

Input pulse data:
$t_r = t_f = 5{,}5 \pm 0{,}5$ ns (10 to 90%)

Input pulse other inputs:
$t_r = t_f = 2{,}0$ ns (20 to 80%)

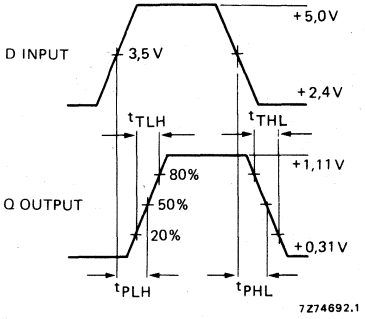
* Pin 11 to V_{IH}; pin 10 open; all other inputs to V_{IL}.

A.C. CHARACTERISTICS

V_{CC1} = + 0,2 V (ground); V_{CC2} = + 7,0 V; V_{EE} = −3,2 V

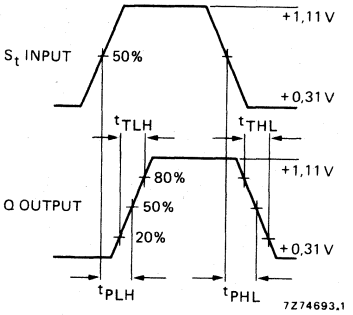
	symbol		T_{amb} (°C) −30	+ 25	+ 85	unit	remarks
Rise propagation delay time D → Q	t_{PLH}	min.	6,0	6,6	6,6	ns	Input 3,5 V to 50% output see Fig. 7
		max.	20,0	20,0	30,0	ns	
C → Q	t_{PLH}	min.	2,7	2,7	2,7	ns	50% to 50% Fig. 9
		max.	11,0	9,0	11,0	ns	
S_t → Q	t_{PLH}	min.	1,6	1,6	1,6	ns	50% to 50% Fig. 8
		max.	8,0	7,0	8,0	ns	
R → Q	t_{PLH}	min.	2,0	2,0	2,0	ns	50% to 50% Fig. 9
		max.	8,0	6,5	8,0	ns	
Fall propagation delay time D → Q	t_{PHL}	min.	3,7	3,7	3,7	ns	input 3,5 V to 50% output (Fig. 7)
		max.	15,0	15,0	40,0	ns	
Rise time	t_{TLH}	min.	1,5	1,5	1,5	ns	between 20% and 80%
		max.	5,0	4,3	5,0	ns	
Fall time	t_{THL}	min.	1,5	1,5	1,5	ns	
		max.	5,0	4,3	5,0	ns	
Set-up time D → C	t_s	min.	27	20	27	ns	between 50% (Fig. 11)
Hold time D → C	t_h	min.	0	−2	−2	ns	
Hysteresis mode							
Rise propagation delay time D → Q	t_{PLH}	min.	6,6	6,7	6,6	ns	Input 3,5 V to 50% output (Fig. 7)
		max.	30,0	25,0	30,0	ns	
Fall propagation delay time D → Q	t_{PHL}	min.	3,7	3,7	3,7	ns	Input 3,5 V to 50% output (Fig. 7)
		max.	17,0	15,0	40,0	ns	
Set-up time	t_s	min.	30,0	25,0	30,0	ns	between 50% (Fig. 11)
Hold time	t_h	min.	0	−2,0	−2,0	ns	

Switching times waveforms



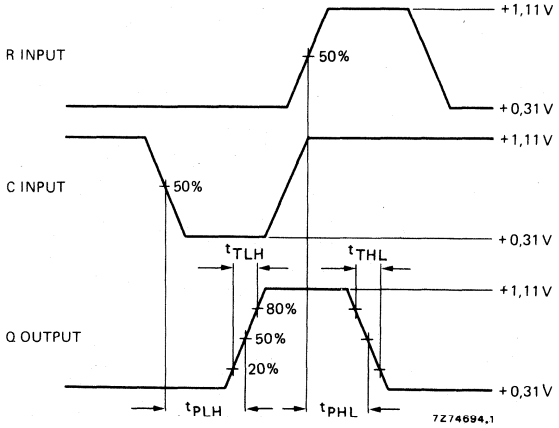
inputs		
C	R	S_t
L	L	H

Fig. 7 Data to output waveforms.



inputs		
D	C	R
H	L	L

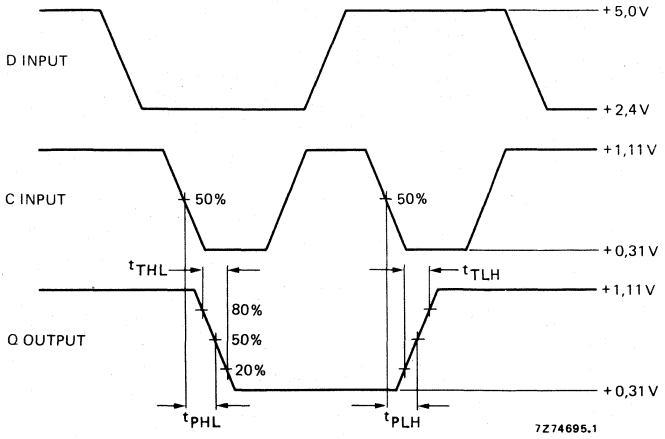
Fig. 8 Strobe to output waveforms.



inputs	
D	S_t
H	H

Fig. 9 Reset to output waveforms.

Switching times waveforms



inputs	
R	S_t
L	H

Fig. 10 Clock to output waveforms.

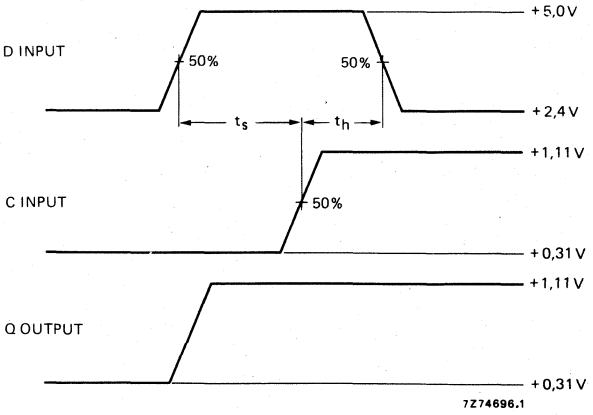


Fig. 11 Set-up and hold times waveforms.

DUAL D-TYPE LATCH

The GXB10130 is a clocked dual D-type latch. Each element can be clocked separately by holding the common clock in the LOW state and using the clock enable inputs for the clocking function. The outputs are latched when the level of the clock is high.

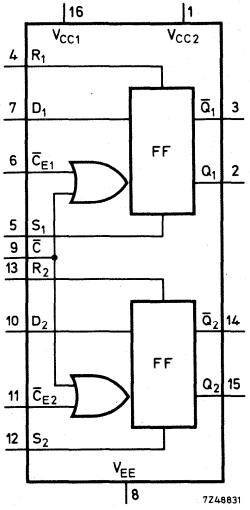


Fig. 1 Logic diagram.

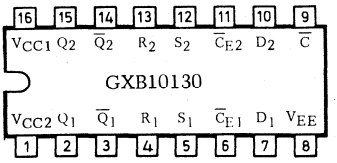


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 ± 10 % V
Operating ambient temperature range	T_{amb}		−30 to +85 °C
Average propagation delay	t_{PHL}	typ.	2,0 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package	P_{av}	typ.	110 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (see Package Outlines)

GXB10130P: plastic 16-lead dual in-line (SOT-38).
GXB10130D: ceramic 16-lead dual in-line (SOT-74).

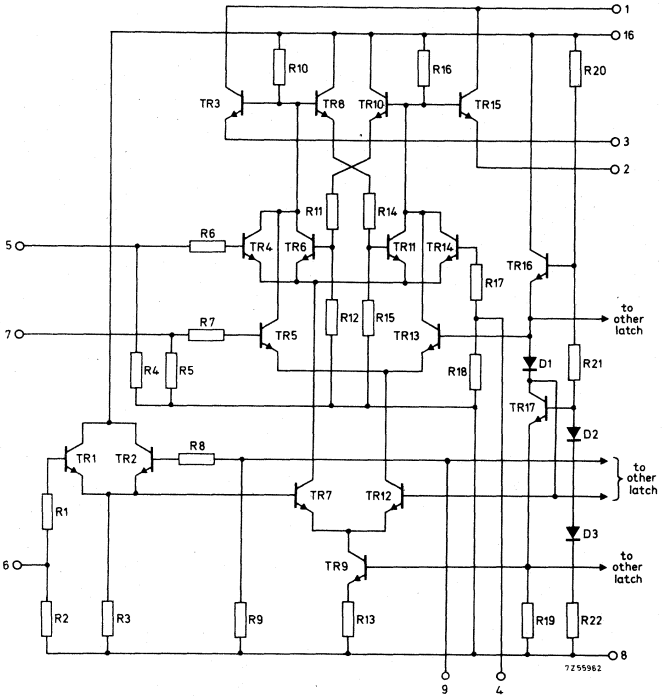
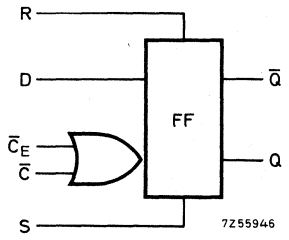


Fig. 3 Circuit diagram (one latch).



Synchronous operation

D_n	$\overline{C}$	$\overline{C_E}$	Q_{n+1} *
L	L	L	L
L	L	H	Q_n
L	H	L	Q_n
L	H	H	Q_n
H	L	L	H
H	L	H	Q_n
H	H	L	Q_n
H	H	H	Q_n

* R + S = LOW.

Asynchronous operation
($\overline{C}$ or $\overline{C_E}$ = HIGH)

R	S	Q_1
L	L	Q
L	H	H
H	L	L
H	H	**

** not allowed

HIGH state = 1
LOW state = 0

Fig. 4 Logic function.

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5,2 V.

	symbol		T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Input current HIGH							
pins 6, 11	I_{IH}	max.	350	220	220	μA	
pin 9	I_{IH}	max.	425	265	265	μA	
other inputs	I_{IH}	max.	455	285	285	μA	
Input current LOW	I_{IL}	min.	0,5	0,5	0,3	μA	
Supply current	I_{EE}	max.	38	35	38	mA	

A.C. CHARACTERISTICS

V_{CC1} = V_{CC2} = 0 V (ground); V_{EE} = −5,2 V.

	symbol		T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Rise and fall propagation delay times	t_{PLH}/t_{PHL}						
D → Q		min.	1,0	1,0	1,0	ns	
		max.	3,6	3,5	3,8	ns	
R → Q		min.	1,0	1,0	1,0	ns	
		max.	3,6	3,5	3,9	ns	
S → Q		min.	1,0	1,0	1,0	ns	
		max.	3,6	3,5	3,9	ns	
$\overline{C}$ → Q		min.	1,0	1,0	1,0	ns	
		max.	4,3	4,0	4,1	ns	
Rise and fall transition times	t_{TLH}/t_{THL}						
		min.	1,0	1,1	1,1	ns	between 20% and 80%
		max.	3,6	3,5	3,8	ns	between 20% and 80%
Set-up time D → C	t_s	min.	2,5	2,5	2,5	ns	
Hold time D → C	t_h	min.	1,5	1,5	1,5	ns	

For waveforms see Fig. 5.

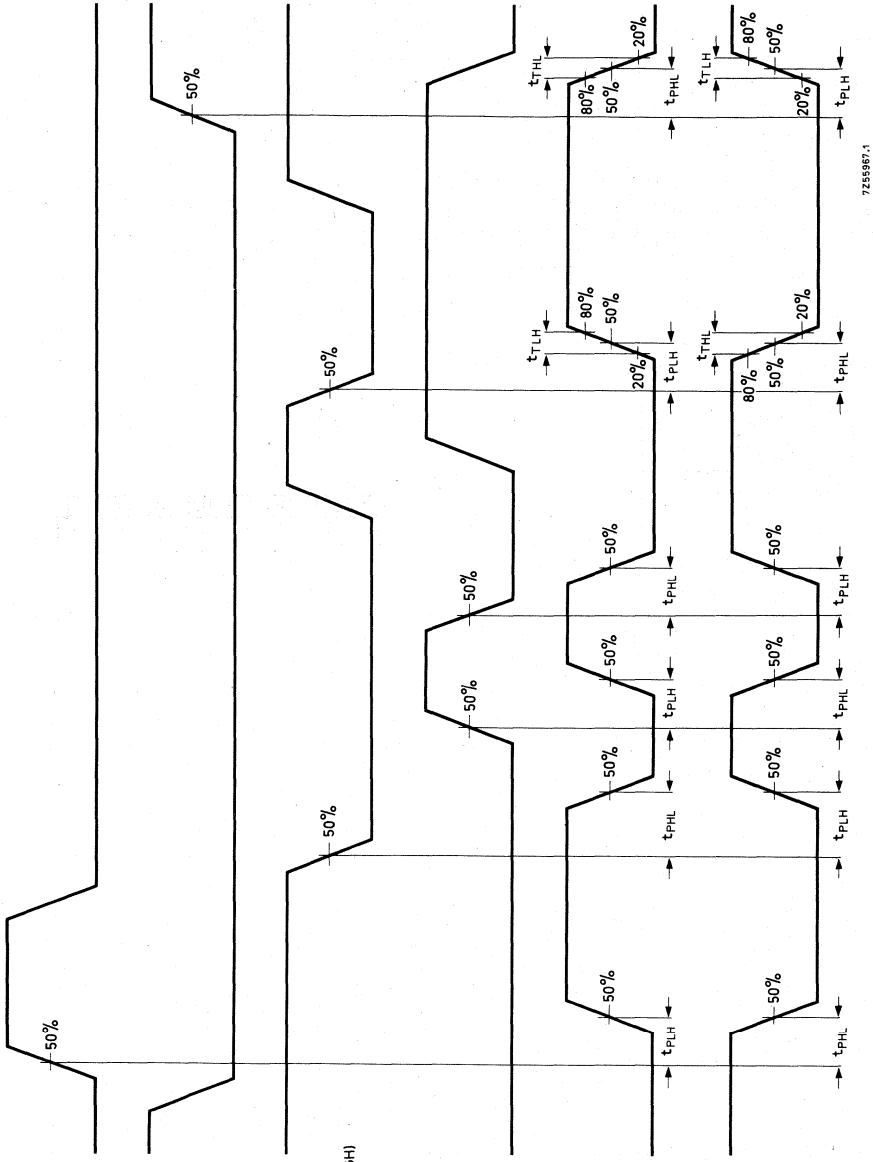


Fig. 5 Switching times waveforms. For input signals $t_{TLH} = t_{THL} = 2{,}0$ ns (between 20% and 80%); $V_{IH} = +1{,}1$ V; $V_{IL} = +0{,}3$ V.

DUAL D-TYPE MASTER-SLAVE FLIP-FLOP

The GXB10131 is a dual master-slave D-type flip-flop. Each flip-flop can be clocked separately by holding the common clock in the LOW state and using the clock enable inputs for the clocking function. The output states of the flip-flops change when the level of the clock is high.

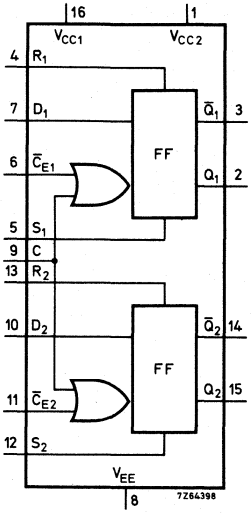


Fig. 1 Logic diagram.

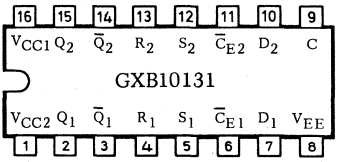


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 ± 10 % V
Operating ambient temperature range	T_{amb}		−30 to +85 °C
Clock frequency	f_C	typ.	160 MHz
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	1720 mV
Power consumption per package	P_{av}	typ.	230 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (see Package Outlines)

GXB10131P: plastic 16-lead dual in-line (SOT-38).
GXB10131D: ceramic 16-lead dual in-line (SOT-74).

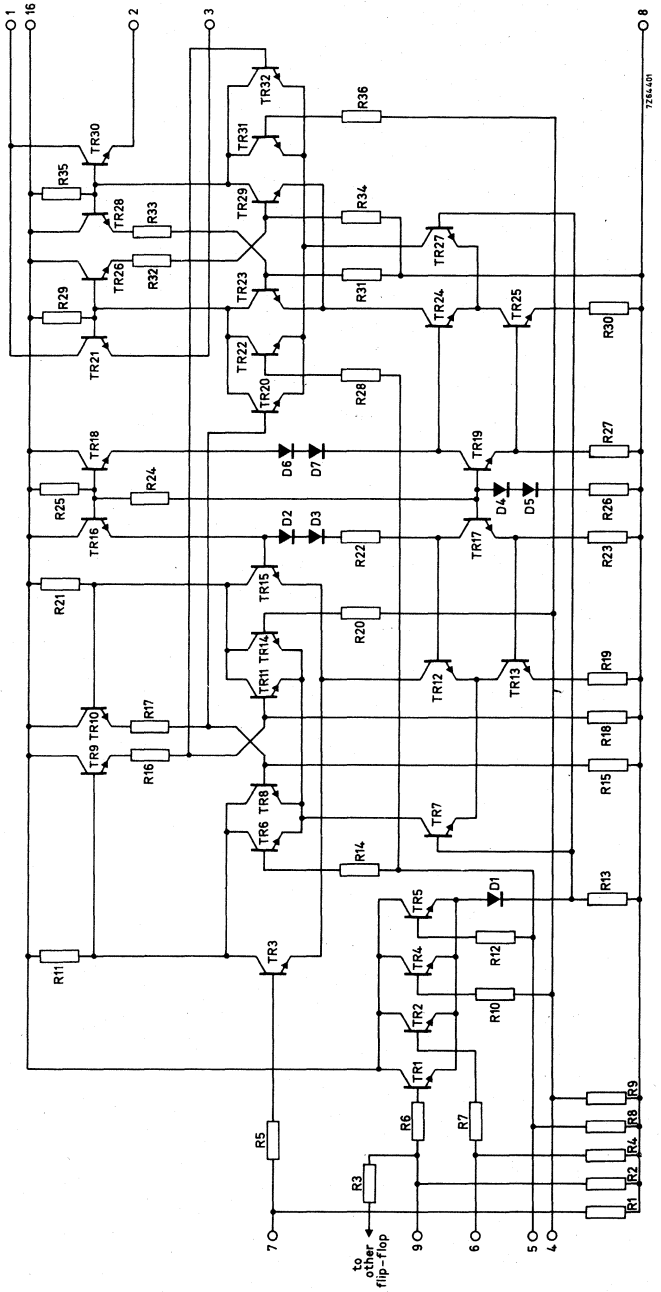
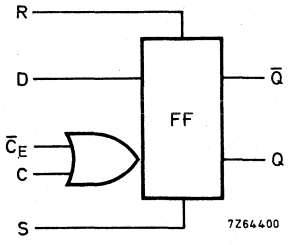


Fig. 3 Circuit diagram.



Synchronous operation

D_n	C	$\overline{C_E}$ *	Q_{n+1} **
L	L	L	Q_n
L	L	H	Q_n
L	H	L	L
L	H	H	Q_n
H	L	L	Q_n
H	L	H	Q_n
H	H	L	H
H	H	H	Q_n

Asynchronous operation

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N

Positive logic:

HIGH state = 1
LOW state = 0
N = not allowed.

Fig. 4 Logic function (one flip-flop).

* Conditions for C and $\overline{C_E}$ may be interchanged. In this table $\overline{C_E}$ is static, while for C a H represents a transition from L to H between t_n and t_{n+1}.

** R + S = LOW.

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = −5,2 V.

	symbol		T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Input current HIGH							
pin 4,5,12,13	I_{IH}	max.	525	330	330	μA	
pin 6,11	I_{IH}	max.	350	220	220	μA	
pin 7,10	I_{IH}	max.	390	245	245	μA	
pin 9	I_{IH}	max.	425	265	265	μA	
Input current LOW	I_{IL}	min.	0,5	0,5	0,3	μA	
Supply current	I_{EE}	max.	62	56	62	mA	

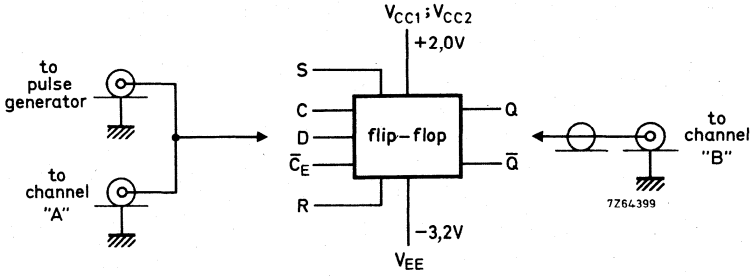


Fig. 5 Measurement of propagation delay.

A.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = −5,2 V.

	symbol		T_{amb} (°C) −30	+25	+85	unit	remarks
Rise propagation delay time							
S → Q	t_{PLH}	min.	1,7	1,8	1,8	ns	see Figs 5 and 7
		max.	4,4	4,3	4,8	ns	
R → $\overline{Q}$	t_{PLH}	min.	1,7	1,8	1,8	ns	see Figs 5 and 7
		max.	4,4	4,3	4,8	ns	
C → Q	t_{PLH}	min.	1,7	1,8	1,8	ns	see Figs 5 and 7
		max.	4,6	4,5	5,0	ns	
Fall propagation delay time							
S → $\overline{Q}$	t_{PHL}	min.	1,7	1,8	1,8	ns	see Figs 5 and 7
		max.	4,4	4,3	4,8	ns	
R → Q	t_{PHL}	min.	1,7	1,8	1,8	ns	see Figs 5 and 7
		max.	4,4	4,3	4,8	ns	
C → Q	t_{PHL}	min.	1,7	1,8	1,8	ns	see Figs 5 and 7
		max.	4,6	4,5	5,0	ns	
Rise time	t_{TLH}	min.	1,0	1,1	1,1	ns	between 20% snd 80%
		max.	4,6	4,5	4,9	ns	
Fall time	t_{THL}	min.	1,0	1,1	1,1	ns	between 20% snd 80%
		max.	4,6	4,5	4,9	ns	
Set-up time	t_s	min.	2,5	2,5	2,5	ns	see Fig. 7
Hold time	t_h	min.	1,5	1,5	1,5	ns	see Fig. 7
Clock frequency	f_c	min.	125	125	125	MHz	see Fig. 6.

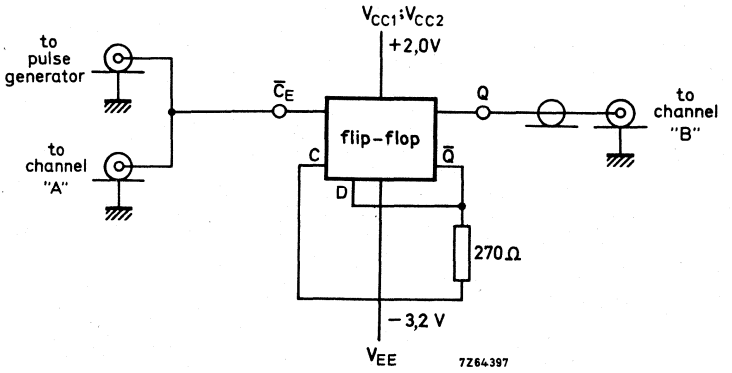


Fig. 6 Switching times test circuit. Measurement of clock frequency.

$t_{THL} = t_{THL}$ = 2,0 ns (20% to 80%).

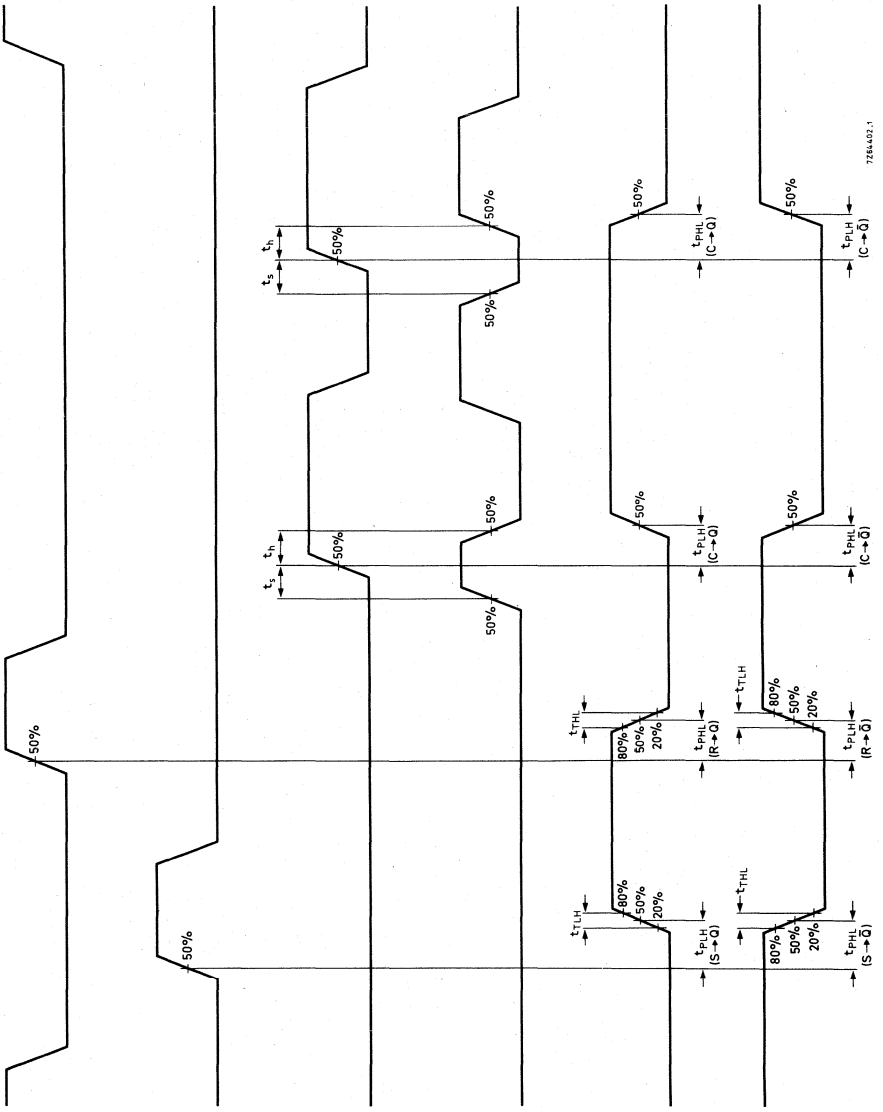


Fig. 7 Switching times waveforms. $V_{IH} = +1{,}11$ V; $V_{IL} = 0{,}31$ V.

DUAL MULTIPLEXER WITH D-TYPE LATCHES

The GXB10132 is a dual 2-input multiplexer with clocked D-type latches and common reset. Latches can be clocked by the common clock (C) when the clock enable input (C_E) is LOW or by the clock enable input when the common clock is held in the LOW state. The outputs are latched by the positive transition of the clock (leading edge). Any change in the data input will be registered at the output only if the clock is LOW. Data inputs are selected by a common data select input (D_S).

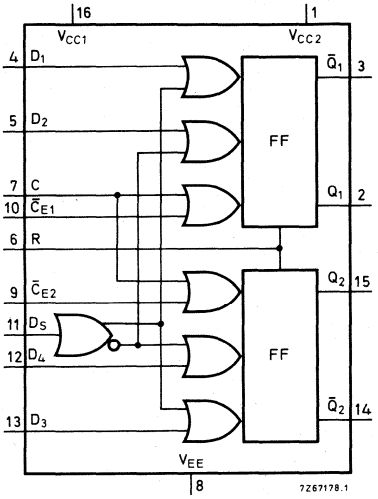


Fig. 1 Logic diagram.

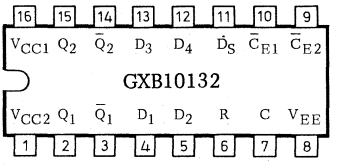


Fig. 2 Pin designation.
$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 ± 10% V
Operating ambient temperature range	T_{amb}		−30 to + 85 °C
Average propagation delay	t_{PLH}	typ.	3,0 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package	P_{av}	typ.	210 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see Package Outlines)

GXB10132P : plastic 16-lead dual in-line (SOT-38).
GXB10132D: ceramic 16-lead dual in-line (SOT-74).

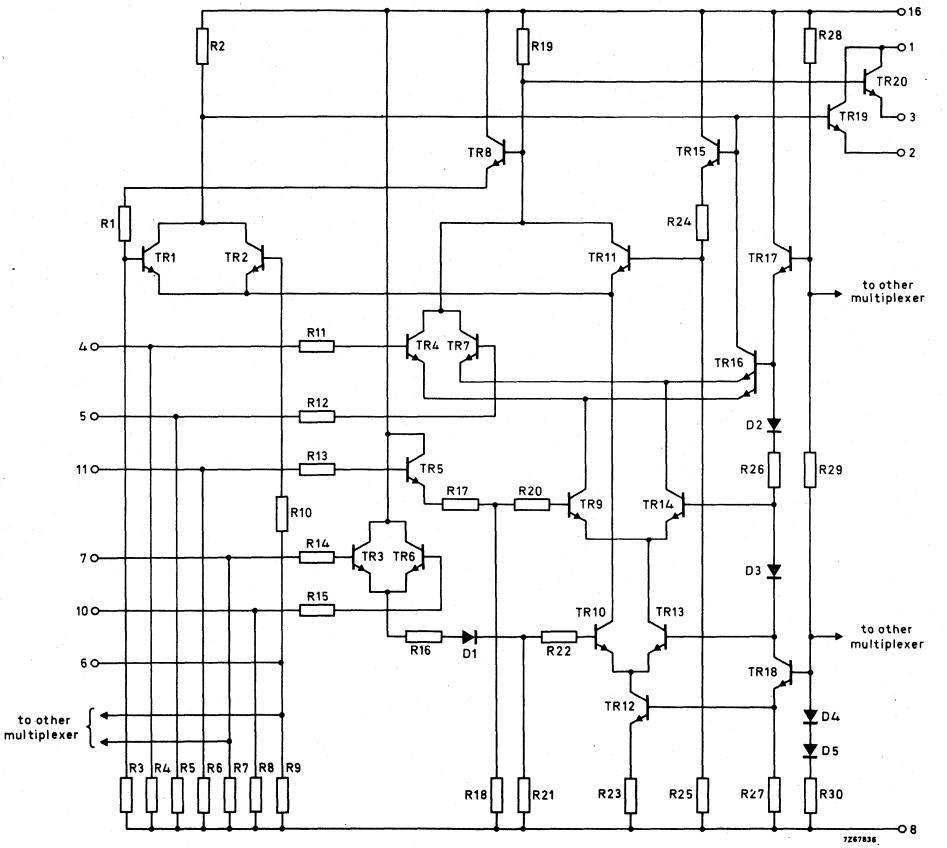


Fig. 3 Circuit diagram (one multiplexer).

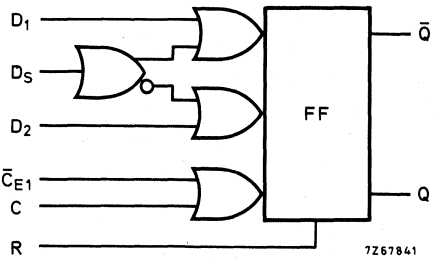


Fig. 4 Logic function.

R	D_S	C	$\overline{C}_E$	Q_{n+1}
L	L	L	L	D_1
L	L	L	H	Q_n
L	L	H	L	Q_n
L	L	H	H	Q_n
L	H	L	L	D_2
L	H	L	H	Q_n
L	H	H	L	Q_n
L	H	H	H	Q_n
H	X	X	H	L
H	X	H	X	L
H	X	L	L	Q_n

RATINGS see Family Specifications

D.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = −5,2 V

	symbol		T_{amb} (°C) −30	+ 25	+ 85	unit	remarks
Input current HIGH							
pins 4,5,7,12,13	I_{IH}	max.	460	290	290	μA	
pin 6	I_{IH}	max.	620	390	390	μA	
pins 9,10,11	I_{IH}	max.	425	265	265	μA	
Input current LOW	I_{IL}	min.	0,5	0,5	0,3	μA	
Supply current	I_{EE}	max.	60	55	60	mA	

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = + 2,0 V; V_{EE} = −3,2 V

	symbol		T_{amb} (°C) −35	+ 25	+ 85	unit	remarks
Rise propagation delay times							
D → Q	t_{PLH}	min.	1,0	1,0	1,0	ns	For waveforms see Fig. 5.
		max.	3,6	3,3	3,7	ns	
R → Q	t_{PLH}	min.	1,0	1,0	1,0	ns	
		max.	4,0	3,8	4,2	ns	
C → Q	t_{PLH}	min.	1,0	1,0	1,0	ns	
		max.	6,0	5,7	6,3	ns	
D_S → Q	t_{PLH}	min.	1,0	1,0	1,0	ns	
		max.	4,8	4,6	5,0	ns	
Rise time	t_{TLH}	min.	1,5	1,5	1,5	ns	between 20% and 80%
		max.	3,7	3,5	3,8	ns	
Fall time	t_{THL}	min.	1,5	1,5	1,5	ns	
		max.	3,7	3,5	3,8	ns	

For **switching times test circuit** see Family Specifications.

Notes

1. Any change on the data input will be registered at the output only if the clock is LOW.
2. Outputs are latched on the positive transition of the clock.
3. The reset input is enbled when the clock is HIGH.

Positive logic: HIGH state = 1
LOW state = 0
H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

D.C. CHARACTERISTICS (continued)

	symbol	T_{amb} (°C) −35	+ 25	+ 85	unit	remarks
Set-up time						
D → C	t_s min.	2,5	2,5	2,5	ns	
D_S → C	t_s min.	3,5	3,5	3,5	ns	
Hold time						
D → C	t_h min.	1,5	1,5	1,5	ns	
D_S → C	t_h min.	1,0	1,0	1,0	ns	

Conditions for inputs signals: $t_{TLH} = t_{THL} = 2{,}0$ ns (20 to 80%).

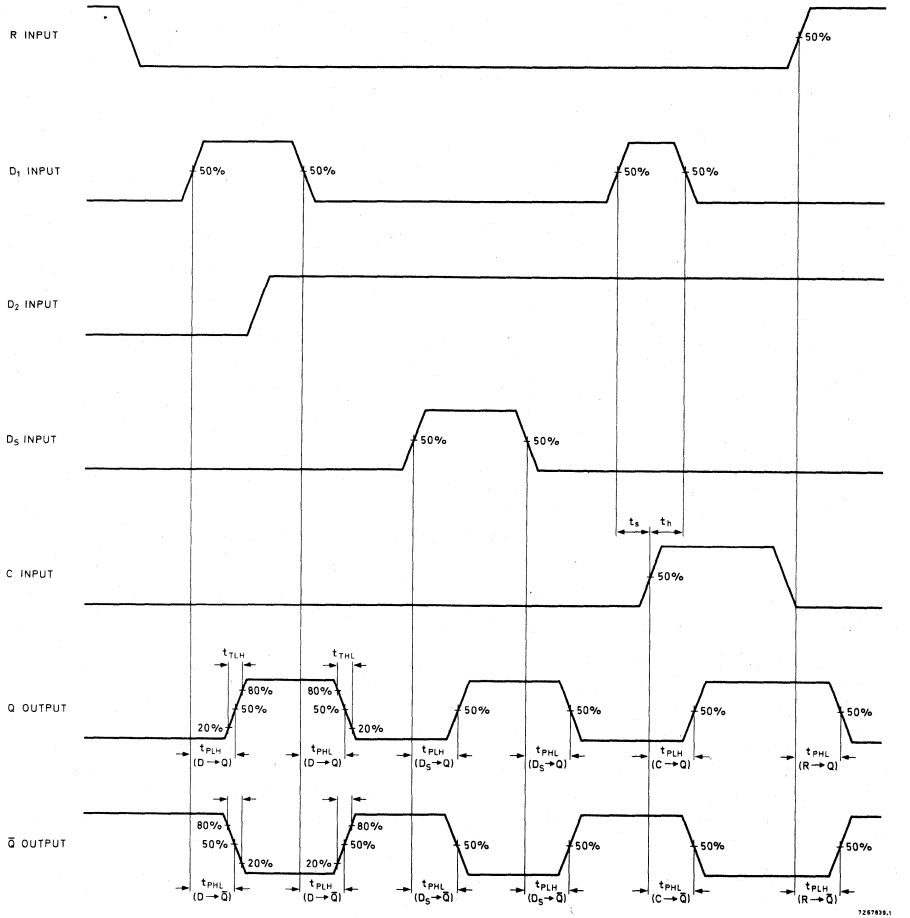


Fig. 5 Switching times waveforms. $V_{IH} = +1{,}11$ V; $V_{IL} = +0{,}31$ V.

QUADRUPLE LATCH

The GXB10133 is a quadruple latch with D-type inputs and enable outputs. Data (D) inputs are registered at the output while the clock is HIGH. Data inputs are latched by the negative transition of the clock (trailing edge).

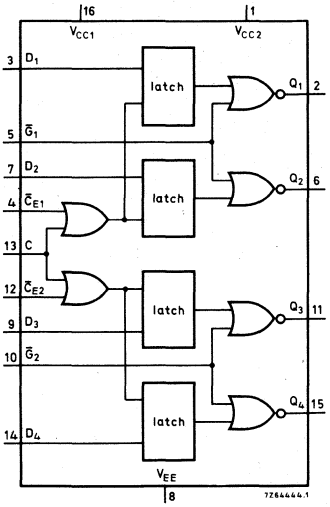


Fig. 1 Logic diagram.

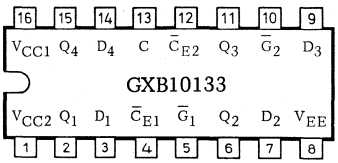


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 ± 10 % V
Operating ambient temperature range	T_{amb}		−30 to +85 °C
Average propagation delay	t_{PLH}	typ.	4 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package	P_{av}	typ.	310 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (see Package Outlines)

GXB10133P: plastic 16-lead dual in-line (SOT-38).
GXB10133D: ceramic 16-lead dual in-line (SOT-74).

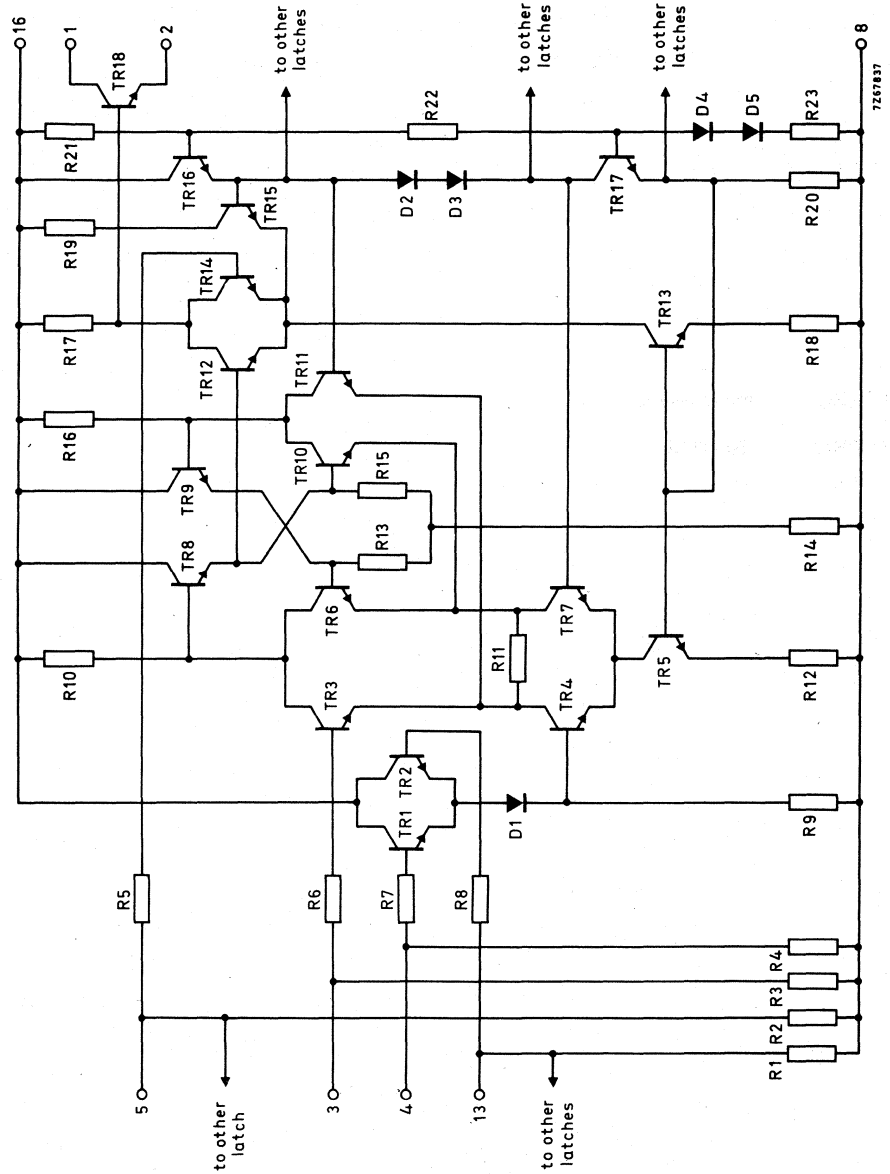


Fig. 3 Circuit diagram (one latch).

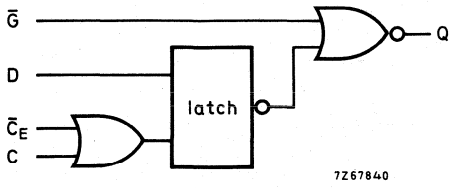


Fig. 4 Logic function.

$\overline{G}$	C	$\overline{C_E}$	D	Q_{n+1}
H	X	X	X	L
L	L	L	X	Q_n
L	L	H	L	L
L	H	L	L	L
L	H	H	L	L
L	L	H	H	H
L	H	L	H	H
L	H	H	H	H

Positive logic: HIGH state = 1
LOW state = 0
H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = −5,2 V.

	symbol		T_{amb} (°C) −30	+25	+85	unit	remarks
Input current HIGH							
pins 3,7,9,14		max.	390	245	245	μA	
pins 4,12	I_{IH}	max.	425	265	265	μA	
pins 5,10,13		max.	560	350	350	μA	
Input current LOW	I_{IL}		0,5	0,5	0,3	μA	
Supply current	I_{EE}	max.	82	75	82	mA	

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = +2,0 V; V_{EE} = −3,2 V.

	symbol		T_{amb} (°C) −30	+25	+85	unit	remarks
Rise propagation delay time:							
D → Q	t_{PLH}	min.	1,0	1,0	1,1	ns	data
		max.	5,6	5,4	5,9	ns	
C → Q	t_{PLH}	min.	1,0	1,0	1,2	ns	clock
		max.	5,4	5,4	6,0	ns	
$\overline{G}$ → Q	t_{PLH}	min.	1,0	1,0	1,0	ns	gate enable
		max.	3,2	3,1	3,4	ns	

	symbol		T_{amb} (°C) −30	+25	+85	unit	remarks
Rise time	t_{TLH}	min.	1,0	1,1	1,1	ns	between 20 and 80%
		max.	3,6	3,5	3,8	ns	
Fall time	t_{THL}	min.	1,0	1,1	1,1	ns	
		max.	3,6	3,5	3,8	ns	
Set-up time	t_s	min.	2,5	2,5	2,5	ns	
Hold time	t_h	min.	1,5	1,5	1,5	ns	

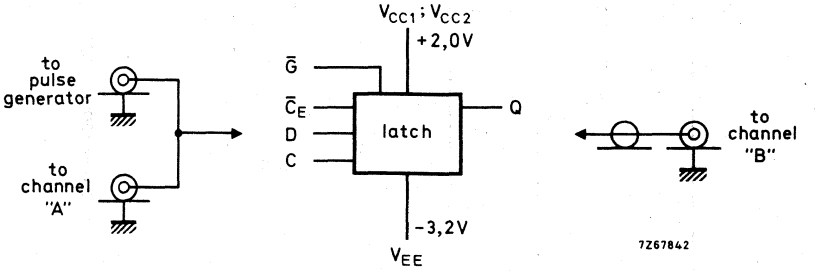


Fig. 5 Switching times test circuit.

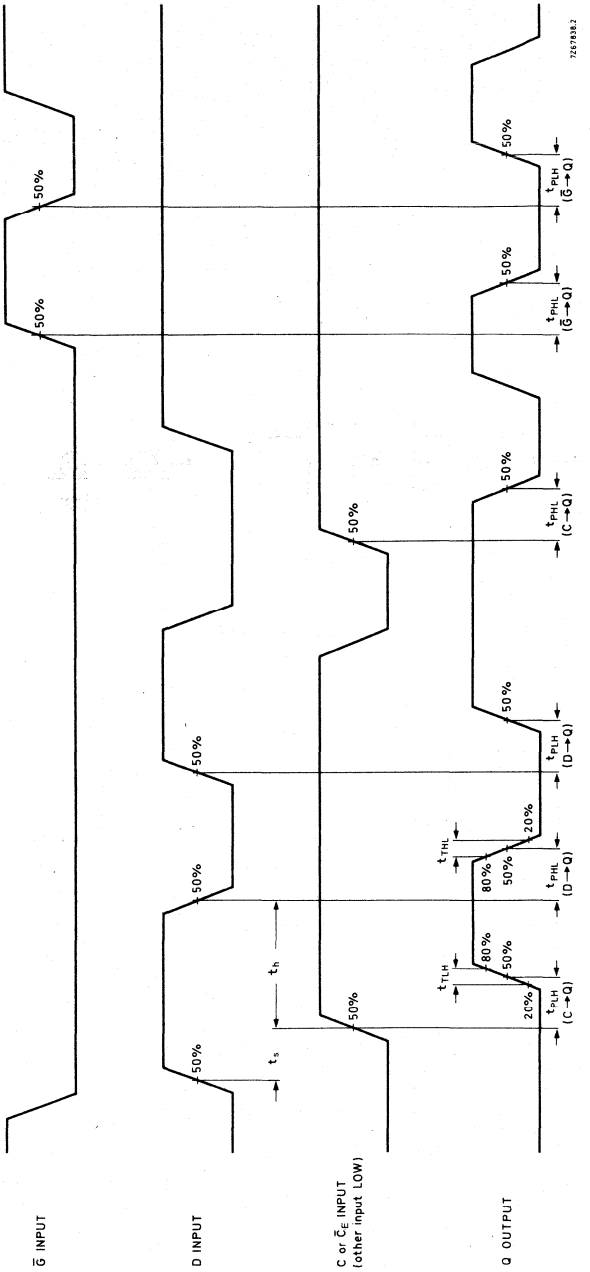


Fig. 6 Switching times waveforms. Conditions for input signals; $t_r = t_f = 2{,}0$ ns (20% to 80%); $V_{IH} = +1{,}1$ V; $V_{IL} = +0{,}3$ V.

DUAL MULTIPLEXER WITH D-TYPE LATCHES

The GXB10134 is a dual 2-input multiplexer with clocked D-type latches. Latches can be clocked by the common clock (C) when the clock enable input (C_E) is LOW or by the clock enable input when the common clock is held in the LOW state. The outputs are latched by the positive transition of the clock (leading edge). Any change in the data input will be registered at the output only if the clock is LOW. Data inputs are selected by two data select inputs (D_{S1} and D_{S2}).

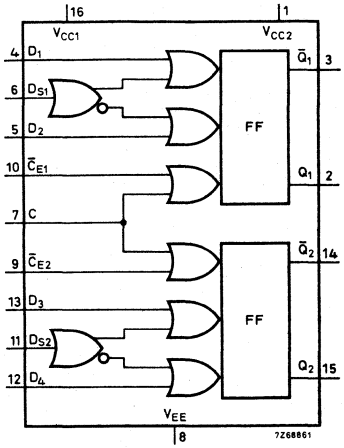


Fig. 1 Logic diagram.

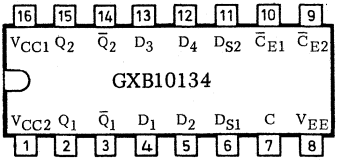


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 ± 10 % V
Operating ambient temperature range	T_{amb}		−30 to +85 °C
Average propagation delay	t_{PHL}	typ.	3,0 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package	P_{av}	typ.	220 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (see Package Outlines)

GXB10134P: plastic 16-lead dual in-line (SOT-38).
GXB10134D: ceramic 16-lead dual in-line (SOT-74).

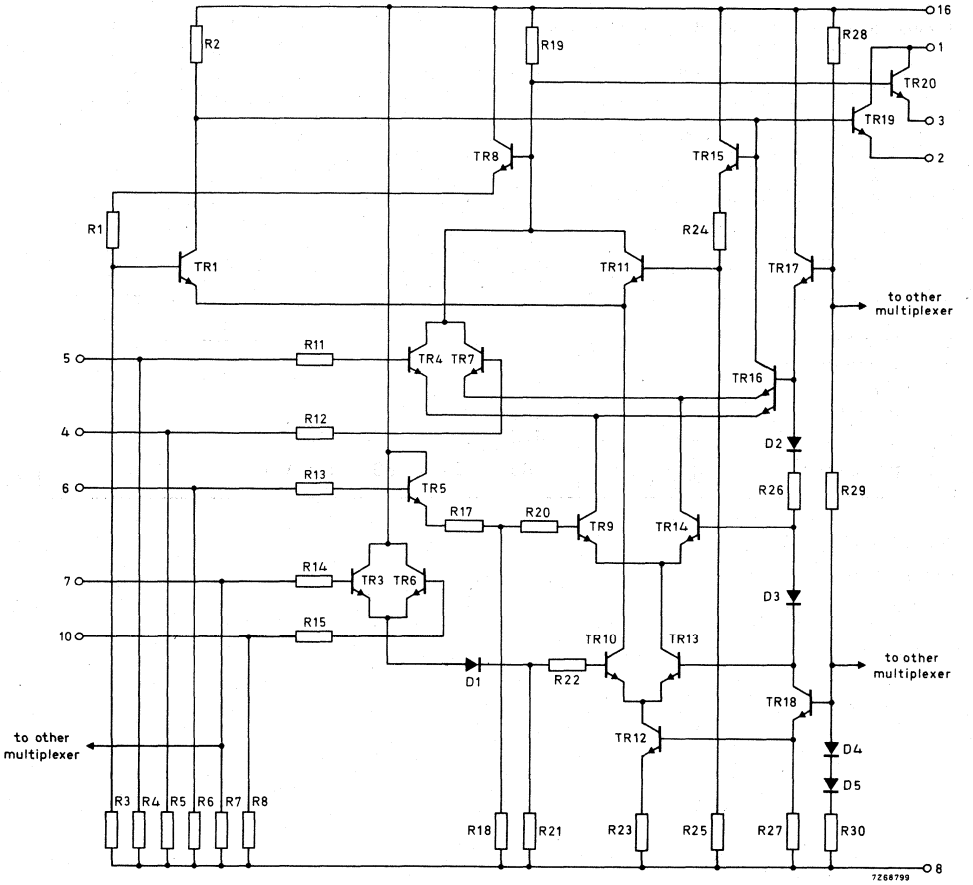


Fig. 3 Circuit diagram (one multiplexer).

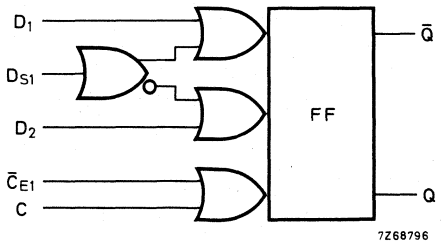


Fig. 4 Logic function.

D_S	C	$\overline{C_E}$	Q_{n+1}
L	L	L	D_1
L	L	H	Q_n
L	H	L	Q_n
L	H	H	Q_n
H	L	L	D_2
H	L	H	Q_n
H	H	L	Q_n
H	H	H	Q_n

Function table.

1. Any change on the data input will be registered at the output only if the clock is LOW
2. Outputs are latched on the positive transition of the clock.

Positive logic: HIGH state = 1
LOW state = 0
H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS see Family Specifications

D.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = −5,2 V.

	symbol		T_{amb} (°C) −30	+25	+85	unit	remarks
Input current HIGH							
inputs 4,5,7,12,13	I_{IH}	max.	460	290	290	μA	
inputs 6,9,10,11	I_{IH}	max.	425	265	265	μA	
Supply current	I_{EE}	max.	60	55	60	mA	

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = +2,0$ V; $V_{EE} = -3,2$ V.

	symbol		T_{amb} (°C) −30	+25	+85	unit	remarks
Rise propagation delay time							
D → Q	t_{PLH}	min.	1,0	1,0	1,0	ns	DATA
		max.	3,5	3,3	3,6	ns	
C → Q	t_{PLH}	min.	1,0	1,0	1,0	ns	CLOCK
		max.	6,0	5,7	6,3	ns	
D_S → Q	t_{PLH}	min.	1,0	1,0	1,0	ns	DATA SELECT
		max.	4,8	4,6	5,0	ns	
Rise/fall time	t_{TLH} / t_{THL}	min.	1,5	1,5	1,5	ns	between 20 and 80%
		max.	3,7	3,5	3,8	ns	
Set-up time							
D → C	t_s	min.	2,5	2,5	2,5	ns	
D_s → C	t_s	min.	3,5	3,5	3,5	ns	
Hold time							
C → D	t_h	min.	1,5	1,5	1,5	ns	
C → D_s	t_h	min.	1,0	1,0	1,0	ns	

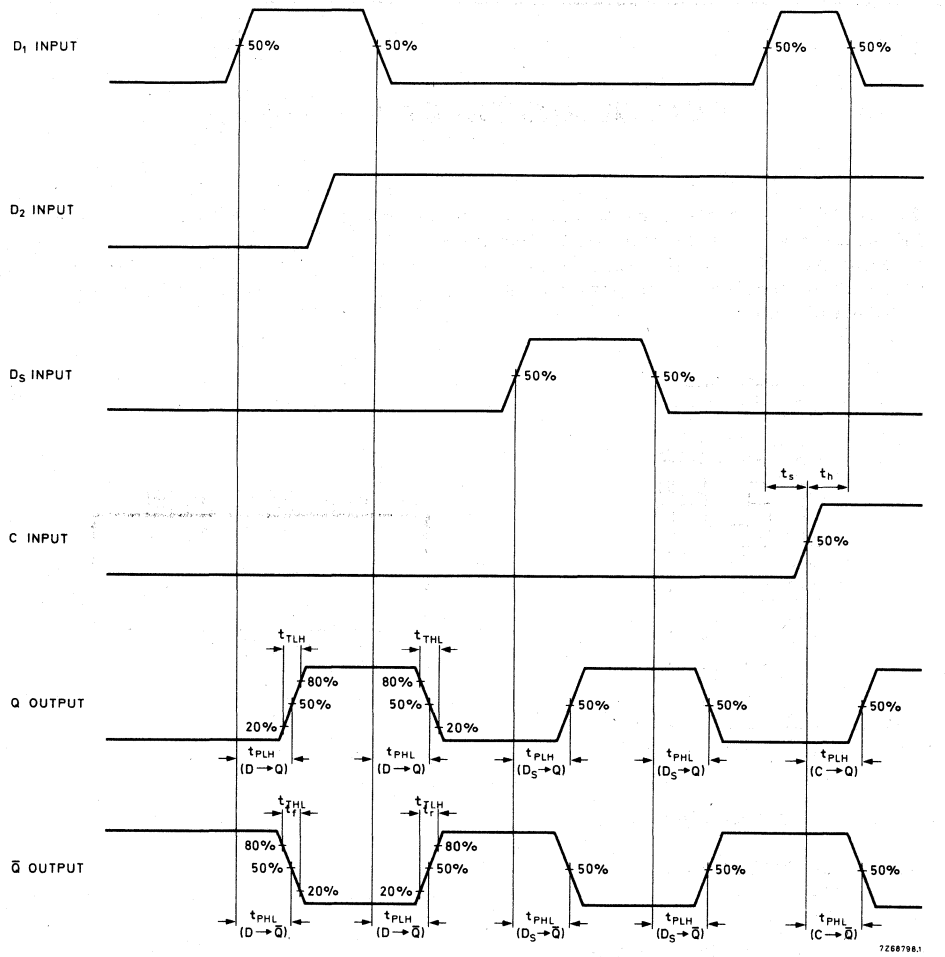


Fig. 5 Switching times waveforms.

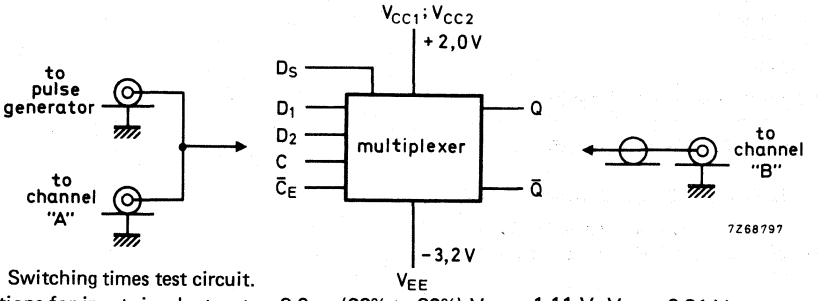


Fig. 6 Switching times test circuit.
Conditions for input signals: $t_r = t_f = 2{,}0$ ns (20% to 80%). $V_{IH} = 1{,}11$ V; $V_{IL} = 0{,}31$ V.

DUAL JK MASTER-SLAVE FLIP-FLOP

The GXB10135 is a dual master-slave d.c. coupled JK flip-flop. It contains a common clock and separate $\overline{J}\,\overline{K}$ inputs which do not effect the output when the clock is static. The outputs of the GXB10135 change state with the positive transition of the clock. Asynchronous set (S) and reset (R) inputs are provided which override the clock. Unused inputs need not be tied to V_{EE} since input pull-down resistors are integrated in the circuit.

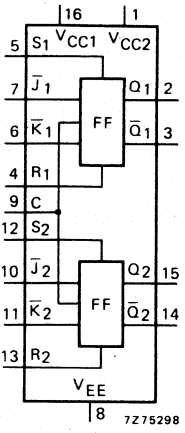


Fig. 1 Logic diagram.

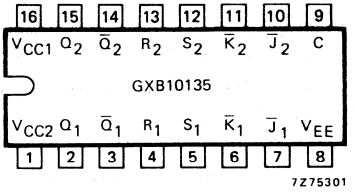


Fig. 2 Pin designation.
$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	$-5{,}2 \pm 10\%$	V
Operating ambient temperature range	T_{amb}	-30 to $+85$	°C
Clock frequency	f_C	typ. 140	MHz
Output voltage			
HIGH state	V_{OH}	nom. -880	mV
LOW state	V_{OL}	nom. -1720	mV
Power consumption per package (no load)	P_{av}	typ. 280	mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see Package Outlines)

GXB10135P : 16-lead DIL; plastic (SOT-38).
GXB10135D: 16-lead DIL; ceramic (SOT-47).

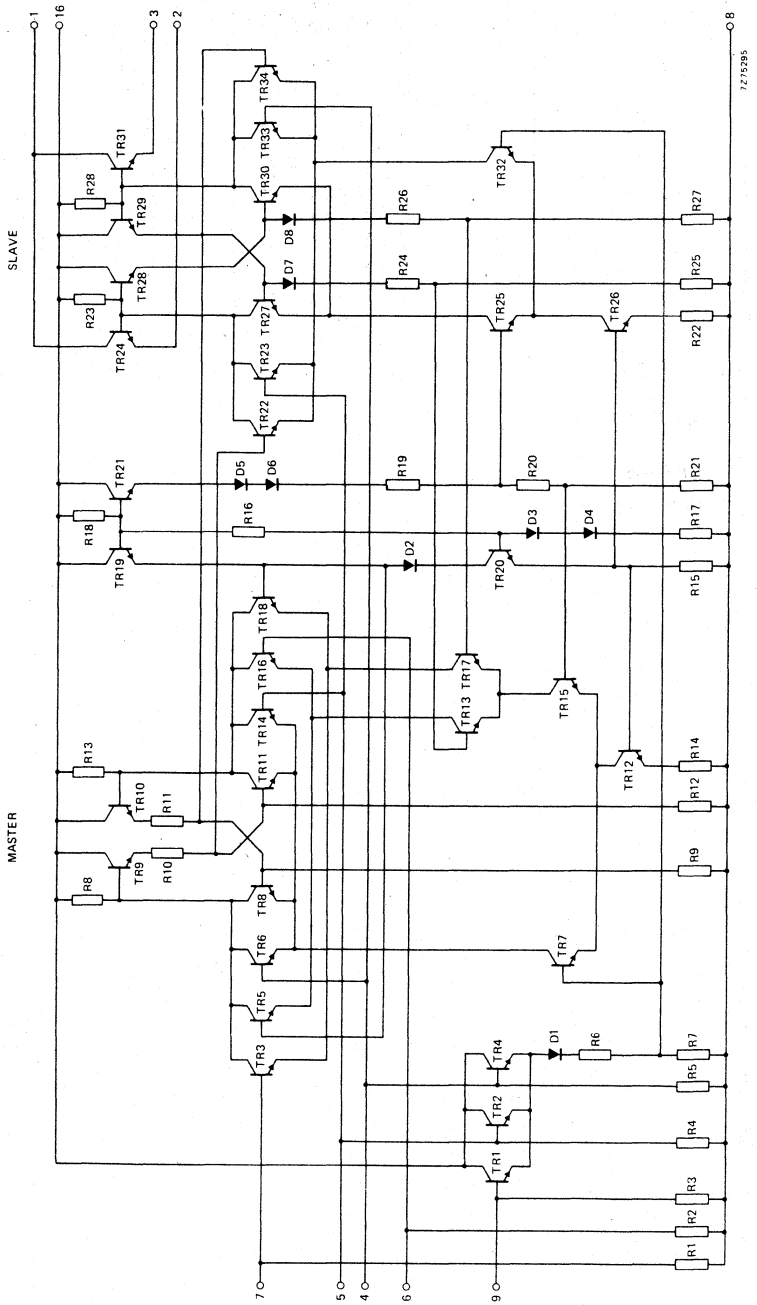


Fig. 3 Circuit diagram (one flip-flop).

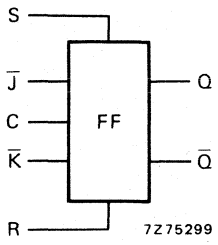


Fig. 4 Logic function.

FUNCTION TABLES

R	S	$Q_n + 1$
L	L	Q_n
L	H	H
H	L	L
H	H	*

$\overline{J}$	$\overline{K}$	$Q_n + 1$
L	L	$\overline{Q}_n$
H	L	L
L	H	H
H	H	Q_n

* Not allowed.

Positive logic: HIGH state = 1
LOW state = 0
H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS see Family Specifications

D.C. CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground; $V_{EE} = -5{,}2$ V

	symbol		T_{amb} (°C) −30	+ 25	+ 85	unit	remarks
Input currents HIGH							
pins 6,7,9,10,11	I_{IH}	max.	425	265	265	μA	
pins 4,5,12,13	I_{IH}	max.	620	390	390	μA	
Input current LOW	I_{IL}	min.	0,5	0,5	0,3	μA	
Supply current	I_{EE}	max.	75	68	75	mA	

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2$ V; $V_{EE} = -3{,}2$ V; input pulse condition $t_{TLH} = t_{THL} = 2$ ns ± 0,2.

	symbol		T_{amb} (°C) −30	+ 25	+ 85	unit	remarks
Rise and fall propagation delay times	t_{PLH} / t_{PHL}						
C → Q/$\overline{Q}$		min.	1,8	1,8	1,8	ns	
		max.	5,0	4,5	4,6	ns	clock
S → Q/$\overline{Q}$		min.	1,8	1,8	1,8	ns	
		max.	5,6	5,0	5,2	ns	set
R → Q/$\overline{Q}$		min.	1,8	1,8	1,8	ns	
		max.	5,6	5,0	5,2	ns	reset

	symbol		T_{amb} (°C) −30	+ 25	+ 85	unit	remarks
Rise time	t_{TLH}	min.	1,1	1,1	1,1	ns	between 20% and 80%
		max.	4,8	4,5	4,7	ns	
Fall time	t_{THL}	min.	1,1	1,1	1,1	ns	
		max.	4,8	4,5	4,7	ns	
Set-up time	t_s	min.	2,5	2,5	2,5	ns	C → $\overline{K}$
Hold time	t_h	min.	1,5	1,5	1,5	ns	
Clock frequency	f_C	min.	125	125	125	MHz	

For **switching times test circuit** see Family Specifications.

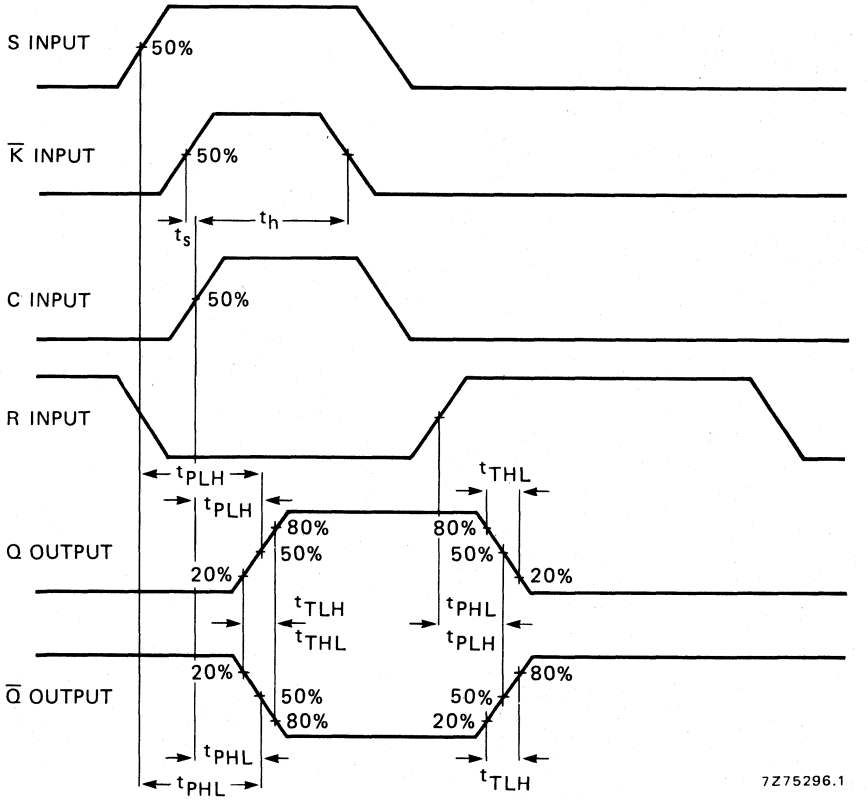


Fig. 5 Switching times waveforms; V_{IH} = 1,11 V; V_{IL} = 0,31 V.

UNIVERSAL HEXADECIMAL COUNTER

The GXB10136 is a high speed hexadecimal synchronous counter that can count up, count down, preset, or stop count at frequencies exceeding 100 MHz.
The operation mode of the counter is programmed by three control lines (S_1, S_2 and $\overline{C}_{IN}$) as can be seen in the function select table. In the preset mode (loading step), a clock pulse is needed for the information present on the data inputs (D_0, D_1, D_2 and D_3) to be entered into the counter.
$\overline{C}_{OUT}$ goes LOW on the terminal count, or when the counter is being preset.
The counter changes state only on the positive-going edge of the clock, so at any other time, any other input may change without any result (except for $\overline{C}_{OUT}$).
This binary counter can be used in many applications, such as in computing for high speed control processors and peripheral controllers.

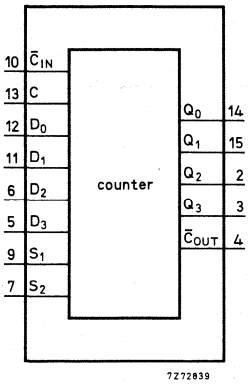


Fig. 1 Block diagram.

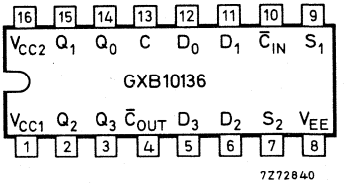


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	$-5{,}2 \pm 10\%$	V
Operating ambient temperature	T_{amb}	-30 to $+85$	°C
Clock frequency	f_C	typ. 150	MHz
Output voltage			
HIGH state	V_{OH}	nom. -880	mV
LOW state	V_{OL}	nom. -1720	mV
Power consumption per package	P_{av}	typ. 625	mW

For **FAMILY DATA** see Family Specifications.

PACKAGE OUTLINE (see Package Outlines)

GXB10136P : plastic 16-lead dual in-line (SOT-38).
GXB10136D: ceramic 16-lead dual in-line (SOT-74).

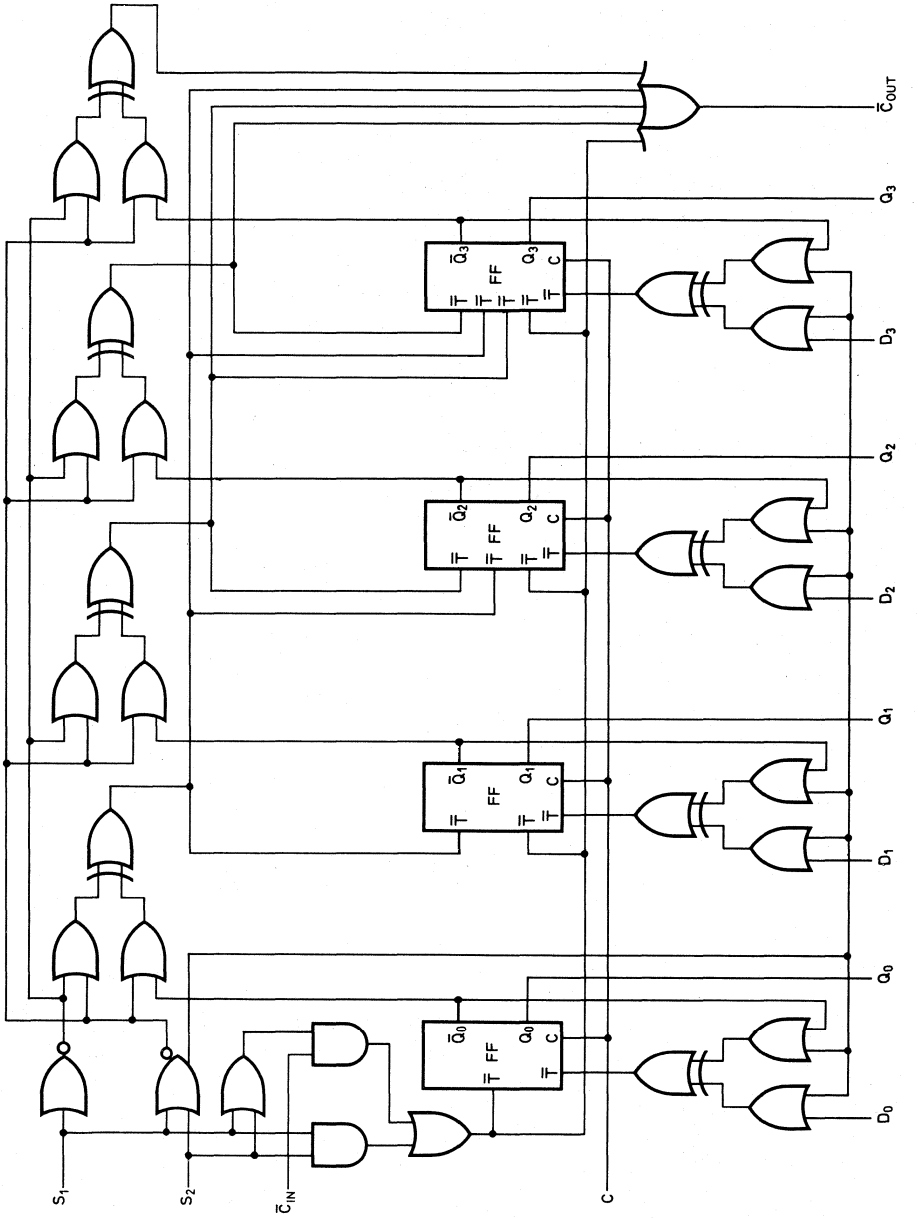


Fig. 3 Logic diagram.

FUNCTION SELECT TABLE

S_1	S_2	operating mode
L	L	preset (programme)
L	H	increment (count up)
H	L	decrement (count down)
H	H	hold (stop count)

Positive logic:
H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0
X = state is immaterial

SEQUENTIAL FUNCTION TABLE

inputs								outputs				
S_1	S_2	D_0	D_1	D_2	D_3	$\overline{C}_{IN}$	C	Q_0	Q_1	Q_2	Q_3	$\overline{C}_{OUT}$
L	L	L	L	H	H	X	H	L	L	H	H	L
L	H	X	X	X	X	L	H	H	L	H	H	H
L	H	X	X	X	X	L	H	L	H	H	H	H
L	H	X	X	X	X	L	H	H	H	H	H	L
L	H	X	X	X	X	H	L	H	H	H	H	H
L	H	X	X	X	X	H	H	H	H	H	H	H
H	H	X	X	X	X	X	H	H	H	H	H	H
L	L	H	H	L	L	X	H	H	H	L	L	L
H	L	X	X	X	X	L	H	L	H	L	L	H
H	L	X	X	X	X	L	H	H	L	L	L	H
H	L	X	X	X	X	L	H	L	L	L	L	L
H	L	X	X	X	X	L	H	H	H	H	H	H

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = −5,2 V.

	symbol		T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Input current HIGH							
pins 5,6,11,12	I_{IH}	max.	350	220	220	μA	
pins 9 and 10	I_{IH}	max.	390	245	245	μA	
pin 7	I_{IH}	max.	425	265	265	μA	
pin 13	I_{IH}	max.	460	290	290	μA	
Input current LOW	I_{IL}	min.	0,5	0,5	0,3	μA	
Supply current	I_{EE}	max.	165	150	165	mA	

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = +2\ V$; $V_{EE} = -3{,}2\ V$

	symbol		T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Rise and fall propagation delay time							
C → Q	t_{PLH} / t_{PHL}	min.	0,8	1,0	1,4	ns	
		max.	4,8	4,5	5,0	ns	
C → $\overline{C}_{OUT}$	t_{PLH} / t_{PHL}	min.	2,0	2,5	2,4	ns	
		max.	10,9	10,5	11,5	ns	
$\overline{C}_{IN}$ → $\overline{C}_{OUT}$	t_{PLH} / t_{PHL}	min.	1,6	1,6	1,9	ns	
		max.	7,4	6,9	7,5	ns	
Rise/fall transition time	t_{TLH} / t_{THL}	min.	0,9	1,0	1,0	ns	between 20% and 80%
		max.	3,3	3,3	3,5	ns	
Set-up time							
D_n → C	t_s	min.	3,5	3,5	3,5	ns	Fig. 4
S → C	t_s	min.	7,5	7,5	7,5	ns	Fig. 4
$\overline{C}_{IN}$ → C	t_s	min.	4,5	3,7	4,5	ns	Fig. 7 - a
C → C_{IN}	t_s	min.	−1,0	−1,0	−1,0	ns	Fig. 7 - c
Hold time							
C → D_n	t_h	min.	0	0	0	ns	Fig. 4
C → S	t_h	min.	−2,5	−2,5	−2,5	ns	Fig. 4
C → $\overline{C_{IN}}$	t_h	min.	−1,6	−1,6	−1,6	ns	Fig. 7 - b
$\overline{C}_{IN}$ → C	t_h	min.	4,0	3,1	4,0	ns	Fig. 7 - d
Counting frequency							
count up	$f_{c\,up}$		125	125	125	MHz	
count down	$f_{c\,down}$		125	125	125	MHz	

For **switching times test circuit** see Family Specifications.

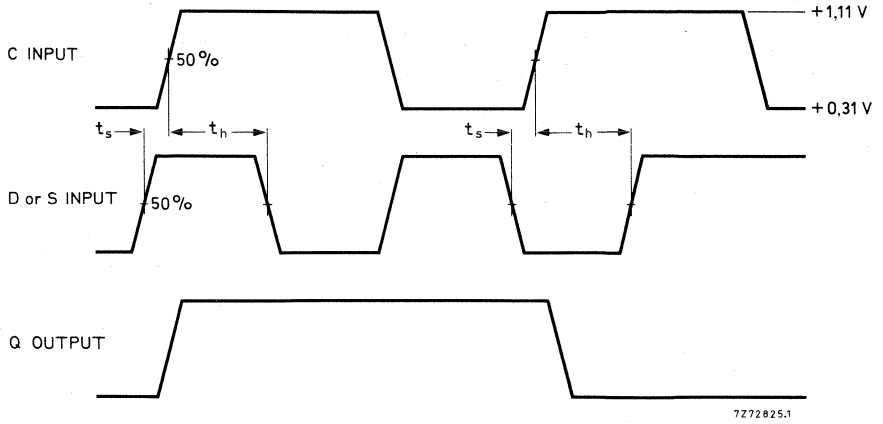


Fig. 4 Switching times waveforms.

Set-up times are the minimum times before the positive transition of the clock pulse (C) that information must be present at the data input (D) or control input (S).

Hold times are the minimum times after the positive transition of the clock pulse (C) that information must remain unchanged at the data input (D) or control input (S).

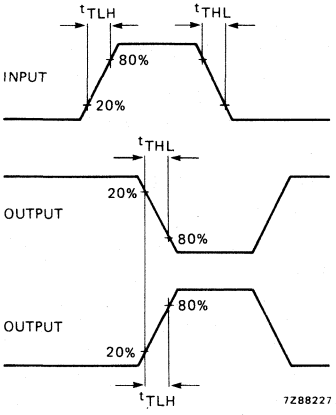


Fig. 5 Transition times (rise and fall times).

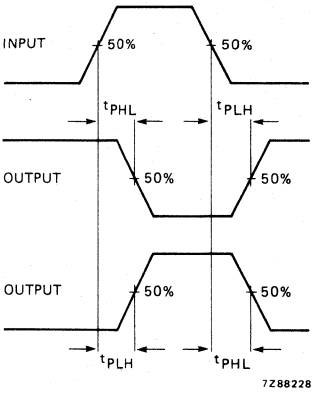


Fig. 6 Propagation delay times.

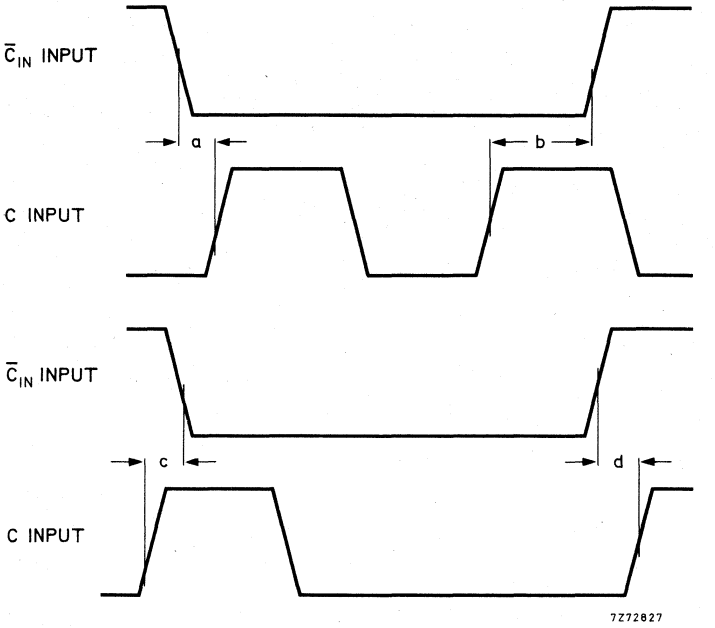


Fig. 7 Switching times waveforms (Set-up and hold).

(a) is the minimum time to wait to clock the counter after it has been enabled.

(b) is the minimum time that the counter may be clocked before it has been disabled.

(c) is the minimum time that a clock pulse may be applied with no effect on the state of the counter before it is enabled.

(d) is the minimum time to wait before a clock pulse may be applied with no effect on the state of the counter after it is disabled.

(b) and (c) may be negative numbers.

UNIVERSAL DECADE COUNTER

The GXB10137 is a high speed synchronous decade counter that can count up, count down, preset, or stop count at frequencies exceeding 100 MHz. The operation mode of the counter is programmed by three control lines (S_1, S_2 and $\overline{C}_{IN}$) as can be seen in the function select table. In the preset mode (loading step), a clock pulse is needed for the information present on the data inputs (D_0, D_1, D_2 and D_3) to be entered into the counter. $\overline{C}_{OUT}$ goes LOW on the terminal count. $\overline{C}_{OUT}$ is partially decoded from Q_1 and Q_2 directly, so in the preset mode the condition of $\overline{C}_{OUT}$ after the clock's positive excursion will depend on the condition of Q_1 and/or Q_2. The counter changes state only on the positive-going edge of the clock, so at any other time, any other input may change without any result (except for $\overline{C}_{OUT}$). The sequence for counting out of improper states is as shown in the state diagrams.
This binary counter can be used in many applications, such as in computing for high speed control processors and peripheral controllers.

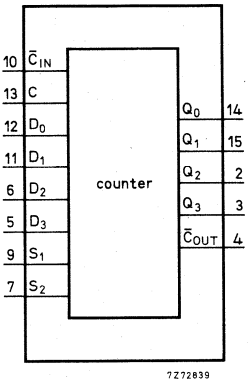


Fig. 1 Block diagram.

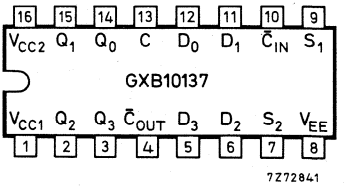


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 ± 10% V
Operating ambient temperature	T_{amb}		−30 to + 85 °C
Counting frequency	f_C	typ.	150 MHz
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package	P_{av}	typ.	625 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINE (see Package Outlines)

GXB10173P : plastic 16-lead dual in-line (SOT-38).
GXB10137D: ceramic 16-lead dual in-line (SOT-74).

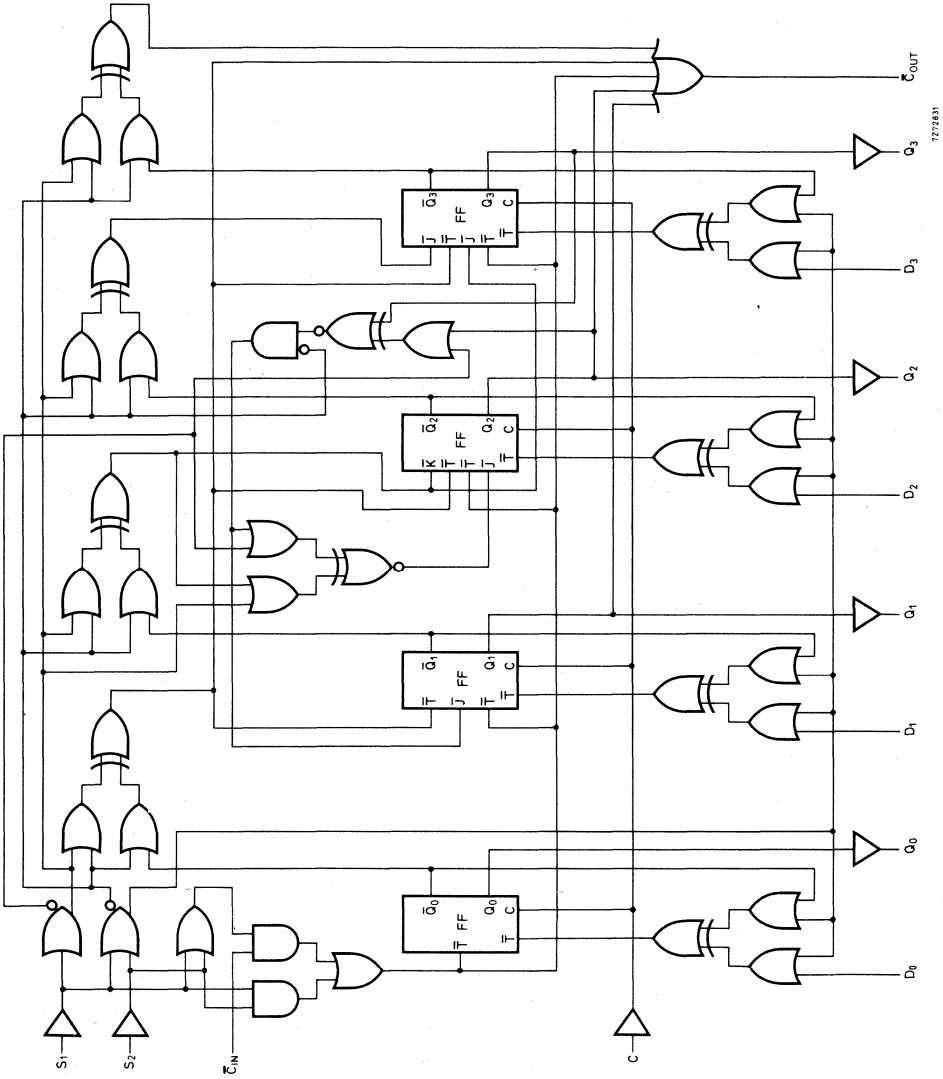


Fig. 3 Logic diagram.

Function select table

S_1	S_2	operating mode
L	L	preset (programme)
L	H	increment (count up)
H	L	decrement (count down)
H	H	hold (stop count)

Positive logic:

H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0
X = state is immaterial

Sequential function table

inputs								outputs				
S_1	S_2	D_0	D_1	D_2	D_3	$\overline{C}_{IN}$	C	Q_0	Q_1	Q_2	Q_3	$\overline{C}_{OUT}$
L	L	H	H	H	L	X	H	H	H	H	L	H
L	H	X	X	X	X	L	H	L	L	L	H	H
L	H	X	X	X	X	L	H	H	L	L	H	L
L	H	X	X	X	X	L	H	L	L	L	L	H
L	H	X	X	X	X	L	H	H	L	L	L	H
L	H	X	X	X	X	H	H	H	L	L	L	H
L	H	X	X	X	X	H	H	H	L	L	L	H
H	H	X	X	X	X	X	H	H	L	L	L	H
L	L	H	H	L	L	X	H	H	H	L	L	H
H	L	X	X	X	X	L	H	L	H	L	L	H
H	L	X	X	X	X	L	H	H	L	L	L	H
H	L	X	X	X	X	L	H	L	L	L	L	L

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = –5,2 V.

	symbol		pin under test	T_{amb} (°C) –30	+ 25	+ 85	unit	remarks
Input current HIGH	I_{IH}	max.	5,6,11,12	350	220	220	μA	
	I_{IH}	max.	9,10	390	245	245	μA	
	I_{IH}	max.	7	425	265	265	μA	
	I_{IH}	max.	13	460	290	290	μA	
Input current LOW	I_{IL}	min.	each data input	0,5	0,5	0,3	μA	
Supply current	I_{EE}	max.		165	150	165	mA	

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2{,}0$ V; $V_{EE} = -3{,}2$ V.

	symbol		T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Rise and fall propagation delay time							
C → Q	t_{PLH} / t_{PHL}	min.	0,8	1,0	1,4	ns	clock to output
		max.	4,8	4,5	5,0	ns	
C → $\overline{C_{OUT}}$	t_{PLH} / t_{PHL}	min.	2,0	2,5	2,4	ns	clock → carry out
		max.	10,9	10,5	11,5	ns	
$\overline{C_{IN}}$ → $\overline{C_{OUT}}$	t_{PLH} / t_{PHL}	min.	1,6	1,6	1,9	ns	carry in → carry out
		max.	7,4	6,9	7,5	ns	
Rise and fall transition time	t_{TLH} / t_{THL}	min.	0,9	1,1	1,1	ns	between 20% and 80%
		max.	3,3	3,3	3,5	ns	
Set-up time							
D → C	t_s	min.	3,5	3,5	3,5	ns	Fig. 6
S → C	t_s	min.	7,5	7,5	7,5	ns	
$\overline{C_{IN}}$ → C	t_s	min.	4,5	3,7	4,5	ns	Fig. 7a
C → $\overline{C_{IN}}$	t_s	min.	−1,0	−1,0	−1,0	ns	Fig. 7c
Hold time							
C → D	t_h	min.	0	0	0	ns	Fig. 6
C → S	t_h	min.	−2,5	−2,5	−2,5	ns	
C → $\overline{C_{IN}}$	t_h	min.	−1,6	−1,6	−1,6	ns	Fig. 7b
$\overline{C_{IN}}$ → C	t_h	min.	4,0	3,1	4,0	ns	Fig. 7d
Counting frequency							
count-up	$f_{c\,up}$	min.	125	125	125	MHz	
count-down	f_{cdown}	min.	125	125	125	MHz	

For **switching times test circuit** see Family Specifications.

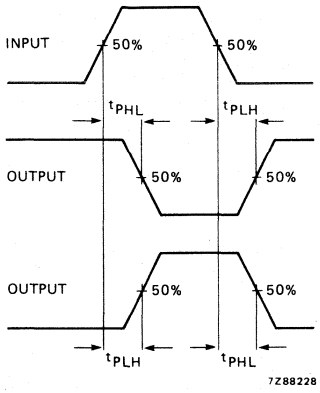


Fig. 4 Propagation delay times waveform.

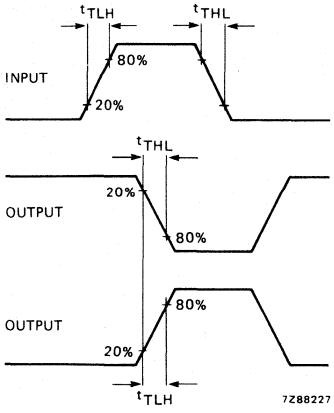


Fig. 5 Transition-times waveform (rise and fall times).

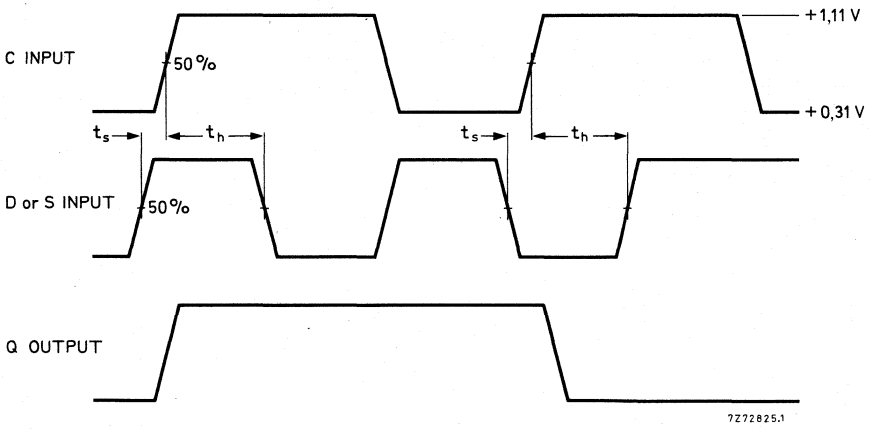


Fig. 6 Set-up and holding times waveform.

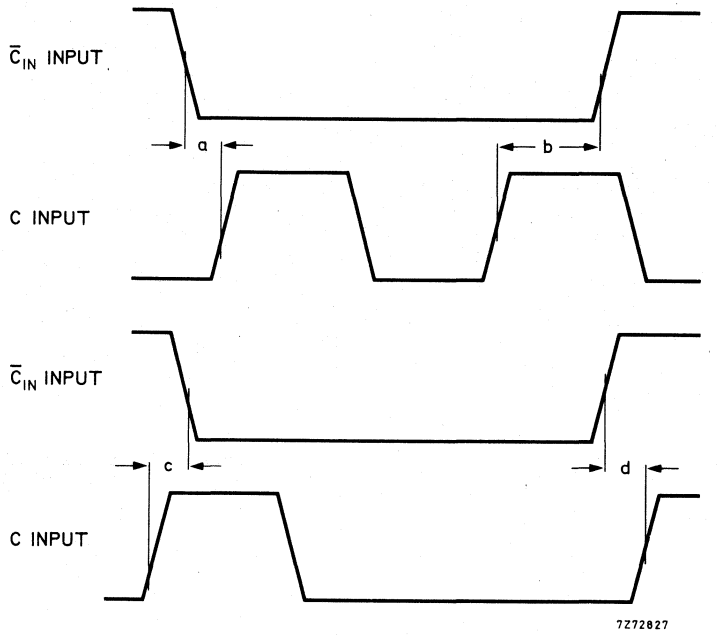


Fig. 7 Set-up and hold times waveform $\overline{C}_{IN} \rightarrow C$.

(a) is the minimum time to wait to clock the counter after it has been enabled.

(b) is the minimum time that the counter may be clocked before it has been disabled.

(c) is the minimum time that a clock pulse may be applied with no effect on the state of the counter before it is enabled.

(d) is the minimum time to wait before a clock pulse may be applied with no effect on the state of the counter after it is disabled.

(b) and (c) may be negative numbers.

4-BIT UNIVERSAL SHIFT REGISTER

The GXB10141 is a four-bit serial-parallel-in, serial-parallel-out shift register. Inputs S_1 and S_2 are used to determine the four possible functions of the register, these being no shift, shift right and parallel entrance of data with no external gating of the clock. The other inputs DL and DR are intended for shifting in from the left and the right, while inputs D_0 to D_3 are normal data inputs. All four outputs are capable of driving 50 Ω lines.

When the register is operating for serial output only, the unused outputs can be left open.

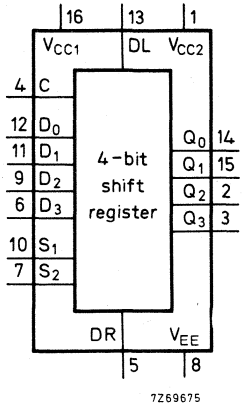


Fig. 1 Logic diagram.

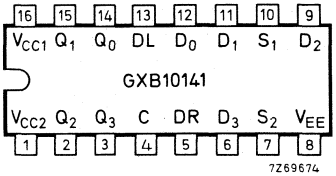


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 ± 10 % V
Operating ambient temperature range	T_{amb}		−30 to +85 °C
Shift frequency	f_{shift}	typ.	200 MHz
Output voltage			
HIGH state	V_{OH}	nom.	−880 V
LOW state	V_{OL}	nom.	−1720 V
Power consumption per package	P_{av}	typ.	425 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINE (see Package Outlines)

GXB10141P: plastic 16-lead dual in-line (SOT-38).
GXB10141D: ceramic 16-lead dual in-line (SOT-74).

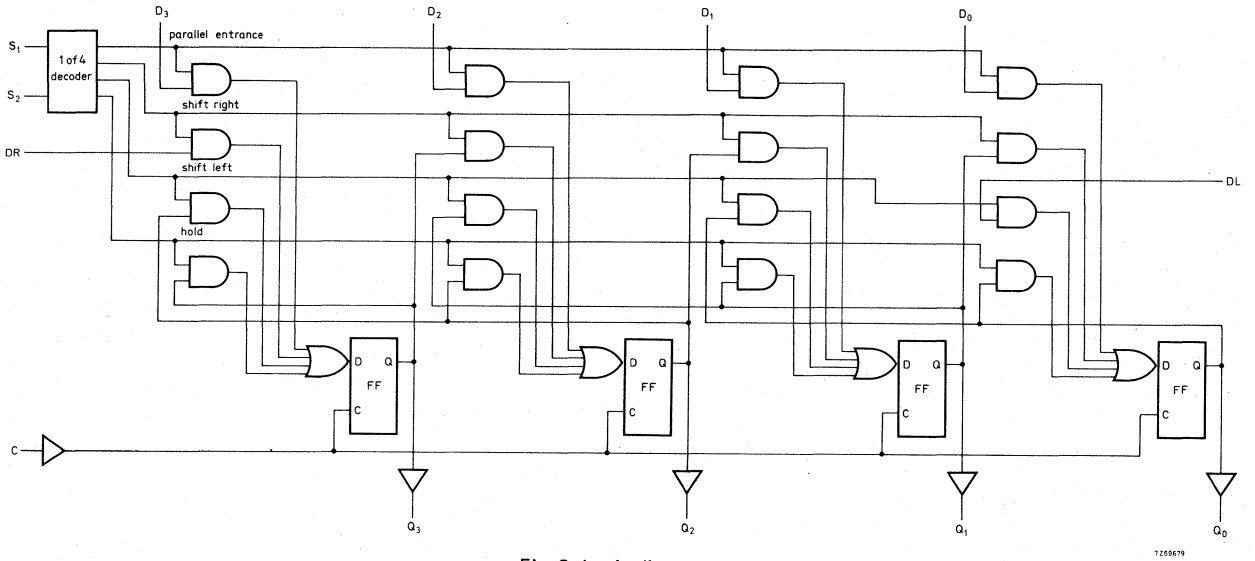


Fig. 3 Logic diagram.

FUNCTION TABLE

select inputs		operation mode	outputs			
S_1	S_2		$Q_{0(n+1)}$	$Q_{1(n+1)}$	$Q_{2(n+1)}$	$Q_{3(n+1)}$
L	L	parallel entrance	D_0	D_1	D_2	D_3
L	H	shift right*	Q_{1n}	Q_{2n}	Q_{3n}	DR
H	L	shift left*	DL	Q_{0m}	Q_{1n}	Q_{2n}
H	H	stop shift	Q_{0n}	Q_{1n}	Q_{2n}	Q_{3n}

Positive logic:

H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0

* Outputs as they exist after pulse at "C" input with conditions as shown.

Pulse is positive transition of clock (C) input.

RATINGS see Family Specifications

D.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = −5,2 V

	symbol		T_{amb} (°C) −30	+25	+85	unit	remarks
Input current HIGH							
pins 5,6,9,11,12,13	I_{IH}	max.	350	220	220	μA	
pins 7 and 10	I_{IH}	max.	390	245	245	μA	
pin 4	I_{IH}	max.	425	265	265	μA	
Input current LOW	I_{IL}	min.	0,5	0,5	0,3	μA	
Supply current (d.c.)	I_{EE}	max.	112	102	112	mA	

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = +2,0$ V; V_{EE} −3,2 V

	symbol		T_{amb} (°C) −35	+25	+85	unit	remarks
Propagation delay rise and fall times	t_{PLH}	min.	1,7	1,8	2,0	ns	see Figs 4 and 5
	$\overline{PHL}$	max.	3,9	3,8	4,2	ns	
Transition rise and fall times	t_{TLH}	min.	1,0	1,1	1,1	ns	
	$\overline{THL}$	max.	3,4	3,3	3,6	ns	
Set-up time							
D → C	t_{DSC}	min.	2,5	2,5	2,5	ns	
S_n → C	t_{SSC}	min.	5,5	5,0	5,5	ns	
Hold time							
C → D	t_{CHD}	min.	1,5	1,5	1,5	ns	
C → S_n	t_{CHS}	min.	1,5	1,5	1,5	ns	
Shift frequency	f_{shift}	min.	150	150	150	MHz	see Fig. 6

See also Family Specifications **Switching times test circuit and waveforms.**

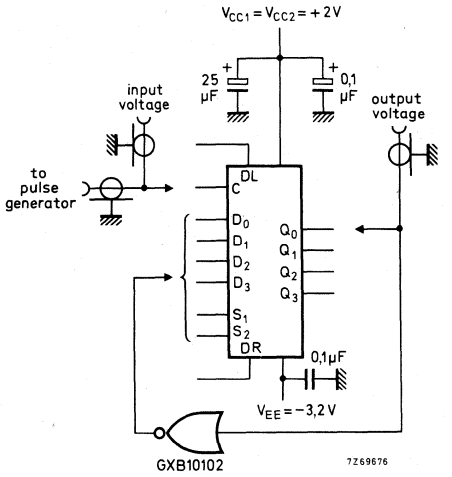


Fig. 4 Switching times test circuit.

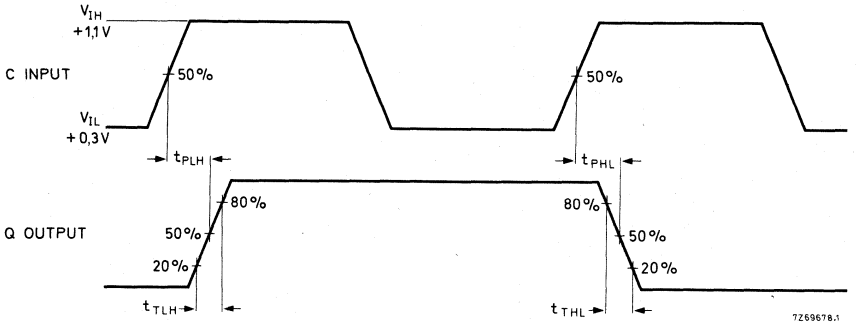


Fig. 5 Switching times waveforms.

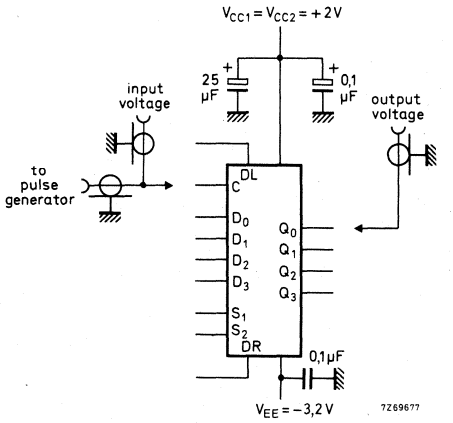


Fig. 6 Shift frequency test circuit.

Test procedure:

1. Set inputs D_1, D_2 and D_3 to LOW state (+0,3 V)
   D_0 to HIGH state (+1,1 V)
2. Apply clock pulse to C to set Q_0 in HIGH state.
3. Maintain clock input LOW.
   Set S_1 to LOW state (+0,3 V)
   S_2 to HIGH state (+1,1 V)
4. Test shift frequency.

64-BIT REGISTER FILE (RAM)

The GXB10145 is a 64-bit RAM organized as a 16 x 4 array. A chip enable input together with fully decoded inputs allow expansion of memory capacity. The chip enable input is combined with open emitter outputs also full wired-ORing and data bussing capability.

Input pull-down resistors (50 kΩ) allow the inputs to be left open is unused.

The GXB10145 is particularly yseful in register file or small scratchpad applications.

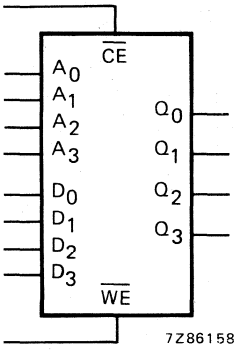


Fig. 1 Logic diagram.

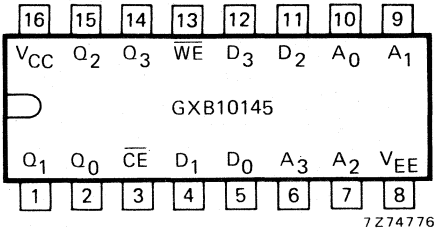


Fig. 2 Pin designation.

V_{CC} = 0 V (ground); V_{EE} = −5,2 V
Q_0 to Q_3 = Data outputs.
A_0 to A_3 = Address inputs;
D_0 to D_3 = Data inputs.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 ± 10 % V
Operating ambient temperature range	T_{amb}		0 to +75 °C
Average propagation delay	t_{PLH}	typ.	10 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_{av}	typ.	625 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (see Package Outlines)

GXB10145E: 16-lead DIL; metal-ceramic (SOT-84B).

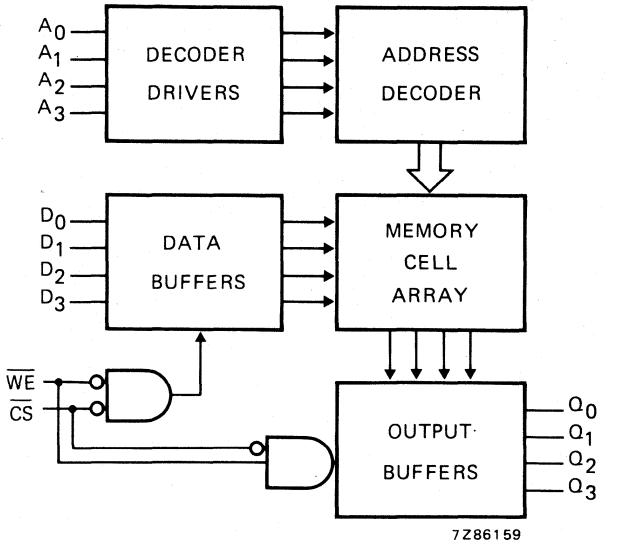


Fig. 3 Block diagram.

FUNCTION TABLE

mode	inputs			output
	$\overline{CE}$	$\overline{WE}$	D	Q
write "0"	L	L	L	L
write "1"	L	L	H	L
read	L	H	X	Q
disabled	H	X	X	L

Positive logic

1 = H = HIGH state (the more positive voltage)
0 = L = LOW state (the less positive voltage)
X = state is immaterial.

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = –5,2 V

	symbol		T_{amb} (°C) 0	+25	+75	unit	remarks
Input current HIGH							
pins 3,6,7,9,10	I_{IH}	max.	200	200	200	μA	
pins 4,5,11,12	I_{IH}	max.	220	220	220	μA	
pin 13	I_{IH}	max.	470	470	470	μA	
Input current LOW	I_{IL}	min.	0,5	0,5	0,3	μA	
Supply current	I_{EE}	typ.	–	120	–	mA	
		max.	165	150	165	mA	

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = +2{,}0$ V; $V_{EE} = -3{,}2$ V

	symbol		T_{amb} (°C) 0	+25	+75	unit	remarks
Read mode							
Chip enable							
access time	t_{ACE}	min.	2,0	2,0	2,0	ns	
recovery time	t_{RCE}	max.	8,0	8,0	8,0	ns	
Address							
access time	t_{AA}	min.	4,0	4,0	4,0	ns	
		max.	15,0	15,0	15,0	ns	
Write mode							
WE pulse duration	t_W	min.	11,0	12,0	16,0	ns	
Set-up times							
D → WE	t_{WSD}	min.	0	0	0	ns	see Fig. 5
CE → WE	t_{WSCE}	min.	5,5	5,5	5,5	ns	
A_n → WE	t_{WSA}	min.	5,3	5,3	5,3	ns	
Hold times							
WE → D	t_{WHD}	min.	4,5	4,5	4,5	ns	
WE → CE	t_{WHCE}	min.	4,5	4,5	4,5	ns	
WE → A_n	t_{WHA}	min.	5,3	5,3	5,3	ns	
Write							
recovery time	t_{WR}	max.	11,0	11,0	11,0	ns	
Chip enable mode							
CE pulse duration	t_{CE}	min.	11,0	11,0	11,0	ns	
Set-up times							
D → CE	t_{CESD}	min.	0	0	0	ns	see Fig. 4
WE → CE	t_{CESW}	min.	5,5	5,5	5,5	ns	
A_n → CE	t_{CESA}	min.	4,5	4,5	4,5	ns	
Hold times							
CE → D	t_{CEHD}	min.	4,5	4,5	4,5	ns	
CE → WE	t_{CEHW}	min.	4,5	4,5	4,5	ns	
CE → A_n	t_{CEHA}	min.	4,5	4,5	4,5	ns	
Transition	t_{TLH}	min.	1,1	1,1	1,1	ns	between 20 and 80%
	t_{THL}	max.	7,0	7,0	7,0	ns	

For **switching times test circuit** see Family Specifications.

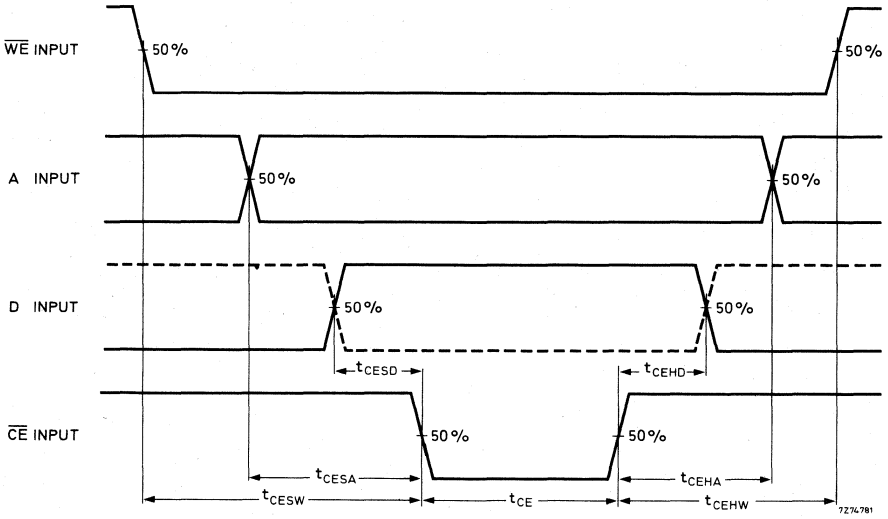


Fig. 4 Chip enable mode waveforms.

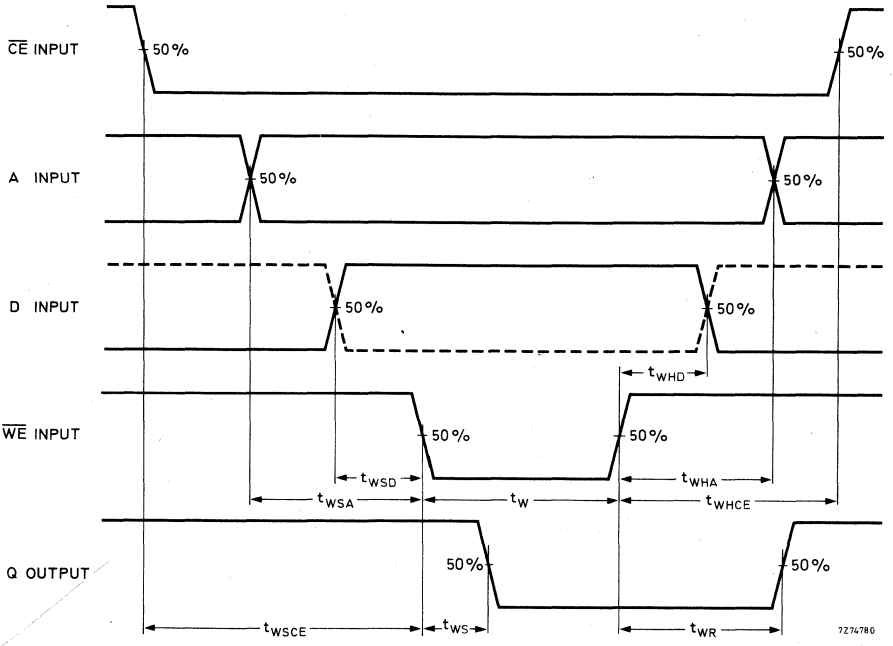


Fig. 5 Write mode waveforms.

FIELD PROGRAMMABLE READ-ONLY MEMORY

The 10149 is field programmable, meaning that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard device is supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix. The 10149 is suitable for use in high performance ECL systems. The outputs are capable of driving 50 Ω loads. A chip enable input is provided for ease of memory expansion.

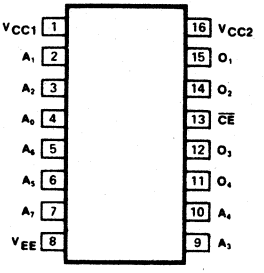
FEATURES

- Address access time: 20 ns max.
- Power dissipation: 0,66 mW/bit typ.
- High impedance inputs (50 kΩ pulldown)
- Open emitter outputs (50 Ω drive)
- On-chip address decoding
- No separate fusing pins
- Fully compatible with ECL 10K series

APPLICATIONS

- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

F PACKAGE*



*F = Cerdip

Fig. 1 Pin designation.

$V_{CC1} = V_{CC2} = 0V$ (ground); $V_{EE} = -5,2$ V

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 ± 5% V
Operating ambient temperature range	T_{amb}		−30 to +85 °C
Average propagation delay	t_{PHL}	typ.	2,0 ns
Output voltage			
HIGH state	V_{OH}	nom.	−890 mV
LOW state	V_{OL}	nom.	−1700 mV

FAMILY DATA see Family Specifications.

PACKAGE OUTLINE (see Package Outlines).

GXB10149D: 16 lead DIL; ceramic (SOT-74). Marking 10149F.

BLOCK DIAGRAM

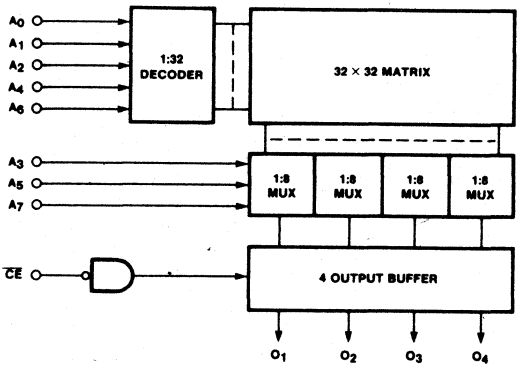


Fig. 2 Block diagram.

RATINGS see Family Specifications

D.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = −5,2 V

	symbol		T_{amb} (°C) −30	+ 25	+ 85	unit	remarks
Input current HIGH	I_{IH}	max.		265		μA	
Input current LOW	I_{IL}	min.	0,5	0,5	0,3	μA	
Supply current	I_{EE}	max.	–	150	–	mA	

PROGRAMMING PROCEDURE

The 10149 is shipped with all bits at logical "0" (LOW). To write logical "1", proceed as follows:

Set-up

a. Set V_{EE} and $\overline{CE}$ to GND.
b. Set V_{CC1} and V_{CC2} to V_{CCVH}.
c. Terminate all device outputs with a 1,8 KΩ resistor in series with a 5,6 KΩ resistor to GND.

PROGRAM-VERIFY SEQUENCE

1. Select the Address to be programmed, and raise V_{CC1} to V_{CCP}.
2. After t_D delay, apply a voltage V_{OPF} to the output to be programmed via the external divider (refer to typical programming circuit). Program one output at a time.
3. After t_p delay, remove V_{OPF} from the programmed output.
4. After t_D delay, repeat steps 2 and 3 to program other bits at the same address.
5. To verify programming of all bits at the same address, after t_D delay lower V_{CC1} and V_{CC2} to V_{CCVH}. All programmed outputs should remain in the logic HIGH state.
6. After t_D delay, repeat steps 1 through 5 to program and verify all other address locations.
7. After t_D delay lower V_{CC1} and V_{CC2} to V_{CCVL} and verify all memory locations by cycling through all device addresses.

PROGRAMMING SYSTEM SPECIFICATIONS

Testing of these limits may cause programming of device. T_{amb} = 25 °C.

parameter	symbol	min.	typ.	max.	unit	remarks
Power supply voltage to program	V_{CCP}	6,0	–	6,8	V	notes 1, 3
upper verify limit	V_{CCVH}	5,5	–	5,7	V	I_{CCP} = 150 ± 25 mA
lower verify limit	V_{CCVL}	4,7	–	4,9	V	I_{CCV} = 400 ± 50 mA
Threshold verify voltage	V_S		V_{CC} −1,3		V	note 2
Programming supply current	I_{CCP}	125	–	175	mA	V_{CCP} = 12 ± 0,5 V
Input voltage HIGH	V_{IH}	V_{CCV} −0,8	–	V_{CCV} −0,2	V	note 4
LOW	V_{IL}	V_{CCV} + 0	–	V_{CCV} +0,8	V	
Input current HIGH	I_{IH}	–	–	300	μA	$V_{IH} = V_{IHA}$
LOW	I_{IL}	–	–	−50	μA	$V_{IL} = V_{ILB}$
Forced output program voltage	V_{OPF}	6,0	–	6,8	V	I_{OPF} = 2,5 ± 0,5 mA notes 3, 5
Forced output program current	I_{OPF}	2,0	–	3,0	mA	V_{OPF} = 6,4 ± 0,4 V
Transition time rise output pulse	t_{TLH}	0,1	–	1,0	μs	
Programming pulse width	t_P	100	–	125	μs	
Verify time	t_V	1	–	–	μs	
Address program-verify cycle	t_{PVA}	–	–	1	ms	
Memory program-verify time	t_{PVM}	–	–	20	s	continuous
Fusing attempts (per link)	F_L	–	–	1	cycle	

PROGRAMMING NOTES

1. Bypass V_{CC} to GND with a 0,01 μF capacitor to reduce voltage spikes.
2. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. This voltage should be maintained within specified limits during the entire fusing cycle. For a transient current of 150 mA, limit voltage spikes to a maximum slew rate of 2 V/μs, and 10 μs maximum recovery.
4. Address buffers must be referenced to the V_{CCV} supply.
5. V_{OPF} supply must be referenced to the V_{CCV} supply.

2x 8 CONTENT ADDRESSABLE MEMORY (CAM)

The 10155 is a 16-bit ECL Content Addressable Memory (CAM) organized as an array of 8 words by 2 bits. Each cell of the array consists of a D-type latch and an exclusive-OR comparator, along with control logic for reading, writing and masking.

FEATURES

- 12 ns associate time (max.)
- Linear address select
- Single bit masking
- 50 Ω output drive
- ECL 10K compatible
- Open emitter match lines for easy bit expansion
- 50 kΩ input pulldown resistors (except on Y lines)

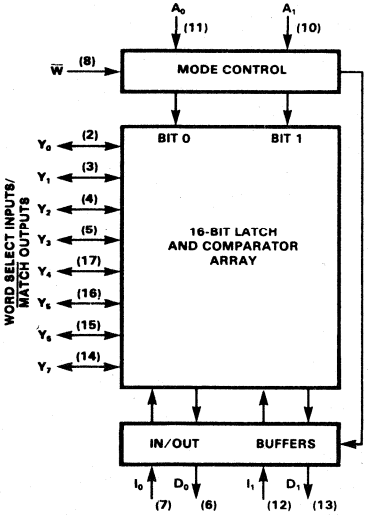
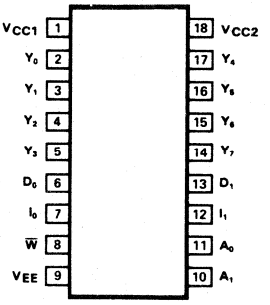


Fig. 1 Block diagram.

F,N PACKAGE*



*F = Cerdip
N = Plastic

Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	−5,2 ± 5% V
Operating ambient temperature range	T_{amb}	−30 to + 85 °C
Output voltage		
HIGH state	V_{OH}	nom. −880 mV
LOW state	V_{OL}	nom. −1720 mV

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES

GXB10155D: 18-lead DIL; ceramic. Marking 10155F.
GXB10155P : 18-lead DIL; plastic. Marking 10155N.

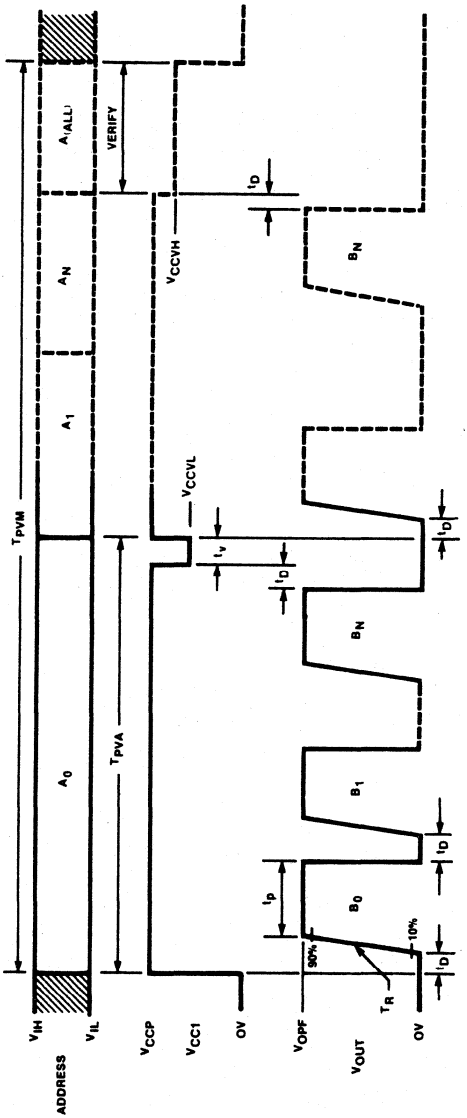


Fig. 6 Programming sequence.

PROGRAMMING PROCEDURE

The 10149 is shipped with all bits at logical "0" (LOW). To write logical "1", proceed as follows:

Set-up

a. Set V_{EE} and $\overline{CE}$ to GND.
b. Set V_{CC1} and V_{CC2} to V_{CCVH}.
c. Terminate all device outputs with a 1,8 KΩ resistor in series with a 5,6 KΩ resistor to GND.

PROGRAM-VERIFY SEQUENCE

1. Select the Address to be programmed, and raise V_{CC1} to V_{CCP}.
2. After t_D delay, apply a voltage V_{OPF} to the output to be programmed via the external divider (refer to typical programming circuit). Program one output at a time.
3. After t_p delay, remove V_{OPF} from the programmed output.
4. After t_D delay, repeat steps 2 and 3 to program other bits at the same address.
5. To verify programming of all bits at the same address, after t_D delay lower V_{CC1} and V_{CC2} to V_{CCVH}. All programmed outputs should remain in the logic HIGH state.
6. After t_D delay, repeat steps 1 through 5 to program and verify all other address locations.
7. After t_D delay lower V_{CC1} and V_{CC2} to V_{CCVL} and verify all memory locations by cycling through all device addresses.

PROGRAMMING SYSTEM SPECIFICATIONS

Testing of these limits may cause programming of device. T_{amb} = 25 °C.

parameter	symbol	min.	typ.	max.	unit	remarks
Power supply voltage to program	V_{CCP}	6,0	–	6,8	V	notes 1, 3
upper verify limit	V_{CCVH}	5,5	–	5,7	V	I_{CCP} = 150 ± 25 mA
lower verify limit	V_{CCVL}	4,7	–	4,9	V	I_{CCV} = 400 ± 50 mA
Threshold verify voltage	V_S		V_{CC} −1,3		V	note 2
Programming supply current	I_{CCP}	125	–	175	mA	V_{CCP} = 12 ± 0,5 V
Input voltage HIGH	V_{IH}	V_{CCV} −0,8	–	V_{CCV} −0,2	V	note 4
LOW	V_{IL}	V_{CCV} + 0	–	V_{CCV} +0,8	V	
Input current HIGH	I_{IH}	–	–	300	μA	$V_{IH} = V_{IHA}$
LOW	I_{IL}	–	–	−50	μA	$V_{IL} = V_{ILB}$
Forced output program voltage	V_{OPF}	6,0	–	6,8	V	I_{OPF} = 2,5 ± 0,5 mA; notes 3, 5
Forced output program current	I_{OPF}	2,0	–	3,0	mA	V_{OPF} = 6,4 ± 0,4 V
Transition time rise output pulse	t_{TLH}	0,1	–	1,0	μs	
Programming pulse width	t_P	100	–	125	μs	
Verify time	t_V	1	–	–	μs	
Address program-verify cycle	t_{PVA}	–	–	1	ms	
Memory program-verify time	t_{PVM}	–	–	20	s	continuous
Fusing attempts (per link)	F_L	–	–	1	cycle	

PROGRAMMING NOTES

1. Bypass V_{CC} to GND with a 0,01 μF capacitor to reduce voltage spikes.
2. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. This voltage should be maintained within specified limits during the entire fusing cycle. For a transient current of 150 mA, limit voltage spikes to a maximum slew rate of 2 V/μs, and 10 μs maximum recovery.
4. Address buffers must be referenced to the V_{CCV} supply.
5. V_{OPF} supply must be referenced to the V_{CCV} supply.

2x 8 CONTENT ADDRESSABLE MEMORY (CAM)

The 10155 is a 16-bit ECL Content Addressable Memory (CAM) organized as an array of 8 words by 2 bits. Each cell of the array consists of a D-type latch and an exclusive-OR comparator, along with control logic for reading, writing and masking.

FEATURES

- 12 ns associate time (max.)
- Linear address select
- Single bit masking
- 50 Ω output drive
- ECL 10K compatible
- Open emitter match lines for easy bit expansion
- 50 kΩ input pulldown resistors (except on Y lines)

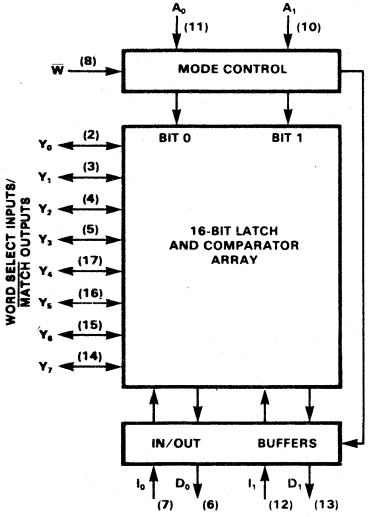
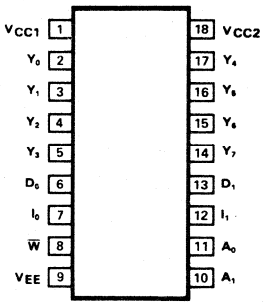


Fig. 1 Block diagram.

F,N PACKAGE*



*F = Cerdip
N = Plastic

Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	−5,2 ± 5% V
Operating ambient temperature range	T_{amb}	−30 to + 85 °C
Output voltage		
HIGH state	V_{OH}	nom. −880 mV
LOW state	V_{OL}	nom. −1720 mV

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES

GXB10155D: 18-lead DIL; ceramic. Marking 10155F.
GXB10155P : 18-lead DIL; plastic. Marking 10155N.

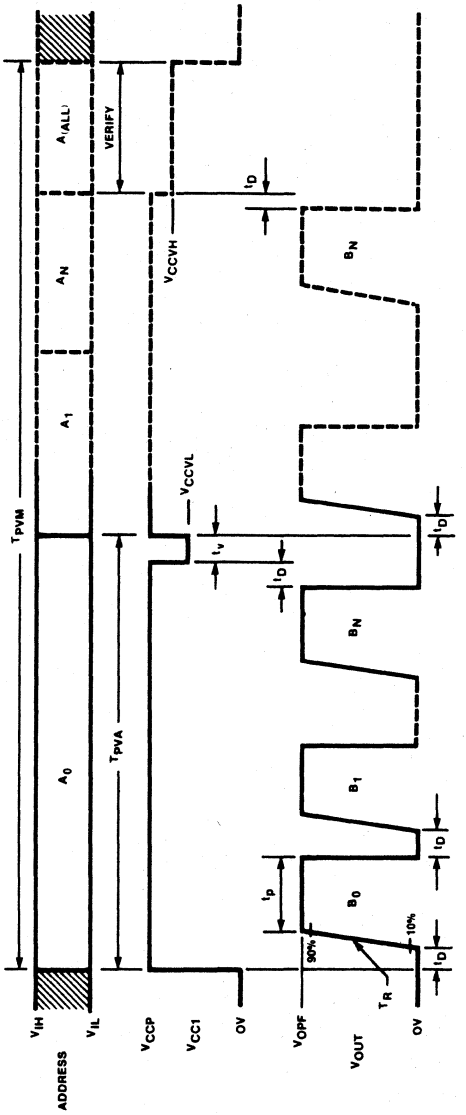


Fig. 6 Programming sequence.

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 0$ V, $V_{EE} = -5{,}2$ V, $R_L = 50\ \Omega$ to -2 V

	symbol		T_{amb} (°C) −30	+ 25	+ 85	unit	remarks
Input current HIGH		max.			220	μA	$A = V_{IHA}$
	I_{IH}	max.			200	μA	$I, W = V_{IHA}$
		max.			50	μA	$Y = V_{IHA}$
Input current LOW	I_{IL}	min.	0,5	0,5	0,3	μA	$A, I, W = V_{ILB}$
Supply current	I_{EE}	max.	–	–	140	mA	$V_I = V_{IHA}$

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = +2{,}0$ V; $V_{EE} = -3{,}2$ V; $R_L = 50\ \Omega$ to ground. Typical values at $T_{amb} = 25$ °C.

parameter	from	to	test conditions	limits min.	typ.	max.	unit
Associate time							ns
T_{A1}	I±	Y±			8	12	
T_{A2}	A±	Y±			9	12	
Disable time							ns
T_{D1}	A–	Y–			8	12	
T_{D2}	A+	D–			4	7	
T_{D3}	Y+	D–			9	13	
Set-up and hold time							ns
T_{H1} Hold time	$\overline{W}$+	A+		1	0		
T_{S2} Set-up time	A–	Y–		15	11		
T_{H2} Hold time	$\overline{W}$+	Y±		3	1		
T_{S3} Set-up time	Y+	$\overline{W}$–		3	2		
T_{H3} Hold time	$\overline{W}$+	I±		3	1		
T_{S4} Set-up time	I±	$\overline{W}$±		5	3		

X = Don't care
Q_{n0} = Contents of address n, Bit 0 (n = 0 to 7)
Q_{n1} = Contents of address n, Bit 1

Notes of page 2.
1. 1 (high) = Mismatch, 0 (low) = Match
2. Read mode: $D_0 = Q_{00} \bullet \overline{Y_0} + Q_{10} \bullet \overline{Y_1} + \bullet\bullet\bullet + Q_{70} \bullet \overline{Y_7}$
   $D_1 = Q_{01} \bullet \overline{Y_0} + Q_{11} \bullet \overline{Y_1} \bullet\bullet\bullet + Q_{71} \bullet \overline{Y_7}$
3. In normal operation a single Y address is selected for read or write
4. Write is transparent
5. Simultaneous Associate and Write at all "Match" addresses

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = +2$ V, $V_{EE} = -3{,}2$ V, $R_L = 50\ \Omega$ to ground

parameter		from	to	test conditions	limits			unit
					min.	typ.	max.	
T_W	Write pulse width				10	5		ns
	Access time							ns
T_{A3}	Write	$\overline{W}-$	D±	$T_{S4} \geqslant T_W$		13	17	
T_{A4}	Write	I+,–	D+,–			9	13	
T_{A5}	Read	Y–	D+			6	10	
T_{A6}	Read	A–	D+			4		

ASSOCIATE TIME I TO Y (T_{A1})

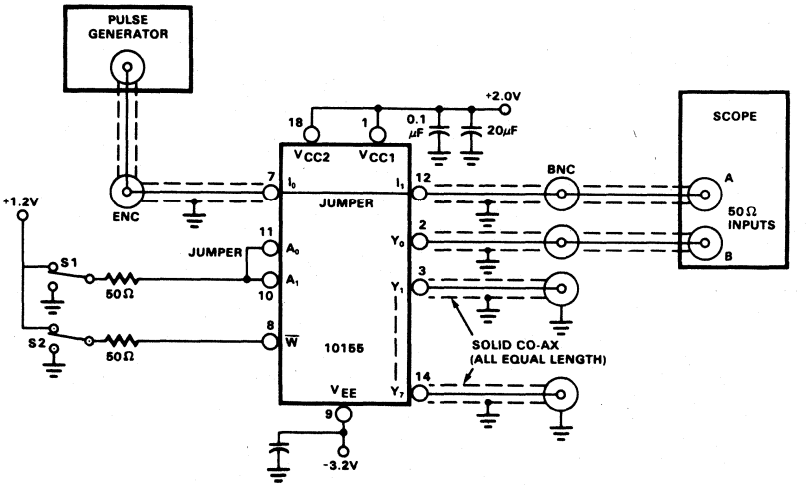
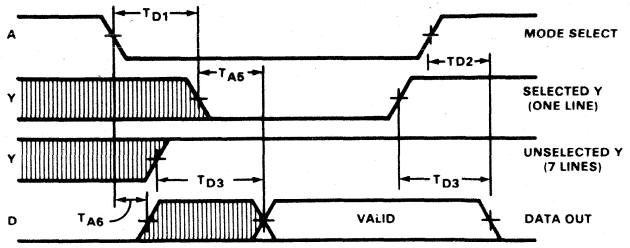


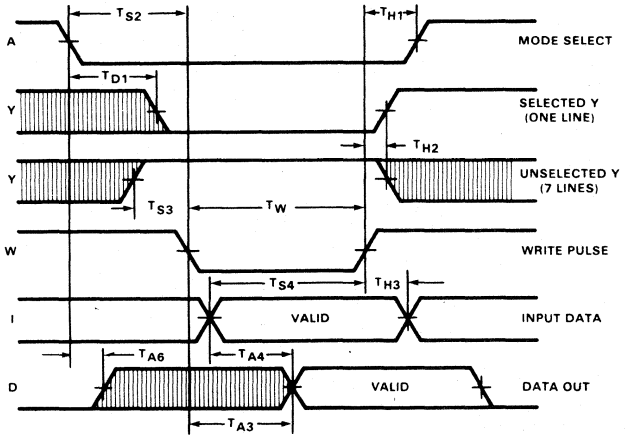
Fig. 4 Switching times test circuit.

VOLTAGE WAVEFORMS

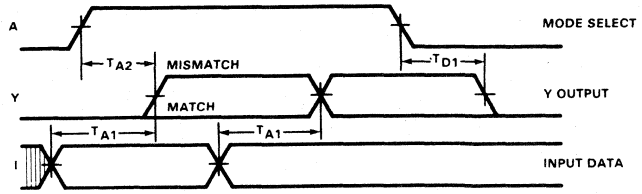
READ CYCLE



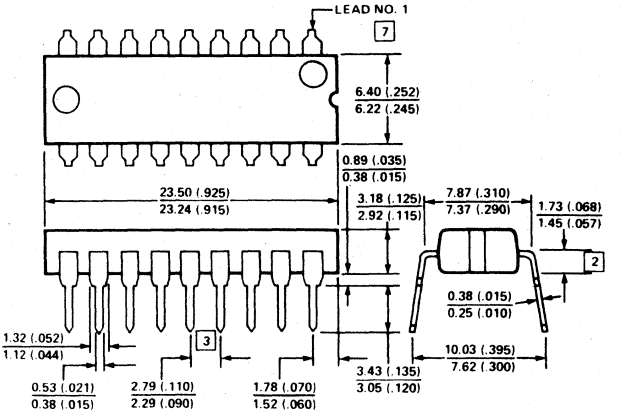
WRITE CYCLE



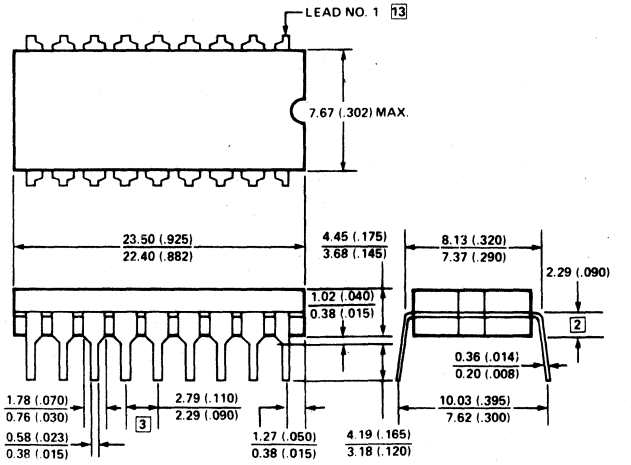
ASSOCIATE CYCLE



NK Package



FK Package



QUADRUPLE 2-TO-1 MULTIPLEXER

The GXB10158 is a high speed, low power, quadruple 2-to-1 multiplexer. With respect to a single control signal it transmits to a common output pin the data present on either of two input pins. As contrasted with the GXB10159 the GXB10158 has no enable input and non-inverting outputs. It includes high-impedance input pull-down resistors and open emitter outputs.

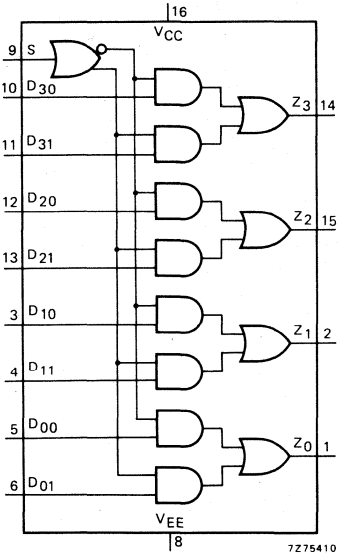


Fig. 1 Logic diagram.

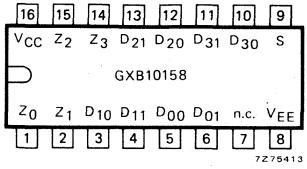


Fig. 2 Pin designation.

V_{CC} = 0 V (ground); V_{EE} = −5,2 V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	−5,2 ± 10%	V
Operating ambient temperature range	T_{amb}	−30 to +85	°C
Average propagation delay: data to output	t_{PLH}	typ. 2,2	ns
select to output	t_{PLH}	typ. 3,0	ns
Output voltage			
HIGH state	V_{OH}	nom. −880	mV
LOW state	V_{OL}	nom. −1720	mV
Power consumption per package (no load)	P_{av}	typ. 162	mW

For **FAMILY DATA** see Family Specifications.

PACKAGE OUTLINES (see Package Outlines)

GXB10158P: 16-lead DIL; plastic (SOT-38Z).
GXB10158D: 16-lead DIL; ceramic (SOT-74).

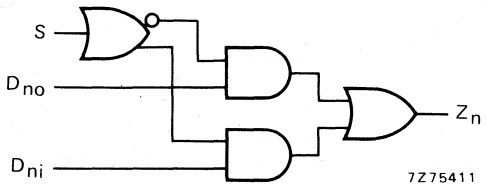


Fig. 3 Logic function (one multiplexer).

FUNCTION TABLE

inputs			output
D_{no}	D_{ni}	S	Z_n
L	X	L	L
H	X	L	H
X	L	H	L
X	H	H	H

Positive logic

H = HIGH state
(the more positive voltage) = 1

L = LOW state
(the less positive voltage) = 0

X = state is immaterial

RATINGS see Family Specifications

D.C. CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground; V_{EE} = −5,2 V

	symbol		T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Input current HIGH	I_{IH}	max.	400	250	250	μA	
Input current LOW	I_{IL}	min.	0,5	0,5	0,3	μA	
Supply current	I_{EE}	max.	53	48	53	mA	

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = 2 V; V_{EE} = −3,2 V; input pulse condition $t_{TLH} = t_{THL}$ = 2 ns ± 0,2.

	symbol		T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) −85	unit	remarks
Rise and fall propagation delay times	$\frac{t_{PLH}}{t_{PHL}}$						
D → Q		min.	1,3	1,2	1,3	ns	data to output
		max.	3,1	3,0	3,2	ns	
S → Q		min.	2,5	2,4	2,5	ns	select to output
		max.	4,8	4,5	4,8	ns	
Transition rise and fall times	$\frac{t_{TLH}}{t_{THL}}$	min.	1,6	1,5	1,6	ns	between 20 and 80%
		max.	3,4	3,3	3,4	ns	

For **switching times test circuit** and **waveform** see Family Specifications.

QUADRUPLE 2-TO-1 MULTIPLEXER

The GXB10159 is a high speed, low power, quadruple 2-to-1 multiplexer. With respect to a single control signal it transmits to a common output pin the data present on either of two input pins. As contrasted with the GXB10158 the GXB10159 has a common enable input and inverting outputs. It includes high-impedance input pull-down resistors and open emitter outputs.

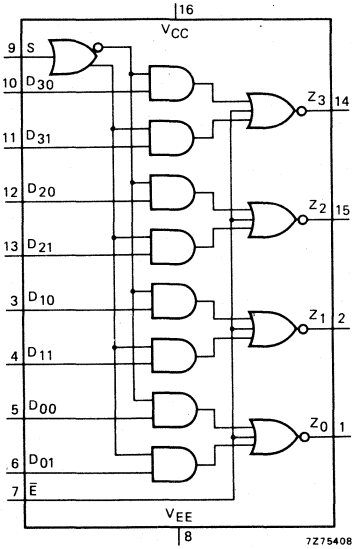


Fig. 1 Logic diagram.

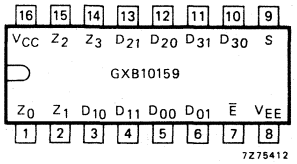


Fig. 2 Pin designation.

V_{CC} = 0 V (ground); V_{EE} = −5,2 V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 ± 10%	V
Operating ambient temperature range	T_{amb}		−30 to +85	°C
Average propagation delay: data to output	t_{PLH}	typ.	2,2	ns
select to output	t_{PLH}	typ.	3,3	ns
Output voltage				
HIGH state	V_{OH}	nom.	−880	mV
LOW state	V_{OL}	nom.	−1720	mV
Power consumption per package (no load)	P_{av}	typ.	162	mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (see Package Outlines)

GXB10159P: 16-lead DIL; plastic (SOT-38Z).
GXB10159D: 16-lead DIL; ceramic (SOT-74).

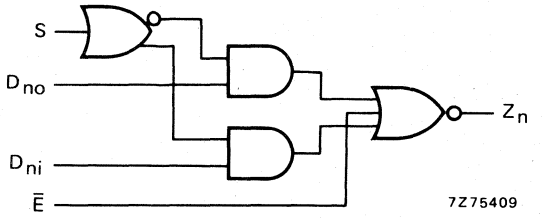


Fig. 3 Logic diagram (one multiplexer).

FUNCTION TABLE

inputs				output
D_{no}	D_{ni}	S	$\bar{E}$	Z_n
X	X	X	H	L
L	X	L	L	H
H	X	L	L	L
X	L	H	L	H
X	H	H	L	L

Positive logic

H = HIGH state
(the more positive voltage) = 1
L = LOW state
(the less positive voltage) = 0
X = state is immaterial

RATINGS see Family Specifications

D.C. CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground; $V_{EE} = -5{,}2$ V

	symbol		T_{amb} (°C)			unit	remarks
			−30	+25	+85		
Input current HIGH	I_{IH}	max.	400	250	250	μA	
Input current LOW	I_{IL}	min.	0,5	0,5	0,3	μA	
Supply current	I_{EE}	max.	58	53	58	mA	

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2$ V; $V_{EE} = -3{,}2$ V; input pulse condition $t_{TLH} = t_{THL} = 2$ ns ± 0,2.

	symbol	T_{amb} (°C)						unit	remarks
		−30		+25		+85			
		min.	max.	min.	max.	min.	max.		
Rise and fall propagation delay times	t_{PLH} / t_{PHL}								
D → Q		1,1	3,8	1,2	3,3	1,1	3,8	ns	
S → Q		1,5	5,3	1,5	5,0	1,5	5,3	ns	
$\bar{E}$ → Q		1,4	5,3	1,5	5,0	1,4	5,3	ns	
Rise and fall transition times	t_{TLH} / t_{THL}	1,0	3,7	1,1	4,5	1,0	5,0	ns	between 20% and 80%

For **switching times test circuit** and **waveforms** see Family Specifications.

12-BIT PARITY CHECKER/GENERATOR

The GXB10160 is a 12-bit parity checker or generator. The output goes HIGH when an odd number of inputs are HIGH. If parity detection or generation is required for less than 12 bits, the unused inputs can be left open (50 kΩ input pull-down resistors).

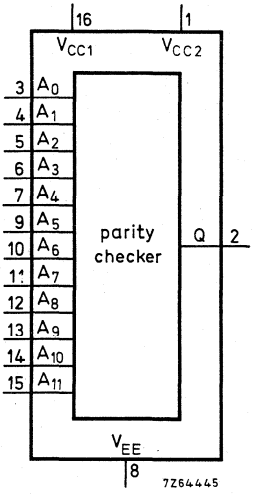


Fig. 1 Logic diagram.

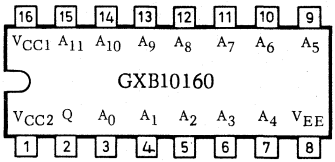


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 ± 10 % V
Operating ambient temperature range	T_{amb}		−30 to +85 °C
Average propagation delay	t_{PLH}	typ.	4,5 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package	P_{av}	typ.	310 mW

For **FAMILY DATA** see Family Specifications.

PACKAGE OUTLINE (see Package Outlines)

GXB10160P: plastic 16-lead dual in-line (SOT-38).
GXB10160D: ceramic 16-lead dual in-line (SOT-74).

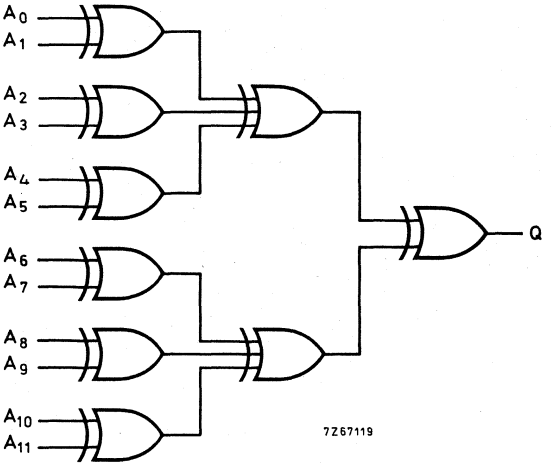


Fig. 3 Logic function.

FUNCTION TABLE

sum of inputs at HIGH state	Q
odd	H
even	L

positive logic:

HIGH state = 1
LOW state = 0

$$Q = A_0 \oplus A_1 \oplus A_2 \oplus A_3 \oplus A_4 \oplus A_5 \oplus A_6 \oplus A_7 \oplus A_8 \oplus A_9 \oplus A_{10} \oplus A_{11}.$$

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground; $V_{EE} = -5{,}2$ V

	symbol		T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Input currents HIGH	I_{IH}	max.	425	265	265	μA	
Input current LOW	I_{IL}	min.	0,5	0,5	0,3	μA	
Supply current	I_{EE}	max.	86	78	86	mA	

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2$ V; $V_{EE} = -3{,}2$ V

	symbol		−30	+25	+85	unit	remarks
Rise and fall propagation delay times	$\overline{t_{PLH}}$	min.	1,8	2,0	2,0	ns	
	t_{PHL}	max.	8,1	7,5	8,0	ns	
Transition times	t_{TLH}	min.	1,1	1,1	1,0	ns	between 20% and 80%
	t_{THL}	max.	3,5	3,3	3,5	ns	between 20% and 80%

For **switching times test circuit** and **waveforms** see Family Specifications.

THREE-BIT DECODER

one of eight lines LOW

The GXB10161 is a three-bit decoder with two enable inputs.

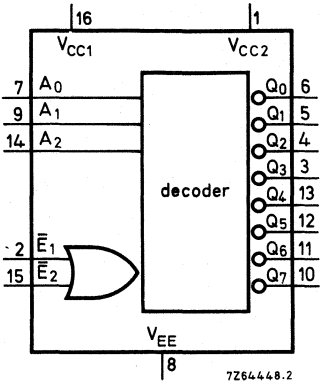


Fig. 1 Logic diagram.

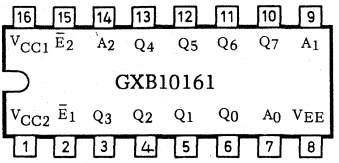


Fig. 2 Pin designation.
$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	$-5{,}2 \pm 10\%$	V
Operating ambient temperature range	T_{amb}	-30 to $+85$	°C
Average propagation delay	t_{PLH} typ.	4,0	ns
Output voltage			
HIGH state	V_{OH} nom.	-880	mV
LOW state	V_{OL} nom.	-1720	mV
Power consumption per package	P_{av} typ.	330	mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINE (see Package Outlines)

GXB10161P : plastic 16-lead dual in-line.
GXB10161D: ceramic 16-lead dual in-line.

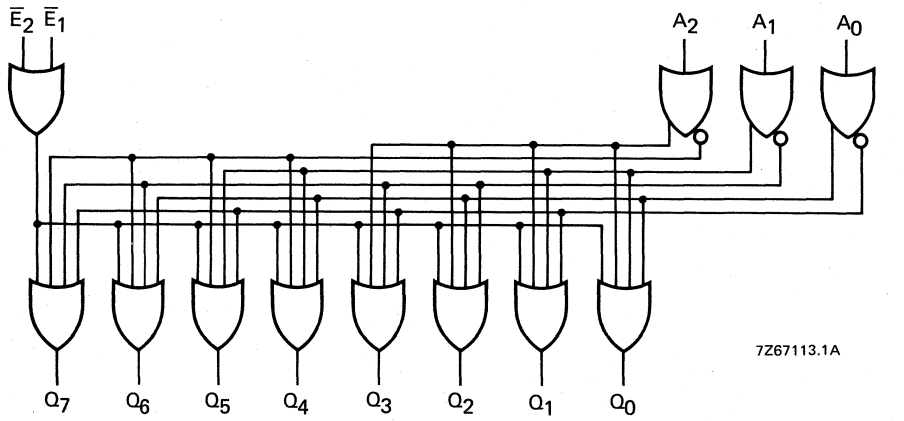


Fig. 3 Logic function.

A_0 to A_2: binary inputs; $\overline{E}_1$; $\overline{E}_2$: enable inputs; Q_0 to Q_7: decoded outputs.

FUNCTION TABLE

enable inputs		binary inputs			decimal outputs							
$\overline{E}_1$	$\overline{E}_2$	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
H	H	X	X	X	H	H	H	H	H	H	H	H
L	H	X	X	X	H	H	H	H	H	H	H	H
H	L	X	X	X	H	H	H	H	H	H	H	H
L	L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	L	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	L	H	H	H	L	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L

positive logic: H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

HIGH state = 1
LOW state = 0

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground; $V_{EE} = -5{,}2$ V

	symbol		T_{amb} (°C) −30	+ 25	+ 85	unit	remarks
Input currents HIGH	I_{IH}	max.	350	220	220	μA	
Input current LOW	I_{IL}	min.	0,5	0,5	0,3	μA	
Supply current	I_{EE}	max.	84	76	84	mA	

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2$ V; $V_{EE} = -3{,}2$ V

	symbol		T_{amb} (°C) −30	+ 25	+ 85	unit	remarks
Rise and fall propagation delay times	t_{PLH}	min.	1,5	1,5	1,5	ns	
	$\overline{t_{PHL}}$	max.	6,2	6,0	6,4	ns	
Transition rise and fall time	t_{TLH}	min.	1,0	1,1	1,1	ns	between
	$\overline{t_{THL}}$	max.	3,3	3,3	3,5	ns	20% and 80%

For **switching times waveforms** see Family Specifications.

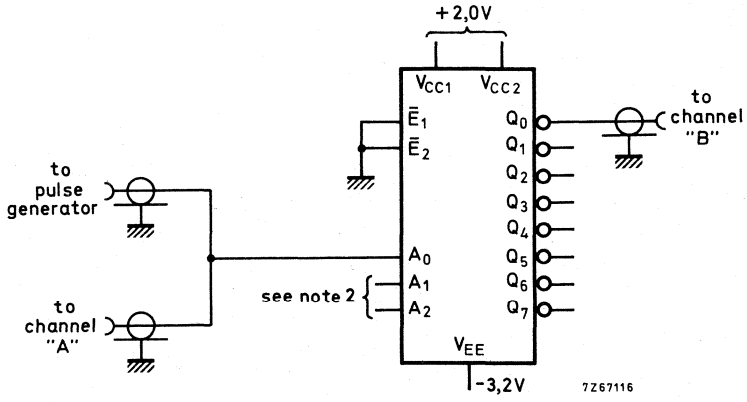


Fig. 4 Switching times test circuit.

THREE-BIT DECODER

one of eight lines HIGH

The GXB10162 is a three-bit decoder with two enable inputs.

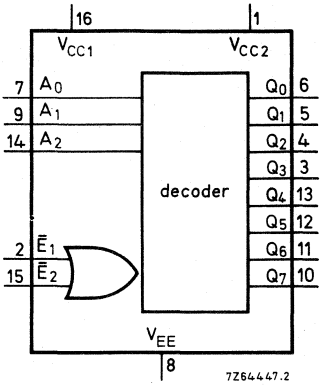


Fig. 1 Logic diagram.

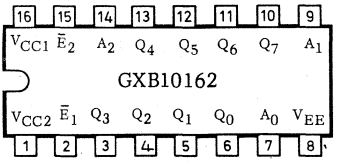


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 ± 10% V
Operating ambient temperature range	T_{amb}		−30 to + 85 °C
Average propagation delay	t_{PLH}	typ.	4,0 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumtpion per package	P_{av}	typ.	330 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINE (see Package Outlines)

GXB10162P : plastic 16-lead dual in-line (SOT-38).
GXB10162D: ceramic 16-lead dual in-line (SOT-74).

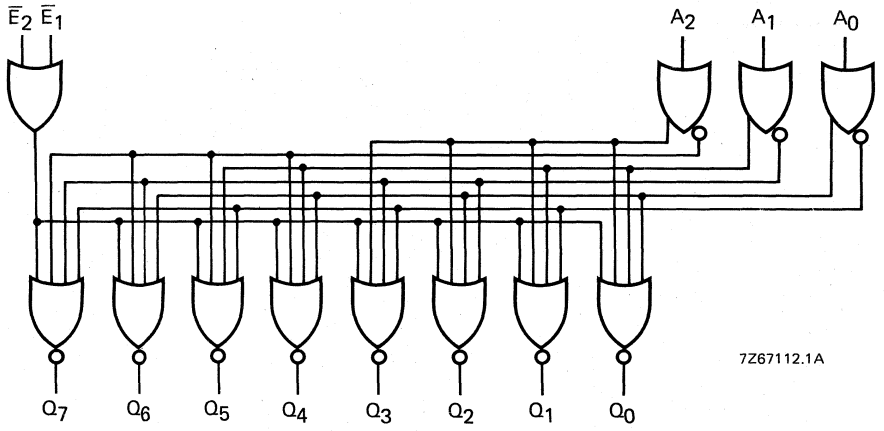


Fig. 3 Logic function.

A_0 to A_2: binary inputs; $\overline{E}_1$; $\overline{E}_2$: enable inputs; Q_0 to Q_7: decoded outputs.

FUNCTION TABLE

enable inputs		binary inputs			decimal outputs							
$\overline{E}_1$	$\overline{E}_2$	A_0	A_1	A_3	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
H	H	X	X	X	L	L	L	L	L	L	L	L
L	H	X	X	X	L	L	L	L	L	L	L	L
H	L	X	X	X	L	L	L	L	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	H	H	L	L	L	L	H	L	L	L	L
L	L	L	L	H	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	L	H	H	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H

positive logic: H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

HIGH state = 1
LOW state = 0

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = −5,2 V.

	symbol		T_{amb} (°C) −30	+ 25	+ 85	unit	remarks
Input current HIGH	I_{IH}	max.	350	220	220	μA	
Input current LOW	I_{IL}	min.	0,5	0,5	0,3	μA	
Supply current	I_{EE}	max.	84	76	84	mA	

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = 2 V; V_{EE} = −3,2 V

	symbol		T_{amb} (°C) −30	+ 25	+ 85	unit	remarks
Rise and fall propagation delay times	t_{PLH}	min.	1,5	1,5	1,5	ns	
	t_{PHL}	max.	6,2	6,0	6,4	ns	
Transition rise and fall time	t_{TLH}	min.	1,0	1,1	1,1	ns	between
	t_{THL}	max.	3,3	3,3	3,5	ns	20% and 80%

For **switching times waveforms** see Family Specifications.

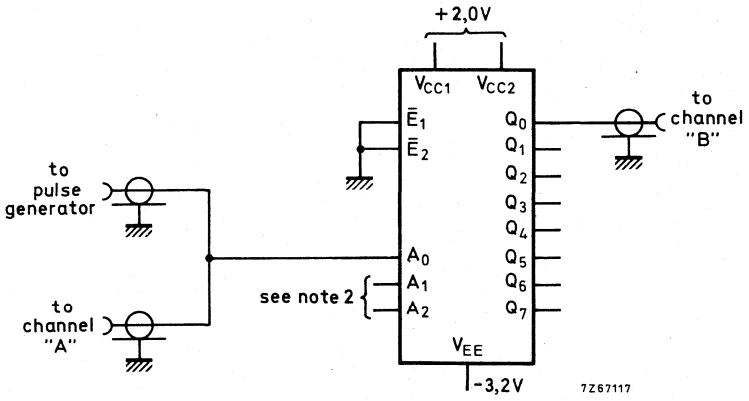


Fig. 4 Switching times test circuit.

EIGHT-INPUT MULTIPLEXER

The GXB10164 performs 8-input multiplexing with enable input. The output goes LOW when not enabled, thus permitting expansion of multiplexers by wired-ORing.

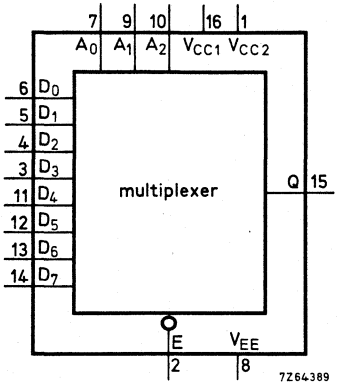


Fig. 1 Logic diagram.

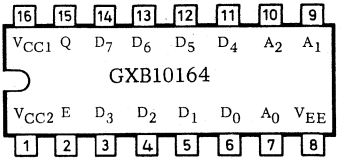


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	−5,2 ± 10%	V
Operating ambient temperature range	T_{amb}	−30 to + 85	°C
Average propagation delay	t_{PLH}	typ. 3	ns
Output voltage			
HIGH state	V_{OH}	nom. −880	mV
LOW state	V_{OL}	nom. −1720	mV
Power consumption per package	P_{av}	typ. 310	mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINE (see Package Outlines)

GXB10164P : plastic 16-lead dual in-line (SOT-38).
GXB10164D: ceramic 16-lead dual in-line (SOT-74).

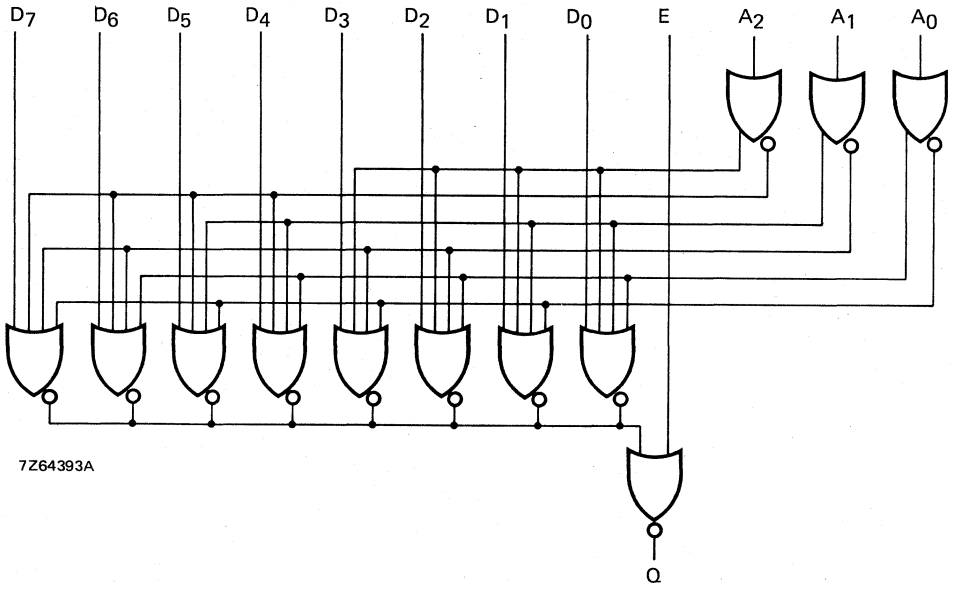


Fig. 3 Logic function.

A_0 to A_2 = address inputs; D_0 to D_7 = data inputs; E = enable input.

inputs												output
A_0	A_1	A_2	$\overline{E}$	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Q
L	L	L	L	L	X	X	X	X	X	X	X	L
L	L	L	L	H	X	X	X	X	X	X	X	H
H	L	L	L	X	L	X	X	X	X	X	X	L
H	L	L	L	X	H	X	X	X	X	X	X	H
L	H	L	L	X	X	L	X	X	X	X	X	L
L	H	L	L	X	X	H	X	X	X	X	X	H
H	H	L	L	X	X	X	L	X	X	X	X	L
H	H	L	L	X	X	X	H	X	X	X	X	H
L	L	H	L	X	X	X	X	L	X	X	X	L
L	L	H	L	X	X	X	X	H	X	X	X	H
H	L	H	L	X	X	X	X	X	L	X	X	L
H	L	H	L	X	X	X	X	X	H	X	X	H
L	H	H	L	X	X	X	X	X	X	L	X	L
L	H	H	L	X	X	X	X	X	X	H	X	H
H	H	H	L	X	X	X	X	X	X	X	L	L
H	H	H	L	X	X	X	X	X	X	X	H	H
X	X	X	H	X	X	X	X	X	X	X	X	L

Function table

H = HIGH state (the more positive voltage); L = LOW state (the less positive voltage); X = state is immaterial.

RATINGS see Family Specifications

D.C. CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground; $V_{EE} = -5{,}2$ V

	symbol		T_{amb} (°C) −30	+ 25	+ 85	unit	remarks
Input current HIGH	I_{IH}	max.	425	265	265	μA	
Input current LOW	I_{IL}	min.	0,5	0,5	0,3	μA	
Supply current	I_{EE}	max.	83	73	83	mA	

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2$ V; $V_{EE} = -3{,}2$ V

	symbol		T_{amb} (°C) −30	+ 25	+ 85	unit	remarks
Rise and fall propagation delay times	$\frac{t_{PLH}}{t_{PHL}}$						
$D_n \longrightarrow Q$		min.	1,5	1,5	1,6	ns	
		max.	4,7	4,5	4,8	ns	
$A_n \longrightarrow Q$		min.	1,9	2,0	2,2	ns	
		max.	6,3	6,0	6,5	ns	
$E \longrightarrow Q$		min.	0,9	1,0	1,0	ns	
		max.	3,3	2,9	3,1	ns	
Transition rise and fall times	$\frac{t_{TLH}}{t_{THL}}$	min.	0,9	1,1	1,2	ns	between 20% and 80%
		max.	3,3	3,3	3,6	ns	

For **switching times test circuit** and **waveforms** see Family Specifications.

8-INPUT PRIORITY ENCODER

The GXB10165 is able to encode eight inputs to binary coded outputs. Each output is stored in a D-type latch which allows synchronous operation. When the clock input is LOW the outputs follow the inputs and latch when the clock goes HIGH. The output code is that of the highest order input so that any input of lower priority is ignored.

The input is active when HIGH (e.g. the three binary outputs are LOW when input D_0 is HIGH). Output Q_3 is HIGH when any input is HIGH, which allows direct extension into another priority encoder when more than 8 inputs are used.

The device can be used in many applications, such as testing systems and checking system status in control processors and peripheral controllers. It can also be used to generate binary codes from random logic inputs, for addressing ROMs, RAMs, or for multiplexing data.

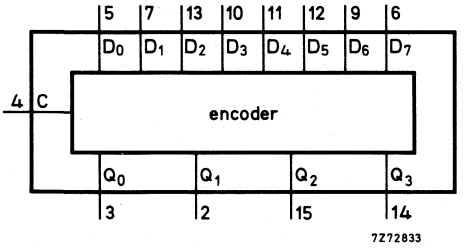


Fig. 1 Block diagram.

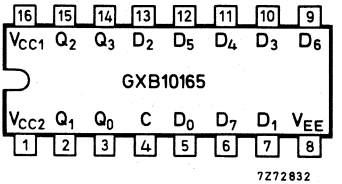


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	−5,2 ± 10%	V
Operating ambient temperature	T_{amb}	−30 to + 85	°C
Average propagation delay	t_{PLH}	typ. 7	ns
Output voltage			
HIGH state	V_{OH}	nom. −880	mV
LOW state	V_{OL}	nom. −1720	mV
Power consumption per package	P_{av}	typ. 545	mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINE (see Package Outlines)

GXB10165P: plastic 16-lead dual in-line (SOT-38).
GXB10165D: ceramic 16-lead dual in-line (SOT-74).

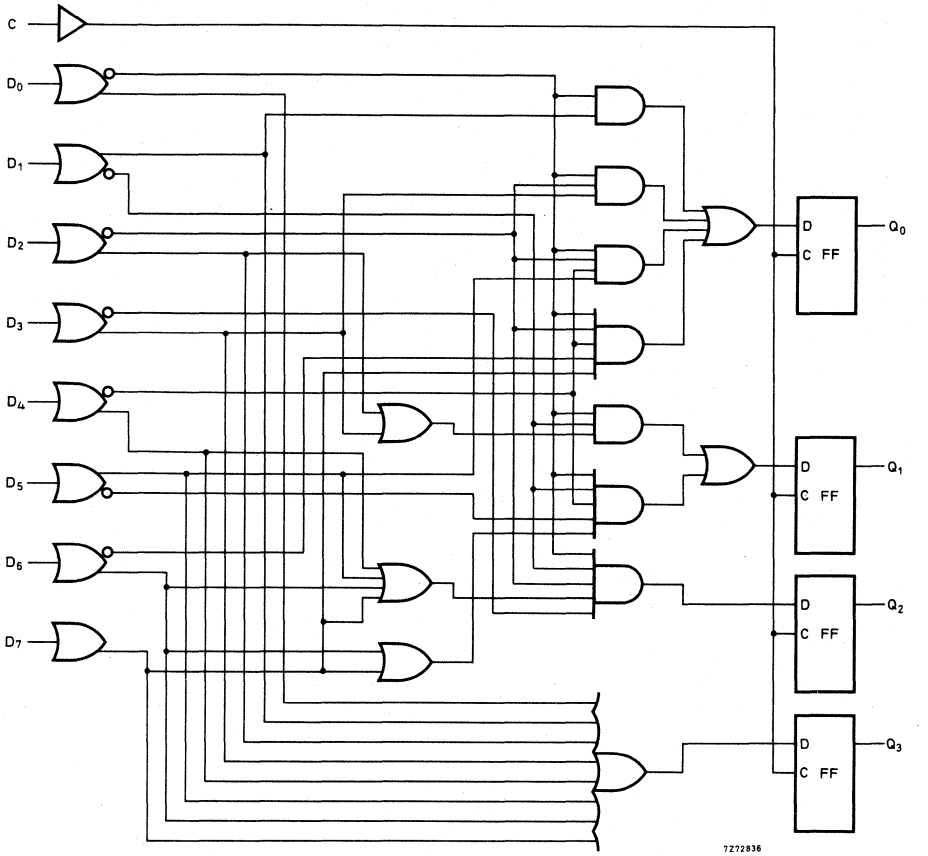


Fig. 3 Logic function.

FUNCTION TABLE

inputs								outputs			
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Q_3	Q_2	Q_1	Q_0
H	X	X	X	X	X	X	X	H	L	L	L
L	H	X	X	X	X	X	X	H	L	L	H
L	L	H	X	X	X	X	X	H	L	H	L
L	L	L	H	X	X	X	X	H	L	H	H
L	L	L	L	H	X	X	X	H	H	L	L
L	L	L	L	L	H	X	X	H	H	L	H
L	L	L	L	L	L	H	X	H	H	H	L
L	L	L	L	L	L	L	H	H	H	H	H
L	L	L	L	L	L	L	L	L	L	L	L

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground; $V_{EE} = -5{,}2$ V

	symbol		T_{amb} (°C) −30	+25	+85	unit	remarks
Input currents HIGH							
pin 4	I_{IH}	max.	390	245	245	μA	
other input pins	I_{IH}	max.	350	220	220	μA	
Input current LOW	I_{IL}	min.	0,5	0,5	0,3	μA	
Supply current	I_{EE}	max.	144	131	144	mA	

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2$ V; $V_{EE} = -3{,}2$ V

	symbol		T_{amb} (°C) −30	+25	+85	unit	remarks
Rise and fall propagation delay times	$\frac{t_{PLH}}{t_{PHL}}$						
D → Q		min.	2,0	2,0	2,0	ns	
		max.	7,0	7,0	8,0	ns	
C → Q		min.	1,5	1,5	1,5	ns	
		max.	4,5	4,0	4,5	ns	
Rise and fall transition time	$\frac{t_{TLH}}{t_{THL}}$	min.	1,1	1,1	1,1	ns	between 20% and 80%
		max.	3,5	3,3	3,5	ns	
Set-up time	t_s	min.	6,0	6,0	6,0	ns	D → C
Hold time	t_h	min.	1,0	1,0	1,0	ns	

For **switching times test circuit** see Family Specifications.

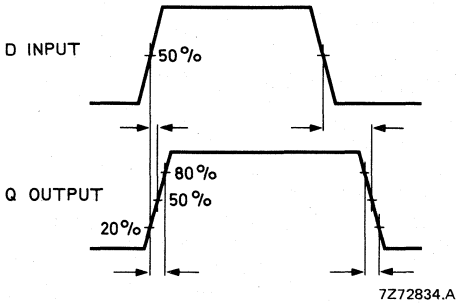


Fig. 4 Switching times waveforms **data** to output.

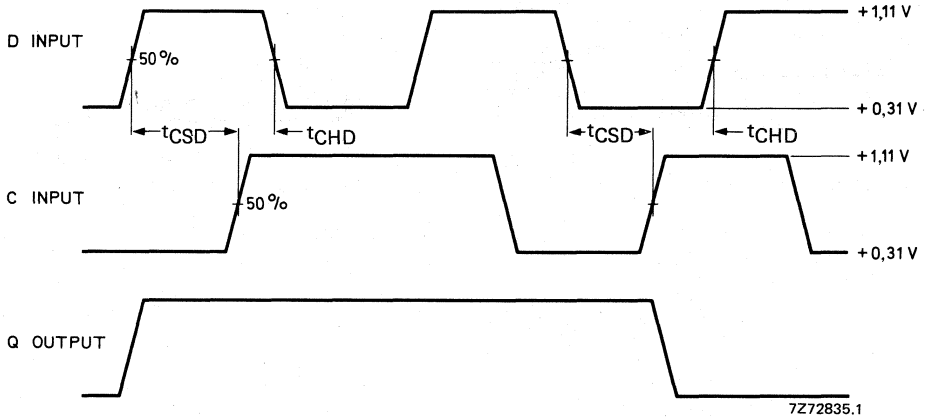


Fig. 5 Switching times waveforms; set-up and hold times DATA to CLOCK.

Notes

1. Set-up times are the minimum times before the positive transition of the clock pulse (C) that information must be present at the data input (D).
2. Hold-times are the minimum times after the positive transition of the clock pulse (C) that information must remain unchanged at the data input (D).

DUAL TWO-BIT DECODER
one of four lines LOW

The GXB10171 is a dual two-bit decoder with one common and two individual enable inputs. The common enable ($\overline{E}$), when HIGH, forces all outputs HIGH. Input pull-down resistors (50 kΩ) allow unused inputs to be left open.

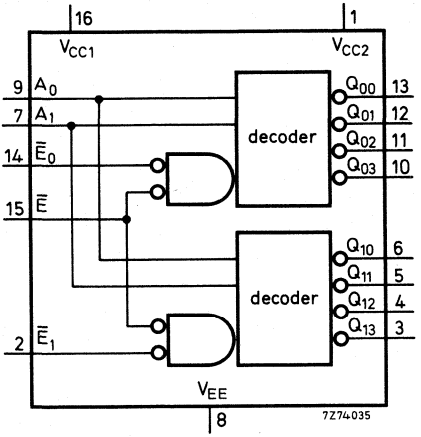


Fig. 1 Logic diagram.

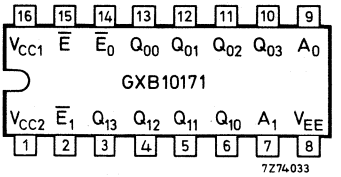


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	−5,2 ± 10%	V
Operating ambient temperature range	T_{amb}	−30 to + 85	°C
Average propagation delay	t_{PLH}	typ. 4,0	ns
Output voltage			
HIGH state	V_{OH}	nom. −880	mV
LOW state	V_{OL}	nom. −1720	mV
Power consumption per package	F_{av}	typ. 325	mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (see Package Outlines)

GXB10171P: plastic 16-lead dual in-line (SOT-38).
GXB10171D: ceramic 16-lead dual in-line (SOT-74).

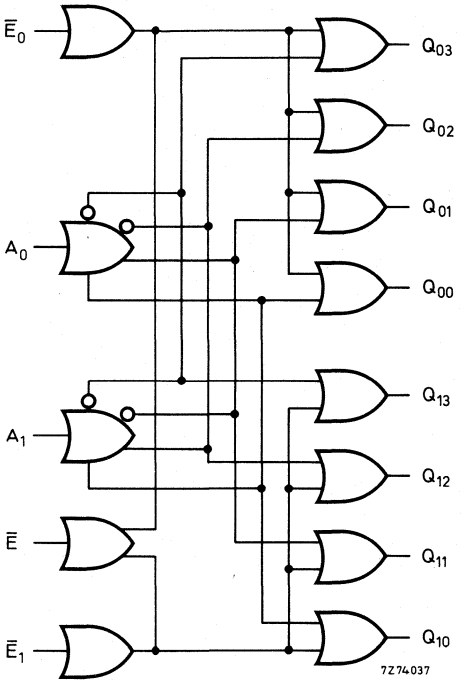


Fig. 3 Logic diagram.

LOGIC FUNCTIONS

$Q_{00} = \overline{E} + \overline{E_0} + A_0 + A_1$
$Q_{01} = \overline{E} + \overline{E_0} + A_0 + \overline{A_1}$
$Q_{02} = \overline{E} + \overline{E_0} + \overline{A_0} + A_1$
$Q_{03} = \overline{E} + \overline{E_0} + \overline{A_0} + \overline{A_1}$

$Q_{10} = \overline{E} + \overline{E_1} + A_0 + A_1$
$Q_{11} = \overline{E} + \overline{E_1} + A_0 + \overline{A_1}$
$Q_{12} = \overline{E} + \overline{E_1} + \overline{A_0} + A_1$
$Q_{13} = \overline{E} + \overline{E_1} + \overline{A_0} + \overline{A_1}$

FUNCTION TABLE

enable inputs			inputs		outputs							
$\overline{E}$	$\overline{E_0}$	$\overline{E_1}$	A_0	A_1	Q_{10}	Q_{11}	Q_{12}	Q_{13}	Q_{00}	Q_{01}	Q_{02}	Q_{03}
L	L	L	L	L	L	H	H	H	L	H	H	H
L	L	L	L	H	H	L	H	H	H	L	H	H
L	L	L	H	L	H	H	L	H	H	H	L	H
L	L	L	H	H	H	H	H	L	H	H	H	L
L	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	L	L	L	H	H	H	H	H	H	H
H	X	X	X	X	H	H	H	H	H	H	H	H

Positive logic: HIGH state = 1
LOW state = 0

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground; $V_{EE} = -5{,}2$ V

	symbol		T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Input current HIGH	I_{IH}	max.	350	220	220	μA	
Input current LOW	I_{IL}	min.	0,5	0,5	0,3	μA	
Supply current	I_{EE}	max.	85	77	85	mA	

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2$ V; $V_{EE} = -3{,}2$ V

	symbol		T_{amb} −30	T_{amb} +25	T_{amb} +85	unit	remarks
Rise and fall propagation delay times	t_{PLH}	min.	1,5	1,5	1,5	ns	
	t_{PHL}	max.	6,2	6,0	6,4	ns	
Rise and fall transition times	t_{TLH}	min.	1,0	1,1	1,1	ns	between 20% and 80%
	t_{THL}	max.	3,3	3,3	3,4	ns	between 20% and 80%

For **switching times test circuit** and **waveforms** see Family Specifications. While testing an input other inputs have to be connected to +0,3 V.

DUAL TWO-BIT DECODER

one of four lines HIGH

The GXB10172 is a dual two-bit decoder with one common and two individual enable inputs. The common enable ($\overline{E}$), when HIGH, forces all outputs LOW. Input pull-down resistors (50 kΩ) allow unused inputs to be left open.

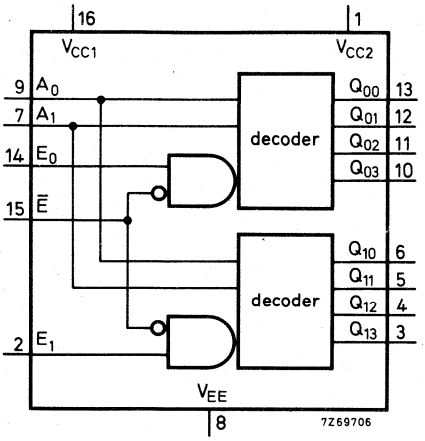


Fig. 1 Logic diagram.

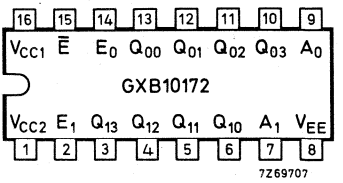


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	−5,3 ± 10%	V
Operating ambient temperature range	T_{amb}	−30 to +85	°C
Average propagation delay	t_{PLH}	typ. 4,0	ns
Output voltage			
HIGH state	V_{OH}	nom. −880	mV
LOW state	V_{OL}	nom. −1720	mV
Power consumption per package	P_{av}	typ. 325	mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINE (see Package Outlines)

GXB10172B: plastic 16-lead dual in-line (SOT-38).
GXB10172D: ceramic 16-lead dual in-line (SOT-74).

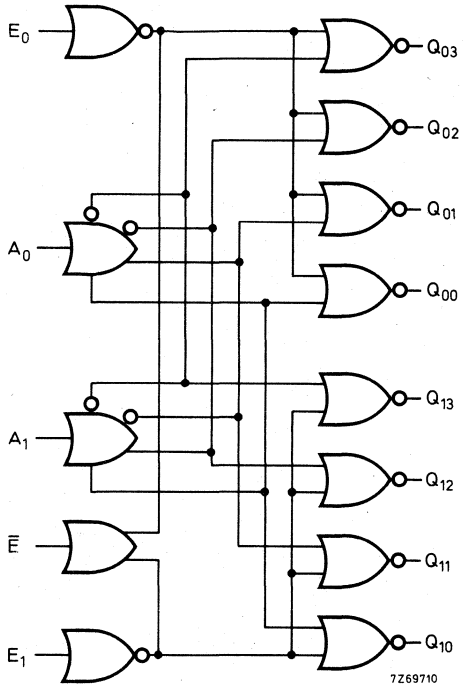


Fig. 3 Logic function.

LOGIC FUNCTIONS

$$Q_{00} = \overline{\overline{E} + \overline{E_0} + A_0 + A_1}$$
$$Q_{01} = \overline{\overline{E} + \overline{E_0} + A_0 + \overline{A_1}}$$
$$Q_{02} = \overline{\overline{E} + \overline{E_0} + \overline{A_0} + A_1}$$
$$Q_{03} = \overline{\overline{E} + \overline{E_0} + \overline{A_0} + \overline{A_1}}$$
$$Q_{10} = \overline{\overline{E} + \overline{E_1} + A_0 + A_1}$$
$$Q_{11} = \overline{\overline{E} + \overline{E_1} + A_0 + \overline{A_1}}$$
$$Q_{12} = \overline{\overline{E} + \overline{E_1} + \overline{A_0} + A_1}$$
$$Q_{13} = \overline{\overline{E} + \overline{E_1} + \overline{A_0} + \overline{A_1}}$$

FUNCTION TABLE

enable inputs			inputs		outputs							
$\overline{E}$	E_0	E_1	A_0	A_1	Q_{10}	Q_{11}	Q_{12}	Q_{13}	Q_{00}	Q_{01}	Q_{02}	Q_{01}
L	H	H	L	L	H	L	L	L	H	L	L	L
L	H	H	L	H	L	H	L	L	L	H	L	L
L	H	H	H	L	L	L	H	L	L	L	H	L
L	H	H	H	H	L	L	L	H	L	L	L	H
L	L	H	L	L	H	L	L	L	L	L	L	L
L	H	L	L	L	L	L	L	L	H	L	L	L
H	X	X	X	X	L	L	L	L	L	L	L	L

Positive logic: HIGH state = 1
LOW state = 0

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground; $V_{EE} = -5{,}2$ V

	symbol		T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Input current HIGH	I_{IH}	max.	350	220	220	μA	
Input current LOW	I_{IL}	min.	0,5	0,5	0,3	μA	
Supply current	I_{EE}	max.	85	77	85	mA	

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2$ V; $V_{EE} = -3{,}2$ V

	symbol		T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Rise and fall propagation delay times	t_{PLH} / t_{PHL}	min.	1,5	1,5	1,5	ns	
		max.	6,2	6,0	6,4	ns	
Rise and fall transition times	t_{THL} / t_{THL}	min.	1,0	1,1	1,1	ns	
		max.	3,3	3,3	3,4	ns	

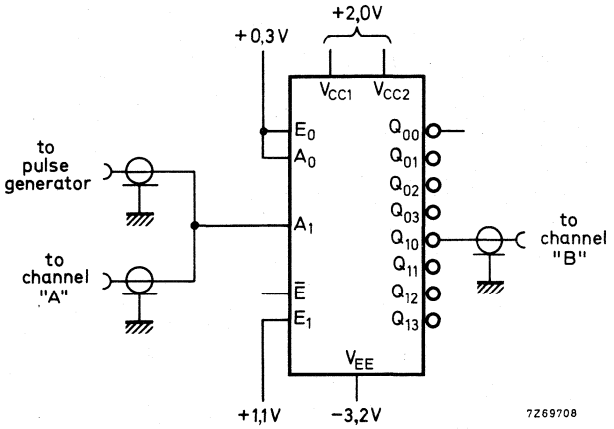


Fig. 4 Switching times test circuit.

For **switching times waveform** see Family Specifications.

QUADRUPLE MULTIPLEXER

The GXB10173 is a quadruple 2-input multiplexer with latched outputs. Each multiplexer has two inputs, selected by the common data select input (D_S). Outputs are latched when the clock is HIGH.

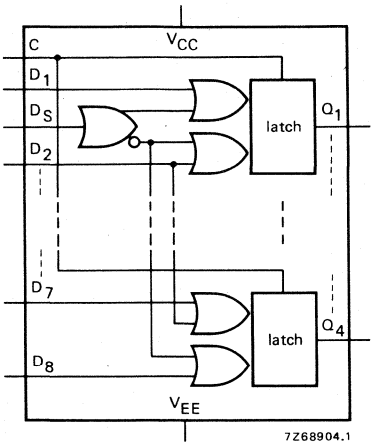


Fig. 1 Logic diagram.

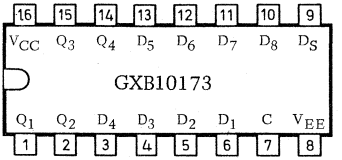


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 ± 10% V
Operating ambient temperature range	T_{amb}		−30 to + 85 °C
Average propagation delay	t_{PLH}	typ.	3,5 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_{av}	typ.	310 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see Package Outlines)

GXB10173P : plastic 16-lead dual in-line (SOT-38).
GXB10173D: ceramic 16-lead dual in-line (SOT-74).

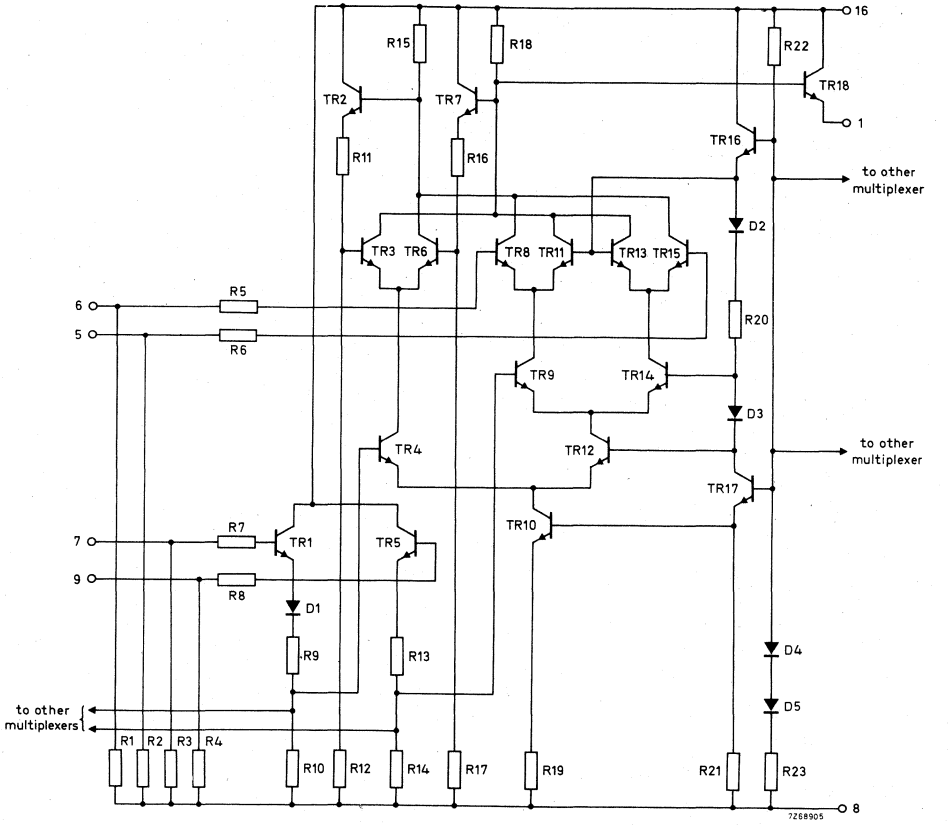


Fig. 3 Circuit diagram (one multiplexer).

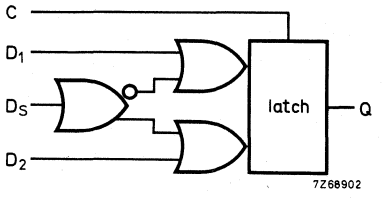


Fig. 4 Logic function.

FUNCTION TABLE

D_S	C	Q_{n+1}
H	L	D_1
L	L	D_2
X	H	Q_n

Positive logic: HIGH state = 1
LOW state = 0
H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground; $V_{EE} = -5{,}2$ V

	symbol		T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Input currents HIGH							
pins 3, 4, 5, 6, 10 11, 12, 13	I_{IH}	max.	470	295	295	μA	
pins 7 and 9	I_{IH}	max.	400	250	250	μA	
Input current LOW	I_{IL}	min.	0,5	0,5	0,3	μA	
Supply current	I_{EE}	max.	73	66	73	mA	

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2$ V; $V_{EE} = -3{,}2$ V

	symbol		T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Rise and fall propagation delay times	t_{PLH} / t_{PHL}						
D → Q		min.	0,8	1,0	1,1	ns	data
		max.	3,7	3,5	5,3	ns	data
C → Q		min.	1,6	1,6	1,4	ns	clock
		max.	7,2	6,8	6,8	ns	clock
D_S → Q		min.	1,1	1,3	1,2	ns	select
		max.	6,2	5,7	6,7	ns	select
Rise and fall transition time	t_{TLH} / t_{THL}	min.	1,2	1,5	1,4	ns	between 20% and 80%
		max.	4,0	3,5	4,0	ns	between 20% and 80%
Rise time CLOCK drive	t_{TLH}	min.	1,2	1,5	1,4	ns	
		max.	5,0	4,5	5,0	ns	
Set-up time							
D → C	t_{DSC}	min.	2,0	2,0	2,0	ns	
D_S → C	t_{DSSC}	min.	3,0	3,0	3,0	ns	
Hold time							
C → D	t_{CHD}	min.	2,5	2,5	2,5	ns	
C → D_S	t_{CHDS}	min.	1,5	1,5	1,5	ns	

For **switching times test circuit** see Family Specifications.

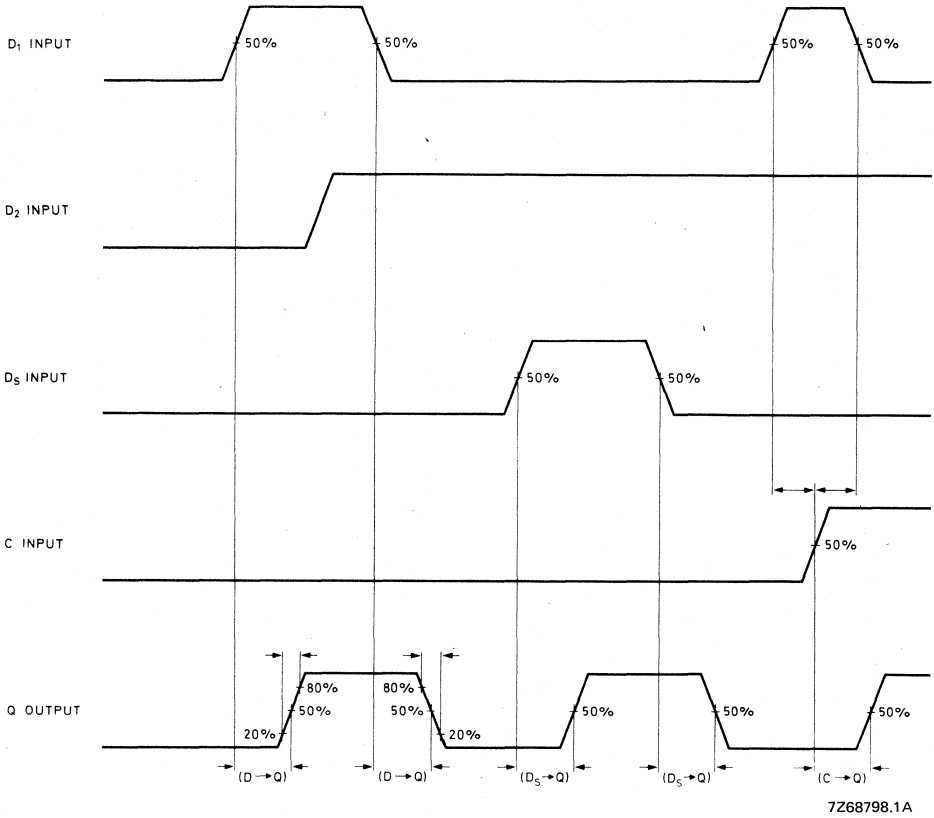


Fig. 5 Switching times waveforms.

Conditions for input signal: $t_r = t_f = 2{,}0$ ns (20% to 80%); $V_{IH} = +1{,}1$ V; $V_{IL} = +0{,}3$ V.

DUAL 4 TO 1 MULTIPLEXER

The GXB10174 performs two 4-input multiplexer functions. The output of each multiplexer reflects one of the 4 data inputs determinated by the states on the two select inputs. An enable input is provided for easy bit expansion by wire-ORing several multiplexers. Each output will go LOW with the enable input in the HIGH state.

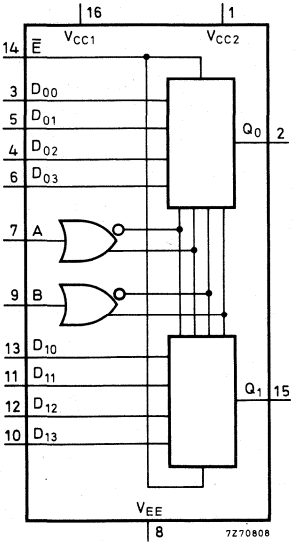


Fig. 1 Logic diagram.

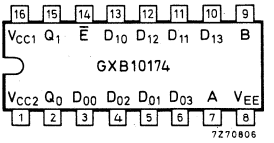


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

A, B: select inputs
D_{00} to D_{03}: data inputs for Q_0
D_{10} to D_{13}: data inputs for Q_1
$\overline{E}$: enable input

QUICK REFERENCE DATA

Supply voltage	V_{EE}	−5,2 ± 10%	V
Operating ambient temperature range	T_{amb}	−3,0 to + 85	°C
Average propagation delay	t_{PLH}	typ. 3	ns
Output voltage			
HIGH state	V_{OH}	nom. −880	mV
LOW state	V_{OL}	nom. −1720	mV
Power consumption per package (no load)	P_{av}	typ. 315	mW

PACKAGE OUTLINES (see Package Outlines).

GXB10174P : plastic 16-lead dual in-line (SOT-38).
GXB10174D: ceramic 16-lead dual in-line (SOT-74).

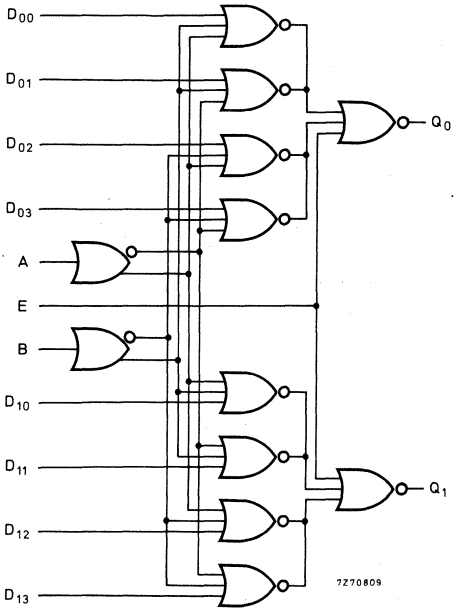


Fig. 3 Logic function.

FUNCTION TABLE

inputs			outputs	
A	B	$\overline{E}$	Q_0	Q_1
L	L	L	D_{00}	D_{10}
L	H	L	D_{02}	D_{12}
H	L	L	D_{01}	D_{11}
H	H	L	D_{03}	D_{13}
X	X	H	L	L

Positive logic:

H = HIGH state
(the more positive voltage) = 1
L = LOW state
(the less positive voltage) = 0
X = state is immaterial

FAMILY DATA and **RATINGS** see Family Specifications.

D.C. CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground; $V_{EE} = -5{,}2$ V

	symbol		T_{amb} (°C) −30	+ 25	+ 85	unit	remarks
Input currents HIGH							
pins 3,4,5,6,7,9 10,11,12,13	I_{IH}	max.	350	220	220	μA	
pin 14	I_{IH}	max.	525	330	330	μA	
Input current LOW	I_{IL}	min.	0,5	0,5	0,3	μA	
Supply current	I_{EE}	max.	80	73	80	mA	

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2$ V; $V_{EE} = -3{,}2$ V; input pulse condition $t_{TLH} = t_{THL} = 2$ ns ± 0,2.

	symbol		T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Rise and fall propagation delay times	$\frac{t_{PLH}}{t_{PHL}}$						
D → Q		min.	1,4	1,5	1,4	ns	
		max.	4,8	4,5	4,8	ns	
A;B → Q		min.	1,9	2,0	2,1	ns	
		max.	6,4	6,0	6,4	ns	
$\overline{E}$ → Q		min.	1,0	1,0	0,9	ns	
		max.	3,1	2,9	3,2	ns	
Transition rise and fall time	$\frac{t_{TLH}}{t_{THL}}$	min.	1,0	1,1	1,1	ns	between 20% and 80%
		max.	3,4	3,3	3,6	ns	

For **switching times waveforms** see Family Specifications

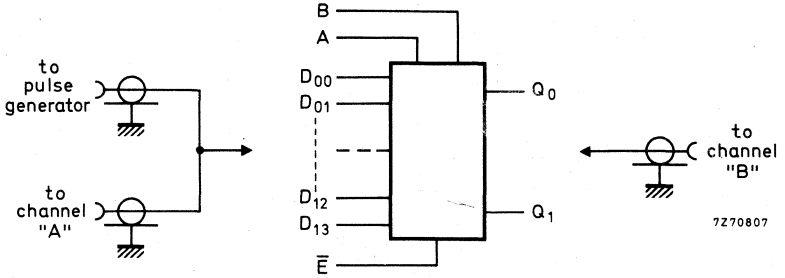


Fig. 4 Switching times test circuit.

QUINT D-LATCH

The GXB10175 includes five D-latches with common reset and two wired-OR common clock inputs. When the clock is in the HIGH state, any change of the data input does not affect the output state. When the clock is in the LOW state, any change of the data input is transferred at the output. The outputs are latched on the positive transition of the clock. The reset input is enabled only when the clock is HIGH.

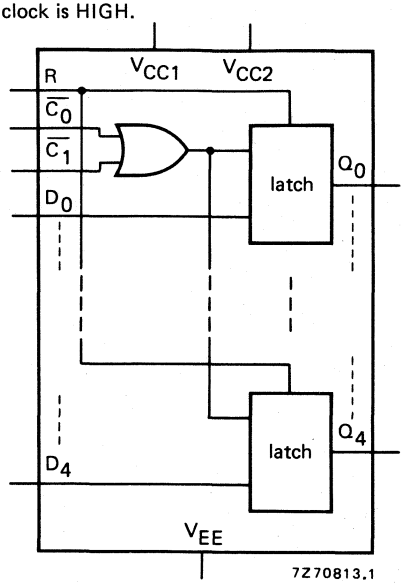


Fig. 1 Logic diagram.

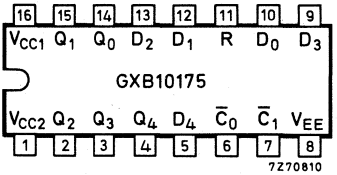


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	−5,2 ± 10%	V
Operating ambient temperature range	T_{amb}	−30 to + 85	°C
Average propagation delay	t_{PLH} typ.	2,5	ns
Output voltage			
HIGH state	V_{OH} nom.	−880	mV
LOW state	V_{OL} nom.	−1720	mV
Power consumption per package (no load)	P_{av} typ.	400	mW

PACKAGE OUTLINES (see Package Outlines)

GXB10175P : plastic 16-lead dual in-line (SOT-38).
GXB10175D: ceramic 16-lead dual in-line (SOT-74).

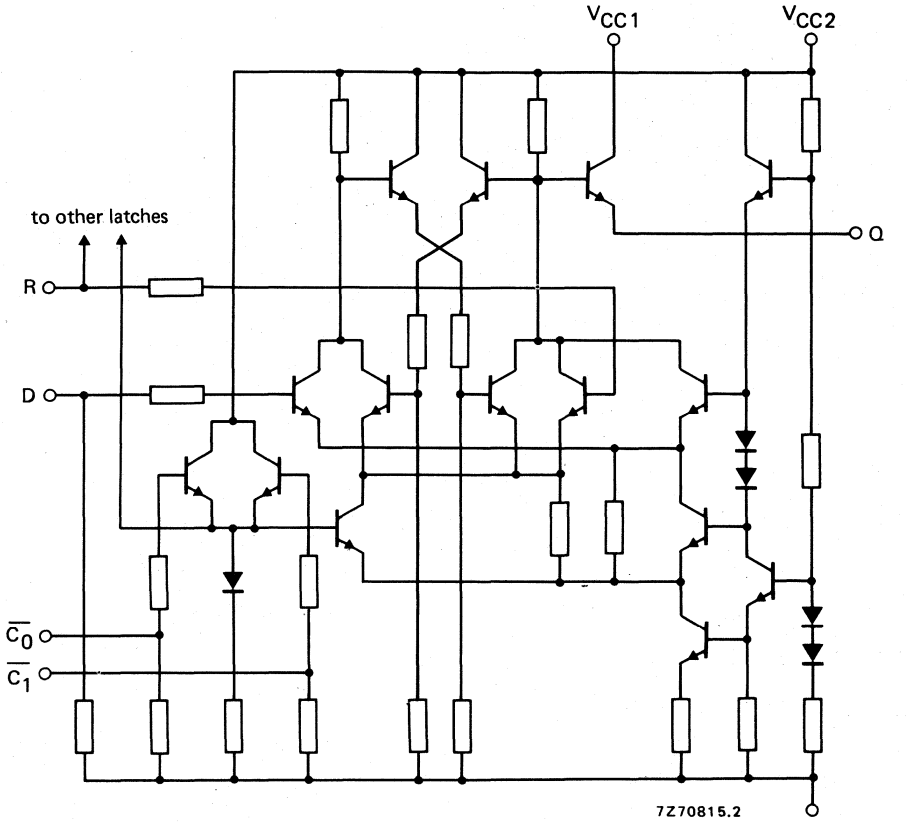


Fig. 3 Circuit diagram (one latch).

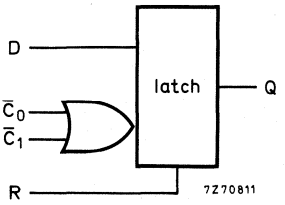


Fig. 4 Logic function.

FUNCTION TABLE

$\overline{C}_0$	$\overline{C}_1$	R	D	$Q_n + 1$
L	L	X	L	L
L	L	X	H	H
H	X	L	X	Q_n
X	H	L	X	Q_n
H	X	H	X	L
X	H	H	X	L

Positive logic:
H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0
X = state is immaterial

FAMILY DATA and **RATINGS** see Family Specifications

D.C. CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground; $V_{EE} = -5{,}2$ V

	symbol		T_{amb} (°C) −30	+ 25	+ 85	unit	remarks
Input currents HIGH							
pins 5, 6, 7, 9, 10, 12, 13	I_{IH}	max.	460	290	290	μA	
pin 11	I_{IH}	max.	1000	650	650	μA	
Input current LOW	I_{IL}	min.	0,5	0,5	0,3	μA	
Supply current	I_{EE}	max.	107	97	107	mA	

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2$ V; $V_{EE} = -3{,}2$ V; input pulse condition $t_{TLH} = t_{THL} = 2$ ns ± 0,2.

	symbol		T_{amb} (°C) −30	+ 25	+ 85	unit	remarks
Rise and fall propagation delay times	$\overline{t_{PLH}}$ / $\overline{t_{PHL}}$						
D → Q		min.	1,0	1,0	1,0	ns	Data to output
		max.	3,6	3,5	3,6	ns	
C → Q		min.	1,0	1,0	1,0	ns	Clock to output
		max.	4,7	4,3	4,4	ns	
R → Q		min.	1,0	1,0	1,0	ns	Reset to output
		max.	4,0	3,9	4,2	ns	
Rise and fall transition time	t_{TLH}	min.	1,0	1,1	1,1	ns	between 20% and 80%
	$\overline{t_{THL}}$	max.	3,6	3,5	3,7	ns	
Set-up time	t_s	min.	2,5	2,5	2,5	ns	
Hold time	t_h	min.	1,5	1,5	1,5	ns	

Notes

1. Input signal: $t_r = t_f = 2{,}0$ ns (20% to 80%); $V_{IH} = +1{,}11$ V; $V_{IL} = +0{,}31$ V.
2. Propagation delay from reset to output. Output latched on a HIGH state prior to test.
3. Set-up times are the minimum times before the positive transition of the clock pulse (C) that information must be held at the data inputs (D).
4. Hold times are the minimum times after the positive transition of the clock pulse (C) that information must be held at the data inputs (D).
5. Input resistance is positive at any frequency.

For **switching times test circuit** and **waveforms** see Family Specifications.

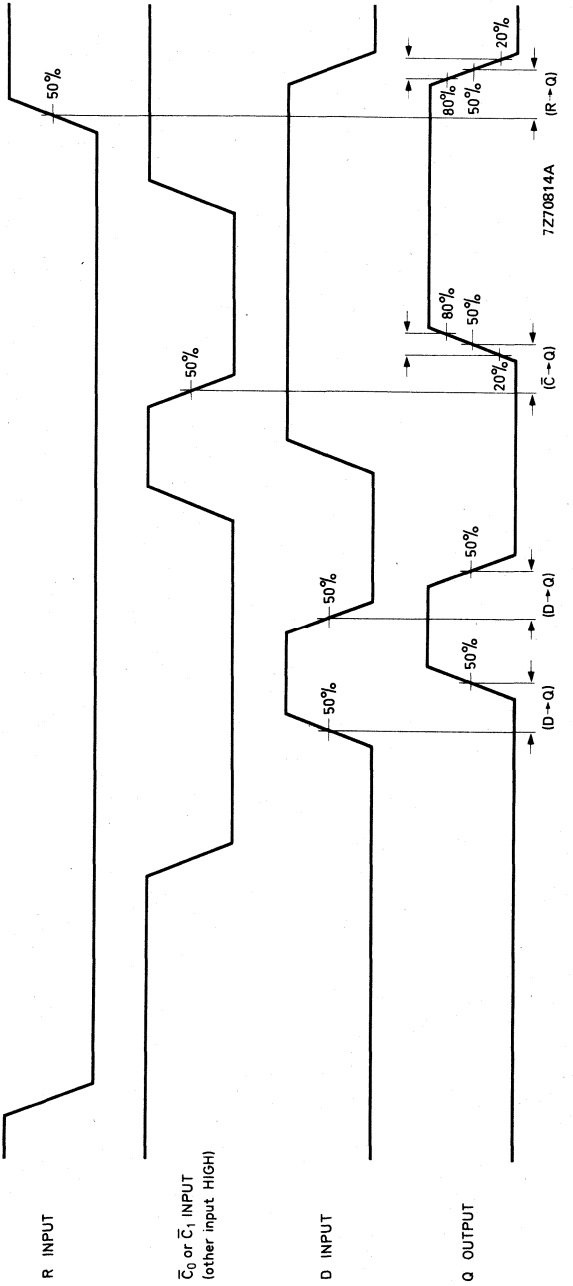


Fig. 5 Switching times waveforms.

HEX D-TYPE MASTER-SLAVE FLIP-FLOP

The GXB10176 includes six high speed master-slave D-type flip-flops with one common input clock for all six. Data enters into the master during the LOW state of the clock and is transferred to the slave during the positive-going clock transition. Due to the master-slave structure of the device, a change in the information present at the data (D) input will not modify the output information at any other time.

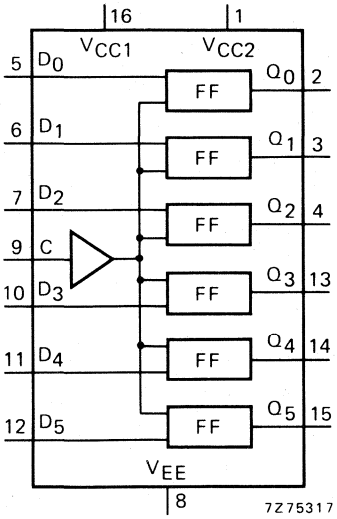


Fig. 1 Logic diagram.

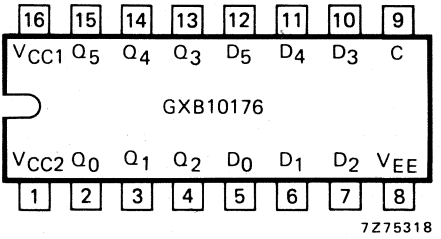


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	−5,2 ± 10%	V
Operating ambient temperature range	T_{amb}	−30 to + 85	°C
Clock frequency	f	typ. 150	MHz
Output voltage			
HIGH state	V_{OH}	nom. −880	mV
LOW state	V_{OL}	nom. −1720	mV
Power consumption per package (no load)	P_{av}	typ. 460	mW

PACKAGE OUTLINES (see Package Outlines)

GXB10176P: 16-lead DIL; plastic (SOT-38).
GXB10176D: 16-lead DIL; ceramic (SOT-74).

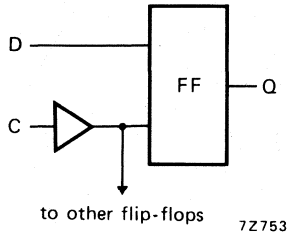


Fig. 3 Logic diagram (one flip-flop).

FUNCTION TABLE

C	D	$Q_n + 1$
L	X	Q_n
H	L	L
H	H	H

Positive logic: HIGH state = 1
LOW state = 0

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

C at LOW state; data enters into the master. A clock H means a clock transition from a LOW to a HIGH state; data transfer to the slave output.

D.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = −5,2 V

	symbol		T_{amb} (°C) −30	+ 25	+ 85	unit	remarks
Input currents HIGH							
pins 5,6,7,10,11,12	I_{IH}	max.	350	220	220	μA	
pin 9	I_{IH}	max.	495	310	310	μA	
Input current LOW	I_{IL}	min.	0,5	0,5	0,3	μA	
Supply current (d.c.)	I_{EE}	max.	121	110	121	mA	

RATINGS and **FAMILY DATA** see Family Specifications.

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = +2{,}0$ V; $V_{EE} = -3{,}2$ V.

	symbol		T_{amb} (°C) −35	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Propagation delay rise and fall times	$t_{\overline{PLH}}$	min.	1,6	1,6	1,6	ns	
	$t_{\overline{PHL}}$	max.	4,6	4,5	5,0	ns	
Transition rise and fall times	$t_{\overline{TLH}}$	min.	1,0	1,1	1,1	ns	between 20% and 80%
	$t_{\overline{THL}}$	max.	4,1	4,0	4,4	ns	between 20% and 80%
Set-up time D → C	t_{DSC}	min.	2,5	2,5	2,5	ns	
Hold time C → D	t_{CHD}	min.	1,5	1,5	1,5	ns	
Clock frequency	f_C	min.	125	125	125	MHz	

For **switching times test circuit** and **waveforms** see Family Specifications

Notes

1. Set-up times are the minimum times before the positive transition of the clock pulse (C) that information must be present at the data input (D).
2. Hold times are the minimum times after the positive transition of the clock pulse (C) that information must remain unchanged at the data input (D).

Note that the hold times may be a negative number.

LOOK-AHEAD CARRY BLOCK

The GXB10179 is a look-ahead carry block. It can be used in conjunction with the GXB10181 4-bit arithmetic/logic unit to perform a high order look-ahead carry, in applications requiring high speed arithmetic operation on long words.

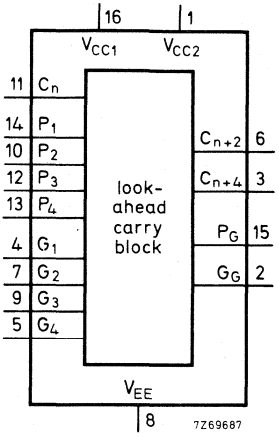


Fig. 1 Block diagram.

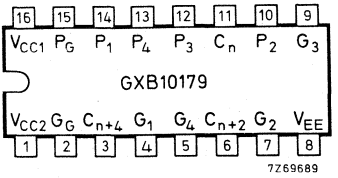


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

C_n:	carry input
P_2 to P_4:	carry propagate inputs
G_1 to G_4:	carry generate inputs
$C_n + 2$; $C_n + 4$:	carry outputs
P_G:	carry propagate output*
G_G:	carry generate output*

* For higher order look-ahead extension.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	$-5{,}2 \pm 10\%$	V
Operating ambient temperature range	T_{amb}	-30 to $+85$	°C
Output voltage			
HIGH state	V_{OH}	nom. -880	mV
LOW state	V_{OL}	nom. -1720	mV
Power consumption per package (no load)	P_{av}	typ. 300	mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see Package Outlines)

GXB10179P: plastic 16-lead dual in-line (SOT-38).
GXB10179D: ceramic 16-lead dual in-line (SOT-74).

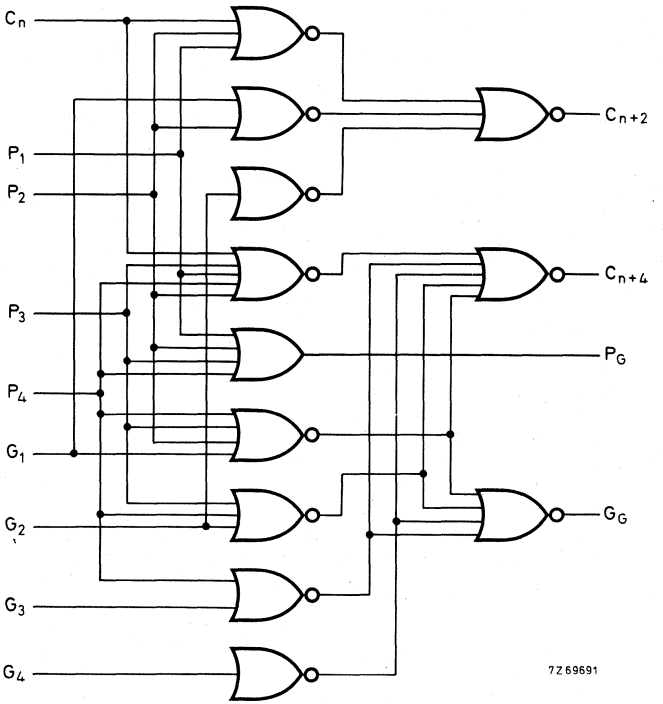


Fig. 3 Logic diagram.

LOGIC FUNCTION

$P_G = P_1 + P_2 + P_3 + P_4$

$G_G = G_4 (G_3 + P_4) (G_2 + P_3 + P_4) (G_1 + P_2 + P_3 + P_4)$

$C_{n+2} = G_2 (G_1 + P_2) (C_n + P_1 + P_2)$

$C_{n+4} = G_4 (G_3 + P_4) (G_2 + G_3 + P_4) (G_1 + P_2 + P_3 + P_4) (C_n + P_1 + P_2 + P_3 + P_4)$

In positive logic: H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0

The overall carry function is invariant with the polarity (positive or negative) of the logic if the P and G inputs are interchanged.

RATINGS see Family Specifications

D.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = −5,2 V

	symbol		T_{amb} (°C) −30	+ 25	+ 85	unit	remarks
Input currents							
HIGH							
pins 5,9	I_{IH}	max.	360	225	225	μA	
pins 4,7,11	I_{IH}	max.	430	270	270	μA	
pin 14	I_{IH}	max.	565	355	355	μA	
pin 12	I_{IH}	max.	630	395	395	μA	
pins 10,13	I_{IH}	max.	700	440	440	μA	
Input current							
LOW	I_{IL}	min.	0,5	0,5	0,3	μA	
Supply current (d.c.)	I_{EE}	max.	79	72	79	mA	

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = + 2,0 V; V_{EE} = −3,2 V

	symbol		T_{amb} (°C) −35	+ 25	+ 85	unit	remarks
Rise and fall propagation delay times	$\frac{t_{PLH}}{t_{PHL}}$						
G → C C_n → C G → G_G P → G_G		min.	1,0	1,0	1,0	ns	
		max.	5,8	5,5	6,1	ns	
P → P_G		min.	1,0	1,0	1,0	ns	
		max.	3,7	3,5	3,9	ns	
Transition rise and fall time	$\frac{t_{TLH}}{t_{THL}}$	min.	1,1	1,1	1,1	ns	Between
		max.	3,7	3,5	3,9	ns	20% and 80%

For **switching times test circuits** and **waveforms** see Family Specifications.

DUAL 2-BIT ADDER/SUBTRACTOR

The GXB10180 is a high-speed, low power, general purpose adder/subtractor. Inputs for each adder are: Carry-in, Operand A, Operand B. Outputs are: Sum, $\overline{\text{Sum}}$ and Carry-out.

Common select inputs act as control lines to invert A or B for subtract. A very high speed of operation is possible with Operand in the Sum or Carry-out propagation delay of 4,5 ns, and Carry-in to Carry-out propagation delay of 2,2 ns.

The GXB10180 is designed to be used in special purpose adders/subtractors or in high speed multiplier arrays.

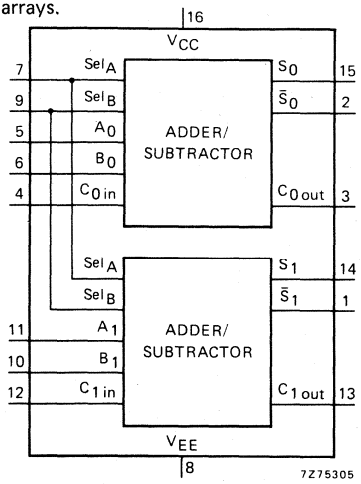


Fig. 1 Block diagram.

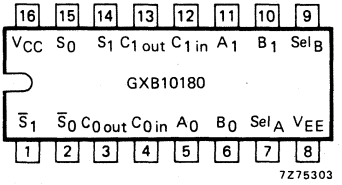


Fig. 2 Pin designation.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	−5,2 ± 10%	V
Operating ambient temperature range	T_{amb}	−30 to +85	°C
Average propagation delay	t_{PLH}	typ. 4,5	ns
Output voltage			
HIGH state	V_{OH}	nom. −880	mV
LOW state	V_{OL}	nom. −1720	mV
Power consumption per package (no load)	P_{av}	typ. 360	mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (see Package Outlines)

GXB10180P: 16-lead DIL; plastic (SOT-38).
GXB10180D: 16-lead DIL; ceramic (SOT-74).

FUNCTION SELECT TABLE

Sel_A	Sel_B	functions S
H	H	$A + B + C_I$
H	L	$C_I + A - B$
L	H	$C_I + B - A$
L	L	$C_I - A - B$

Positive logic: HIGH state = 1
(the more positive voltage)
LOW state = 0
(the less positive voltage)

Positive logic only

$A' = \overline{A \oplus Sel_A} = A \odot Sel_A$

$B' = \overline{B \oplus Sel_B} = B \odot Sel_B$

Both positive and negative logic

$S = \overline{C}_{in} (\overline{A}' B' + A' \overline{B}') + C_{in} (A' B' + \overline{A}' \overline{B}')$

$C_{out} = C_{in} A' + C_{in} B' + A' B'$

FUNCTION TABLE

function	inputs					outputs		
	Sel_A	Sel_B	A	B	C_{in}	S	$\overline{S}$	C_{out}
ADD $(A + B + C_I)$	H	H	L	L	L	L	H	L
	H	H	L	L	H	H	L	L
	H	H	L	H	L	H	L	L
	H	H	L	H	H	L	H	H
	H	H	H	L	L	H	L	L
	H	H	H	L	H	L	H	H
	H	H	H	H	L	L	H	H
	H	H	H	H	H	H	L	H
SUBTRACT $(C_I + A - B)$	H	L	L	L	L	H	L	L
	H	L	L	L	H	L	H	H
	H	L	L	H	L	L	H	L
	H	L	L	H	H	H	L	L
	H	L	H	L	L	L	H	H
	H	L	H	L	H	H	L	H
	H	L	H	H	L	H	L	L
	H	L	H	H	H	L	H	H
Reverse SUBTRACT $(C_I + B - A)$	L	H	L	L	L	H	L	L
	L	H	L	L	H	L	H	H
	L	H	L	H	L	L	H	H
	L	H	L	H	H	H	L	H
	L	H	H	L	L	L	H	L
	L	H	H	L	H	H	L	L
	L	H	H	H	L	H	L	L
	L	H	H	H	H	L	H	H
$(C_I - A - B)$	L	L	L	L	L	L	H	H
	L	L	L	L	H	H	L	H
	L	L	L	H	L	H	L	L
	L	L	L	H	H	L	H	H
	L	L	H	L	L	H	L	L
	L	L	H	L	H	L	H	H
	L	L	H	H	L	L	H	L
	L	L	H	H	H	H	L	L

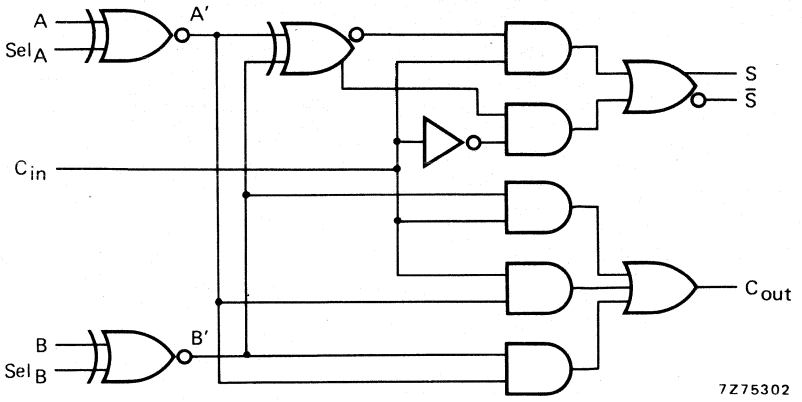


Fig. 3 Logic function (one adder/subtractor).

RATINGS see Family Specifications

D.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = −5,2 V

	symbol		T_{amb} (°C) −30	+25	+85	unit	remarks
Input currents HIGH							
pins 5, 6, 10, 11	I_{IH}	max.	350	220	220	μA	
pins 7, 9	I_{IH}	max.	460	290	290	μA	
pins 4, 12	I_{IH}	max.	590	370	370	μA	
Input current LOW	I_{IL}	min.	0,5	0,5	0,3	μA	
Supply current (d.c.)	I_{EE}	max.	95	86	95	mA	

A.C. CHARACTERISTICS

V_{CC1} = V_{CC2} = +2,0 V; V_{EE} −3,2 V

	symbol		T_{amb} (°C) −30	+25	+85	unit	remarks
Propagation delay rise and fall times	$\frac{t_{PLH}}{t_{PHL}}$						
A → C_{out}		min.	1,3	1,3	1,1	ns	Operand → output
SEL → C_{out}		max.	5,8	5,4	5,8	ns	Select → output
C_I → C_{out}		min.	1,0	1,0	0,9	ns	Carry in → out
		max.	3,4	3,3	3,6	ns	

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = +2{,}0$ V; $V_{EE} - 3{,}2$ V

	symbol	T_{amb} (°C) −35	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Transition rise and fall times	$\frac{t_{TLH}}{t_{THL}}$ min.	1,0	1,1	1,1	ns	between 20% and 80%
	max.	3,8	3,7	3,9	ns	

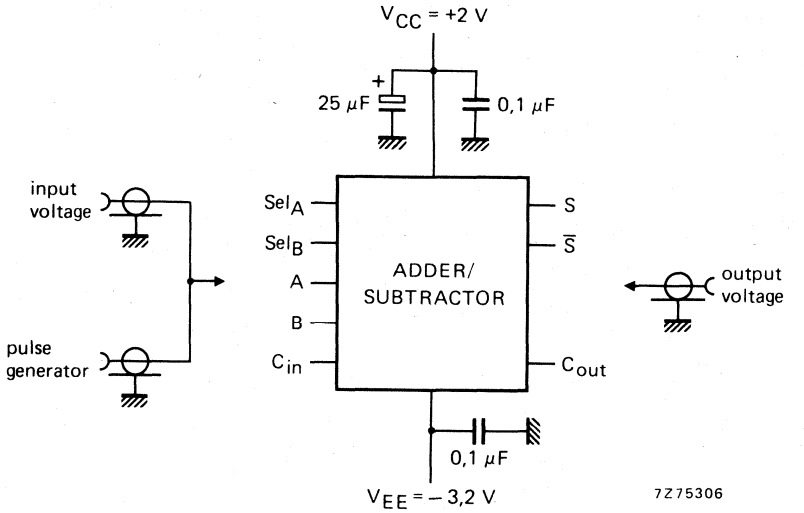


Fig. 4 Switching times test circuit.

Input pulse condition: $t_r = t_f = 2{,}0 \pm 0{,}2$ ns (20 to 80%).

For **switching times waveforms** see Family Specifications.

4-BIT ARITHMETIC/LOGIC UNIT

The GXB10181 is a high-speed arithmetic logic unit. It performs 16 logic operations and 16 arithmetic operations on two 4-bit words. Arithmetic or logic mode of operation is selected by the mode control input (M). Arithmetic logic operations are selected by a 4-bit select input (S_0 to S_3) in accordance with the function table. The device provides a group carry propagate (P_G) and a carry generate (G_G) for high-speed operations on very long words, using a GXB10179 as a high order look-ahead carry block. The internal carry is enabled while the mode control input (M) is LOW (arithmetic operation).

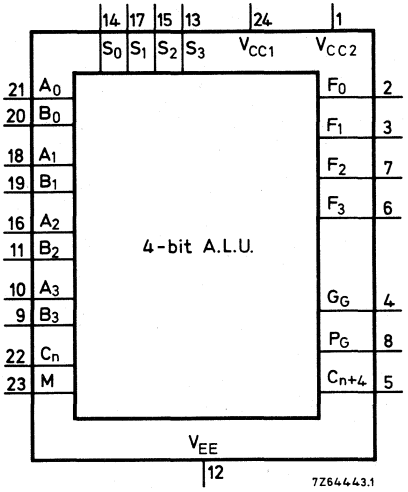


Fig. 1 Block diagram.

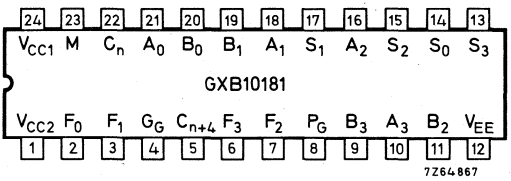


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	−5,2 ± 10%	V
Operating ambient temperature range	T_{amb}	−30 to + 85	°C
Average propagation delay	t_{PLH}	typ. 4,2	ns
Output voltage			
HIGH state	V_{OH}	nom. −880	mV
LOW state	V_{OL}	nom. −1720	mV
Power consumption per package	P_{av}	typ. 600	mW

PACKAGE OUTLINES (see Package Outlines)

GXB10181P: plastic 24-lead dual in-line (SOT-101).
GXB10181D: ceramic 24-lead dual in-line (SOT-149).

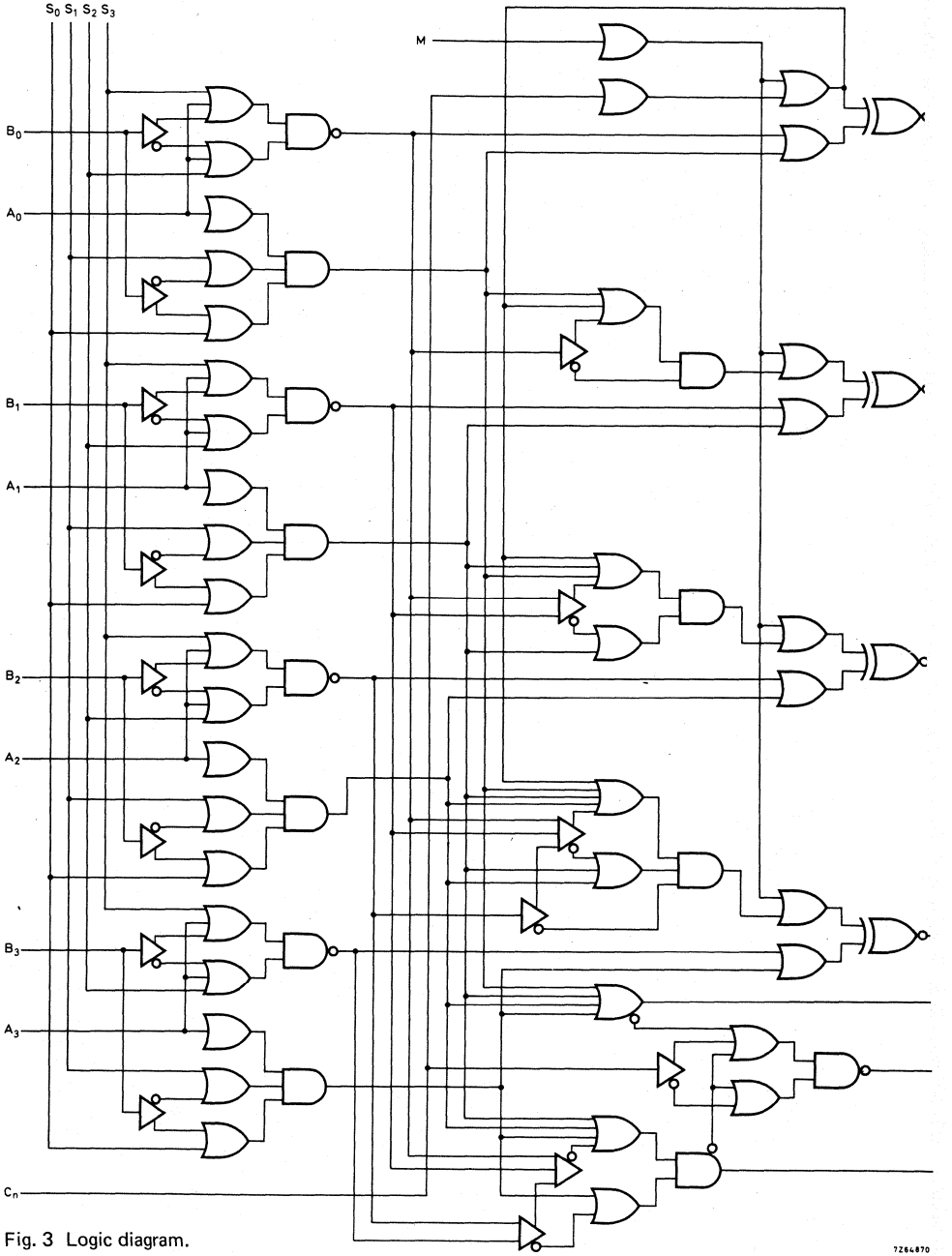


Fig. 3 Logic diagram.

PIN NAMES

A_0 to A_3: word inputs
B_0 to B_3: word inputs
S_0 to S_3: function select inputs
M : mode control input
F_0 to F_3: data outputs

C_n : carry input
C_{n+4}: carry output
P_G : carry propagate output
G_G : carry generate output

FUNCTION TABLE

function select inputs				logic function mode	arithmetic operation mode
S_3	S_2	S_1	S_0	F (M = HIGH)	F (M = LOW; C_n = LOW)
L	L	L	L	$\overline{A}$	A
L	L	L	H	$\overline{A} + \overline{B}$	A plus (A·$\overline{B}$)
L	L	H	L	$\overline{A} + B$	A plus (A·B)
L	L	H	H	logic "1"	A times 2
L	H	L	L	$\overline{A \cdot B}$	(A+B) plus 0
L	H	L	H	$\overline{B}$	(A+B) plus (A·$\overline{B}$)
L	H	H	L	$AB + \overline{AB}$	A plus B
L	H	H	H	$A + \overline{B}$	A plus (A+B)
H	L	L	L	$\overline{A \cdot B}$	(A+$\overline{B}$) plus 0
H	L	L	H	$A\overline{B} + \overline{A}B$	A minus B minus 1
H	L	H	L	B	(A+$\overline{B}$) plus (A·B)
H	L	H	H	A + B	A plus (A+$\overline{B}$)
H	H	L	L	logic "0"	minus 1 (two's complement)
H	H	L	H	A·$\overline{B}$	(A·$\overline{B}$) minus 1
H	H	H	L	AB	(A·B) minus 1
H	H	H	H	A	A minus 1

Positive logic: H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0

RATINGS and **FAMILY DATA** see Family Specifications.

D.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = −5,2 V

	symbol		T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Input currents HIGH							
pins 9,11,19,20	I_{IH}	max.	390	245	245	μA	
pins 10,16,18,21	I_{IH}	max.	350	220	220	μA	
pin 23	I_{IH}	max.	320	200	200	μA	
pins 13,14,15,17	I_{IH}	max.	425	265	265	μA	
pin 22	I_{IH}	max.	460	290	290	μA	
Input current LOW	I_{IL}	min.	0,5	0,5	0,3	μA	
Supply current (d.c.)	I_{EE}	max.	159	145	159	mA	

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = +2{,}0$ V; $V_{EE} = -3{,}2$ V

	symbol	T_{amb} (°C)						unit	remarks
		−35		+ 25		+ 85			
		min.	max.	min.	max.	min.	max.		
Propagation delay rise and fall times	$\frac{t_{PLH}}{t_{PHL}}$								
$C_n \rightarrow C_{n+4}$		1,0	5,1	1,1	5,0	1,1	5,4	ns	
$C_n \rightarrow F$		1,7	7,2	2,0	7,0	2,0	7,5	ns	
$A \rightarrow F$		2,6	10,4	3,0	10,0	3,0	10,8	ns	
$A \rightarrow P_G$		1,6	7,0	2,0	6,5	2,0	7,0	ns	
$A \rightarrow G_G$		1,1	7,4	2,0	7,0	1,3	7,7	ns	
$A \rightarrow C_{n+4}$		1,7	7,3	2,0	7,0	2,0	7,8	ns	
$B \rightarrow F$		2,7	11,3	3,0	11,0	3,0	11,9	ns	
$B \rightarrow P_G$		1,6	7,7	2,0	7,5	2,0	8,0	ns	
$B \rightarrow G_G$		1,7	8,2	2,0	8,0	2,0	8,6	ns	
$B \rightarrow C_{n+4}$		1,8	8,2	2,0	8,0	2,0	8,7	ns	
$M \rightarrow F$		2,4	10,3	3,0	10,0	3,0	10,8	ns	
$S \rightarrow F$		2,5	10,7	3,0	10,0	3,0	10,8	ns	
$S \rightarrow P_G$		1,7	8,3	2,0	8,0	2,0	8,4	ns	
$S \rightarrow G_G$		1,5	9,6	2,0	9,0	1,9	9,7	ns	
$S \rightarrow C_{n+4}$		1,6	9,3	2,0	9,0	2,0	9,9	ns	

Transition rise and fall times	input under test	ambient temperature (°C)						unit	remarks
		−35		+ 25		+ 85			
		min.	max.	min.	max.	min.	max.		
$\frac{t_{TLH}}{t_{THL}}$									
output C_{n+4}	C_n	1,0	3,2	1,0	3,0	1,0	3,2	ns	
	A	1,0	3,1	1,0	3,0	1,0	3,2	ns	
	B	0,9	3,1	1,0	3,0	1,0	3,2	ns	
	S	0,9	5,3	1,1	5,0	1,0	5,2	ns	
Output F	C_n	1,3	5,3	1,5	5,0	1,5	5,3	ns	
	A	1,3	5,4	1,5	5,0	1,5	5,3	ns	
	B	1,2	5,3	1,5	5,0	1,5	5,3	ns	
	M	1,1	5,1	1,5	5,0	1,5	5,3	ns	
	S	1,0	5,4	1,5	5,0	1,5	5,4	ns	
Output P_G	A	0,8	3,7	1,1	3,5	1,1	3,8	ns	
	B	1,0	3,6	1,1	3,5	1,1	3,9	ns	
	S	0,8	5,1	1,1	5,0	1,1	5,2	ns	
Output G_G	A	1,2	5,1	1,5	5,0	1,2	5,3	ns	
	B	1,4	5,2	1,5	5,0	1,2	5,4	ns	
	S	0,8	6,2	0,8	6,0	0,8	6,5	ns	

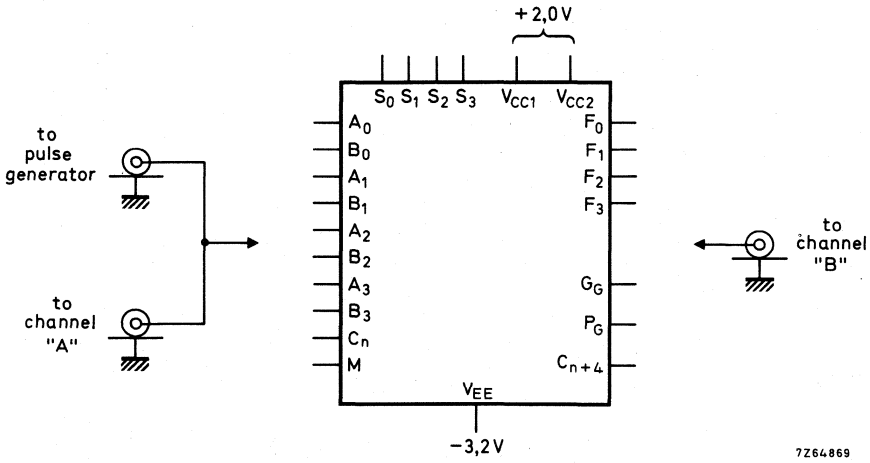


Fig. 4 Switching times test circuit.

See also Family Specifications **switching times test circuit and waveforms.**

HEX BUFFER WITH ENABLE

The GXB10188 includes six buffers offering individual inputs and outputs and a common enable input, driving all outputs LOW. Each input is connected to V_{EE} via a 50 kΩ pull-down resistor resulting in high input impedance and eliminating need of connecting unused inputs LOW.

Due to open emitter outputs the GXB10188 features OR capability with high fan-out for driving 50 Ω lines.

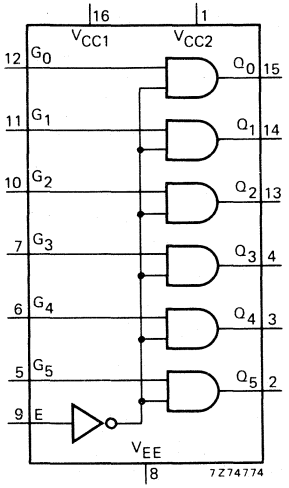


Fig. 1 Logic diagram.

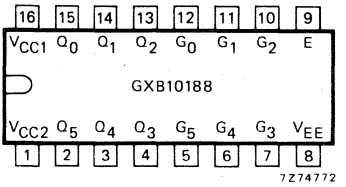


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	−5,2 ± 10%	V
Operating ambient temperature range	T_{amb}	−30 to +85	°C
Average propagation delay	t_{PLH}	typ. 2,0	ns
Output voltage			
HIGH state	V_{OH}	nom. −880	mV
LOW state	V_{OL}	nom. −1720	mV
Power consumption per package (no load)	P_{av}	typ. 170	mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (See Package Outlines)

GXB10188P: 16-lead DIL; plastic (SOT-38Z).
GXB10188D: 16-lead DIL; ceramic (SOT-74).

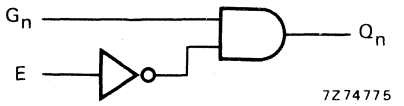


Fig. 3 Logic diagram (one buffer).

FUNCTION TABLE

inputs		output
E	G_n	Q_n
L	L	L
L	H	H
H	X	L

LOGIC FUNCTION

$Q_n = G_n \cdot \overline{E}$

Positive logic:

H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0
X = state is immaterial

RATINGS see Family Specifications

D.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = −5,2 V

	symbol		T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Input current HIGH							
pins 5,6,7,10,11,12	I_{IH}	max.	425	265	265	μA	
pin 9	I_{IH}	max.	460	290	290	μA	
Input current LOW	I_{IL}	min.	0,5	0,5	0,3	μA	
Supply current (d.c.)	I_{EE}	max.	46	42	46	mA	

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = +2,0$ V; V_{EE} −3,2 V

	symbol		T_{amb} (°C) −35	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Propagation delay rise and fall times	$\frac{t_{PLH}}{t_{PHL}}$						
$G_n \longrightarrow Q_n$		min.	1,0	1,0	1,0	ns	data
		max.	3,3	2,9	3,3	ns	data
$E \longrightarrow Q_n$		min.	1,1	1,1	1,1	ns	enable
		max.	3,9	3,5	3,9	ns	enable
Transition rise and fall times	$\frac{t_{TLH}}{t_{THL}}$	min.	1,1	1,1	1,1	ns	between 20% and 80%
		max.	3,7	3,3	3,7	ns	between 20% and 80%

For **switching times test circuit** and **waveform** see Family Specifications.

HEX INVERTER WITH ENABLE

The GXB10189 includes six inverters offering individual inputs and outputs and a common enable input, driving all outputs LOW. Each input is connected to V_{EE} via a 50 kΩ pull-down resistor resulting in high input impedance and eliminating the need of tying unused inputs LOW. Due to open emitter outputs the GXB10189 features OR capability with high fan-out for driving 50 Ω lines.

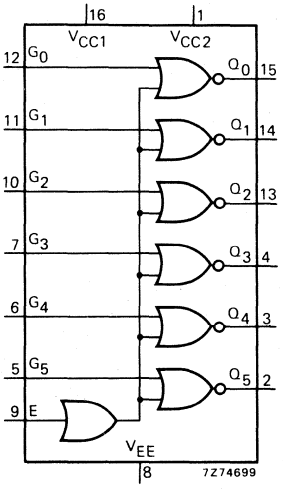


Fig. 1 Logic diagram.

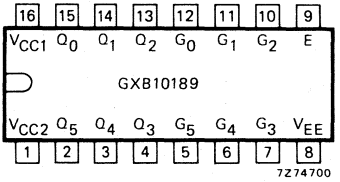


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 ± 10% V
Operating ambient temperature range	T_{amb}		−30 to +85 °C
Average propagation delay	t_{PLH}	typ.	2 ns
Output voltage HIGH state	V_{OH}	nom.	−880 mV
Output voltage LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_{av}	typ.	180 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (see Package Outlines)

GXB10189P: 16-lead DIL; plastic (SOT-38Z).
GXB10189D: 16-lead DIL; ceramic (SOT-74).

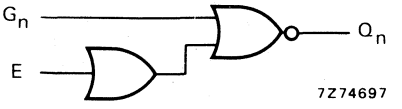


Fig. 3 Logic diagram (one inverter).

LOGIC FUNCTION

$Q_n = \overline{G_n + E}$

Positive logic

H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0

RATINGS see Family Specifications

D.C. CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground; $V_{EE} = -5{,}2$ V

	symbol		T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Input current HIGH							
Pins 5,6,7,10,11,12	I_{IH}	max.	425	265	265	ns	
Pin 9	I_{IH}	max.	890	555	555	ns	
Input current LOW	I_{IL}	min.	0,5	0,5	0,3	μA	
Supply current	I_{EE}	max.	44	40	44	mA	

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2$ V; $V_{EE} = -3{,}2$ V

	symbol		T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Rise and fall propagation delay times	t_{PLH} / t_{PHL}						
$G_n \rightarrow Q_n$		min.	1,0	1,0	1,0	ns	Data to output
		max.	3,3	2,9	3,3	ns	
$E \rightarrow Q_n$		min.	1,1	1,1	1,1	ns	Enable to output
		max.	3,9	3,5	3,9	ns	
Rise and fall transition time	t_{TLH} / t_{THL}	min.	1,1	1,1	1,0	ns	between 20% and 80%
		max.	3,7	3,3	3,7	ns	

For **switching times test circuit** and **waveform** see Family Specifications.

HEX ECL-MST TRANSLATOR

It includes six gates offering individual inputs and outputs and a common enable input, driving all outputs LOW when in the HIGH state. Each input is connected to V_{EE} via a 50 kΩ pull-down resistor resulting in high input impedance and eliminating the need of tying unused inputs LOW. Due to open emitter outputs the GXB10191 features OR capability with high fan-out for driving 50 Ω lines.

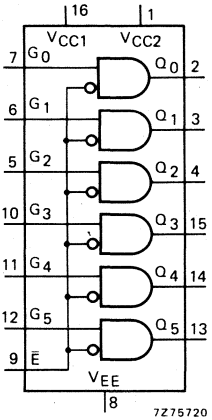


Fig. 1 Circuit diagram.

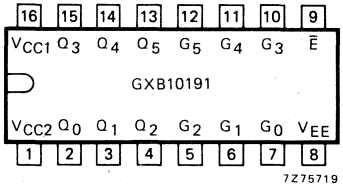


Fig. 2 Pinning diagram.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	−5,2 ± 10%	V
Operating ambient temperature range	T_{amb}	−30 to +85	°C
Average propagation delay	t_{PLH}	typ. 2,2	ns
Output voltage HIGH state	V_{OH}	nom. −880	mV
Output voltage LOW state	V_{OL}	nom. −1720	mV
Power consumption per package (no load)	P_{av}	typ. 180	mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (see Package Outlines)

GXB10191P: 16-lead DIL; plastic (SOT-38Z).
GXB10191D: 16-lead DIL; ceramic (SOT-74).

Fig. 3 Logic diagram (one gate).

LOGIC FUNCTION

$Q_n = G_n . \overline{E}$

FUNCTION TABLE

inputs		output
$\overline{E}$	G_n	Q_n
L	L	L
L	H	H
H	X	L

Positive logic
H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0
X = state is immaterial

D.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = –5,2 V.

	symbol		T_{amb} (°C) –30	+25	+85	unit	remarks
Input current HIGH							
pin 9	I_{IH}	max.	425	265	265	μA	
other pins	I_{IH}	max.	390	245	245	μA	
Input current LOW	I_{IL}	min.	0,5	0,5	0,3	μA	
Supply current	I_{EE}	max.	39	35	39	mA	
	I_{CC}	max.	23	23	23	mA	

A.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = –5,2 V.

	symbol		T_{amb} (°C) –30	+25	+85	unit	remarks
Rise and fall propagation delay times	t_{PLH} / t_{PHL}						
$G_n \rightarrow Q_n$		min.	1,0	1,0	1,0	ns	
		max.	3,6	3,4	3,7	ns	
$\overline{E} \rightarrow Q_n$		min.	1,0	1,0	1,0	ns	
		max.	4,7	4,5	5,0	ns	
Transition rise and fall time	t_{TLH} / t_{THL}	min.	1,1	1,1	1,1	ns	between 20% and 80%
		max.	4,5	4,3	4,7	ns	

For **switching times test circuit** and **waveforms** see Family Specifications.

	symbol	T_{amb} (°C)			unit	remarks
		−30	+25	+85		
Output voltage HIGH						
threshold HIGH	V_{OHA}	156	255	327	mV	
	V_{OHB}	374	440	548	mV	
	V_{OHC}	136	235	307	mV	
Output voltage LOW						
maximum	V_{OLA}	−323	−290	−254	mV	
minimum	V_{OLB}	−523	−490	−454	mV	
threshold	V_{OLC}	−303	−270	−234	mV	

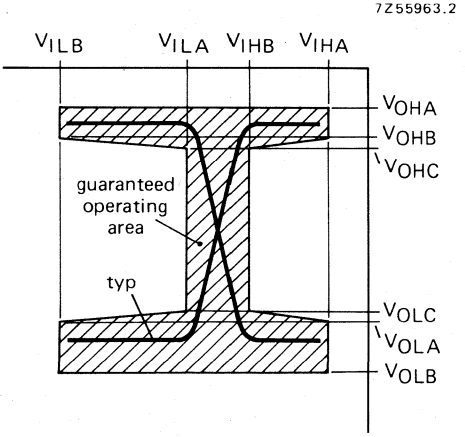


Fig. 4 Transfer characteristics.

DUAL 3-INPUT/3-OUTPUT OR LINE DRIVER

The GXB10210 is a high speed dual 3-input/3-output OR gate intended to drive up to six transmission lines simultaneously. This feature makes the device particularly useful in clock distribution applications. The GXB10210 is a higher speed version of the GXB10110. It is a pin-for-pin replacement for the device.

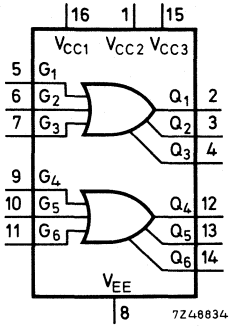


Fig. 1 Logic diagram.

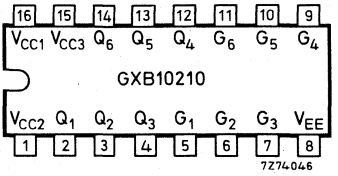


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = V_{CC3} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 ± 10% V
Operating ambient temperature range	T_{amb}		−30 to +85 °C
Average propagation delay	t_{PHL}	typ.	1,5 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_{av}	typ.	160 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (see Package Outlines)

GXB10210P: plastic 16-lead dual in-line (SOT-38).
GXB10210D: ceramic 16-lead dual in-line (SOT-74).

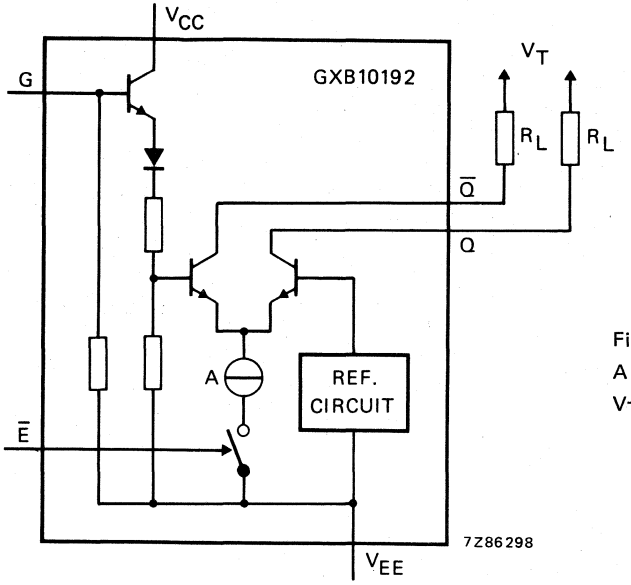


Fig. 3 Simplified circuit diagram.

A = 16 mA switched current source.

V_T should not exceed + 5,5 V and R_L and V_T should be chosen so that V_Q does not go more negative than −2,5 V.

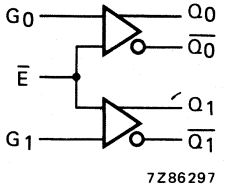


Fig. 4 Logic function.

Function table

inputs		output			
		current		voltage	
$\overline{E}$	G	$\overline{Q}$	Q	$\overline{Q}$	Q
L	L	L	H	H	L
L	H	H	L	L	H
H	X	L	L	H	H

Positive logic HIGH state = 1
LOW state = 0

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

Basic driver operation.

$V_{OH} = V_T$

$V_{OL} = V_T - 0{,}016.\ R_L$ (typ.)

FAMILY DATA and **RATINGS** see Family Specifications.

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = +2{,}0$ V; $V = -3{,}2$ V

	symbol		T_{amb} (°C) −35	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Propagation delay rise and fall times	t_{PLH} / t_{PHL}	min.	1,0	1,0	1,0	ns	
		max.	2,6	2,5	2,8	ns	
Transition rise and fall times	t_{TLH} / t_{THL}	min.	1,0	1,0	1,0	ns	between 20% and 80%
		max.	2,6	2,5	2,8	ns	between 20% and 80%

For **switching times test circuit and waveforms** see Family Specifications.

DUAL 3-INPUT/3-OUTPUT OR LINE DRIVER

The GXB10210 is a high speed dual 3-input/3-output OR gate intended to drive up to six transmission lines simultaneously. This feature makes the device particularly useful in clock distribution applications. The GXB10210 is a higher speed version of the GXB10110. It is a pin-for-pin replacement for the device.

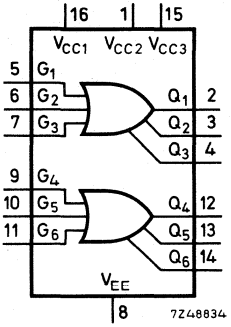


Fig. 1 Logic diagram.

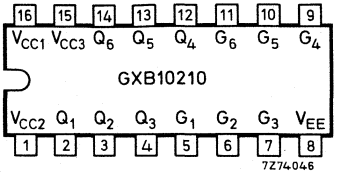


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = V_{CC3} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	$-5{,}2 \pm 10\%$	V
Operating ambient temperature range	T_{amb}	-30 to $+85$	°C
Average propagation delay	t_{PHL}	typ. 1,5	ns
Output voltage			
HIGH state	V_{OH}	nom. -880	mV
LOW state	V_{OL}	nom. -1720	mV
Power consumption per package (no load)	P_{av}	typ. 160	mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (see Package Outlines)

GXB10210P: plastic 16-lead dual in-line (SOT-38).
GXB10210D: ceramic 16-lead dual in-line (SOT-74).

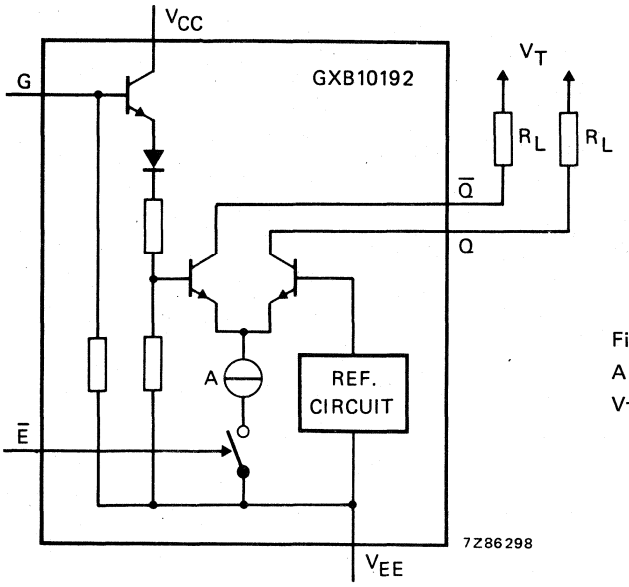


Fig. 3 Simplified circuit diagram.

A = 16 mA switched current source.

V_T should not exceed + 5,5 V and R_L and V_T should be chosen so that V_Q does not go more negative than −2,5 V.

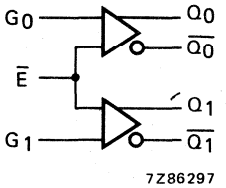


Fig. 4 Logic function.

Function table

inputs		output			
		current		voltage	
$\overline{E}$	G	$\overline{Q}$	Q	$\overline{Q}$	Q
L	L	L	H	H	L
L	H	H	L	L	H
H	X	L	L	H	H

Positive logic HIGH state = 1
LOW state = 0

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

Basic driver operation.

$V_{OH} = V_T$

$V_{OL} = V_T - 0{,}016.\ R_L$ (typ.)

FAMILY DATA and **RATINGS** see Family Specifications.

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = +2{,}0$ V; $V = -3{,}2$ V

	symbol		T_{amb} (°C) −35	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Propagation delay rise and fall times	t_{PLH}	min.	1,0	1,0	1,0	ns	
	t_{PHL}	max.	2,6	2,5	2,8	ns	
Transition rise and fall times	t_{TLH}	min.	1,0	1,0	1,0	ns	between 20% and 80%
	t_{THL}	max.	2,6	2,5	2,8	ns	between 20% and 80%

For **switching times test circuit and waveforms** see Family Specifications.

DUAL 3-INPUT/3-OUTPUT NOR LINE DRIVER

The GXB10211 is a high speed dual 3-input/3-output NOR gate intended to drive up to three transmission lines simultaneously. This feature makes the device particularly useful in clock distribution applications.

The GXB10211 is a higher speed version of the GXB10111. It is a pin-for-pin replacement for this type.

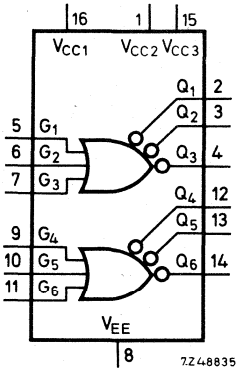


Fig. 1 Logic diagram.

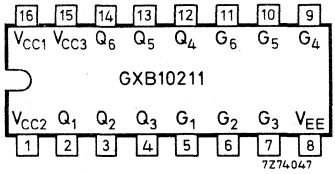


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = V_{CC3} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	−5,2 ± 10%	V
Operating ambient temperature range	T_{amb}	−30 to + 85	°C
Average propagation delay	t_{pd}	typ. 1,5	ns
Output voltage			
HIGH state	V_{OH}	nom. −880	mV
LOW state	V_{OL}	nom. −1720	mV
Power consumption per package	P_{av}	typ. 160	mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (see Package Outlines)

GXB10211P: plastic 16-lead dual in-line (SOT-38).
GXB10211D: ceramic 16-lead dual in-line (SOT-74).

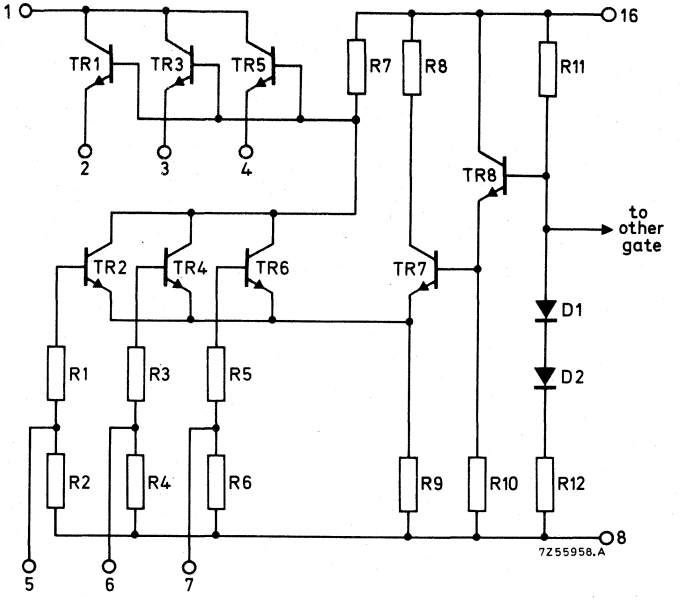
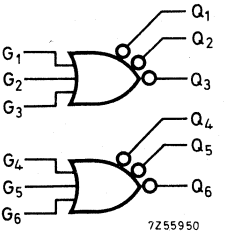


Fig. 3 Circuit diagram.



$$Q_1 = Q_2 = Q_3 = \overline{G_1 + G_2 + G_3}$$

$$Q_4 = Q_5 = Q_6 = \overline{G_4 + G_5 + G_6}$$

Positive logic: HIGH state = 1
LOW state = 0

Fig. 4 Logic function.

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = −5,2 V

	symbol		T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Input current							
HIGH	I_{IH}	max.	680	425	425	μA	
LOW	I_{IL}	min.	0,5	0,5	0,3	μA	
Supply current (d.c.)	I_{EE}	max.	42	38	42	mA	

A.C. CHARACTERISTICS

V_{CC1} = V_{CC2} = +2,0 V; V_{EE} = −3,2 V

	symbol		T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Propagation delay rise and fall times	t_{PLH}	min.	1,0	1,0	1,0	ns	
	t_{PHL}	max.	2,6	2,5	2,8	ns	
Transition rise and fall times	t_{TLH}	min.	1,0	1,0	1,0	ns	between 20% and 80%
	t_{THL}	max.	2,6	2,5	2,8	ns	between 20% and 80%

For **switching times test circuit and waveforms** see Family Specifications.

HIGH SPEED TRIPLE LINE RECEIVER

The GXB10216 is a high speed, triple differential amplifier designed for use in sensing differential signals over long lines. The bias supply (V_{BB}) is made available at pin 11 to make the device useful as a Schmitt trigger or in other applications where a stable reference voltage is necessary. Active current sources provide the GXB10216 with excellent common mode noise rejection. If any amplifier in a package is not used the input of that amplifier must be connected to V_{BB} (pin 11) to prevent upsetting the current source bias network.

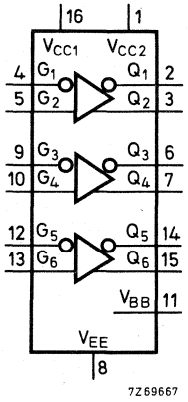


Fig. 1 Logic diagram.

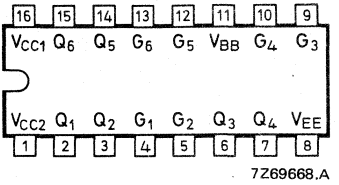


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = 5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 ± 10% V
Operating ambient temperature range	T_{amb}		−30 to + 85 °C
Average propagation delay			
single-ended input	t_{PLH}	typ.	1,8 ns
differential input	t_{PLH}	typ.	1,5 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_{av}	typ.	100 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (see Package Outlines)

GXB10216P : plastic 16-lead dual in-line (SOT-38).
GXB10216D: ceramic 16-lead dual in-line (SOT-74).

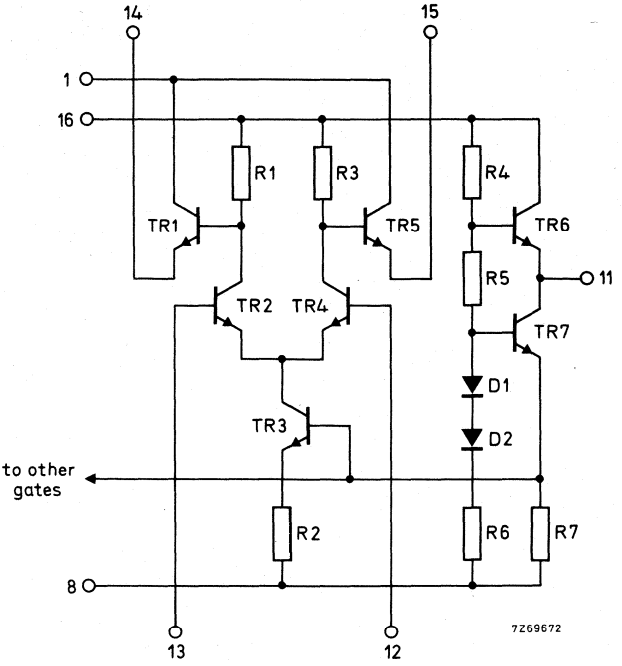
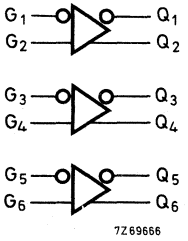


Fig. 3 Circuit diagram (one amplifier).



With inputs G_2, G_4 and G_6 connected to V_{BB} (pin 11)
$Q_1 = G_1$; $Q_2 = \overline{G}_1$; $Q_3 = G_3$; $Q_4 = \overline{G}_3$; $Q_5 = G_5$; $Q_6 = \overline{G}_5$.

Positive logic:

H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0

Fig. 4 Logic function.

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground; $V_{EE} = -5{,}2$ V.

	symbol		T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Input currents	I_{IH}	max.	180	115	115	μA	V_{IHA}
	I_{CBO}	max.	1,5	1,0	1,0	μA	V_{ILB}
Supply current	I_{EE}	max.	27	25	27	mA	
Reference voltage	V_{BB}	min.	−1420	−1350	−1295	V	
		max.	−1280	−1230	−1150	V	

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2$ V; $V_{EE} = -3{,}2$ V.

	symbol		T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Rise propagation delay time	t_{PLH}	min.	1,0	1,0	1,0	ns	
		max.	2,6	2,5	2,8	ns	
Fall propagation delay time	t_{PHL}	min.	1,0	1,0	1,0	ns	
		max.	2,6	2,5	2,8	ns	
Transition rise time	t_{TLH}	min.	1,0	1,0	1,0	ns	between 20% and 80%
		max.	2,6	2,5	2,8	ns	
Transition fall time	t_{THL}	min.	1,0	1,0	1,0	ns	
		max.	2,6	2,5	2,8	ns	

For **switching time test circuit** and **waveforms** see Family Specifications.

DUAL D-TYPE MASTER-SLAVE FLIP-FLOP

The GXB10231 is a high speed dual master-slave D-type flip-flop. It contains asynchronous set (S) and reset (R) which override clock (C) and clock enable ($\overline{C}_E$) inputs.
Each flip-flop may be clocked separately by using the enable inputs for the clocking function and holding the common clock in the LOW state. For the two flip-flops to be clocked, the common clock must be used with the clock enable inputs hold in the LOW state.
The outputs of the GXB10231 change state with the positive transition of the clock. Due to the master-slave structure of the device a change in the information present at the data (D) input will not modify the output information at any other time.
Unused inputs need not be tied to V_{EE} since input pull-down resistors are integrated in the circuit.

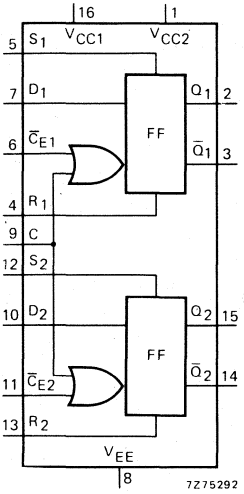


Fig. 1 Block diagram.

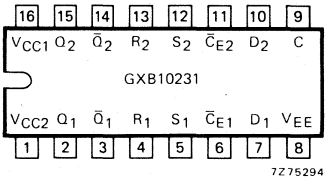


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	−5,2 ± 10%	V
Operating ambient temperature range	T_{amb}	−30 to +85	°C
Clock frequency	f_C	typ. 225	MHz
Output voltage			
HIGH state	V_{OH}	nom. −880	mV
LOW state	V_{OL}	nom. −1720	mV
Power consumption per package (no load)	P_{av}	typ. 270	mW

PACKAGE OUTLINES (see Package Outlines)

GXB10231P: 16-lead DIL; plastic (SOT-38).
GXB10231D: 16-lead DIL; ceramic (SOT-74).

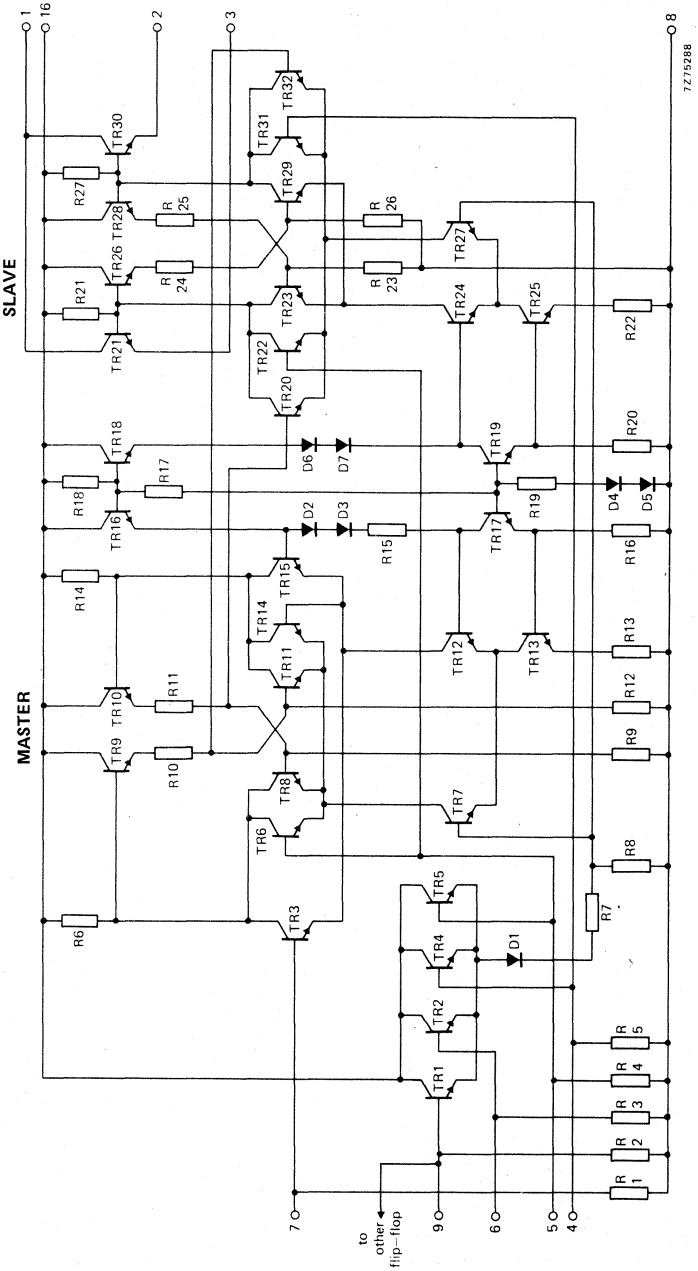


Fig. 3 Circuit diagram (one flip-flop).

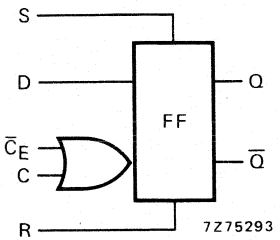


Fig. 4 Logic function.

C	D	Q_{n+1}
L	X	Q_n
H	L	L
H	H	H

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	*

* Not allowed

Positive logic HIGH state = 1
LOW state = 0

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

FAMILY DATA and **RATINGS** see Family Specifications.

D.C. CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground; $V_{EE} = -5{,}2$ V

	symbol		T_{amb} (°C) −30	+25	+85	unit	remarks
Input current HIGH							
pins 6, 7, 10, 11	I_{IH}	max.	350	220	220	μA	
pin 9	I_{IH}	max.	460	290	290	μA	
pins 4, 5, 12, 13	I_{IH}	max.	650	410	410	μA	
Input current LOW	I_{IL}	min.	0,5	0,5	0,3	μA	
Supply current	I_{EE}	max.	72	65	72	mA	

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2$ V; $V_{EE} = -3{,}2$ V

	symbol		T_{amb} (°C) −30	+25	+85	unit	remarks
Rise and fall propagation delay times	t_{PLH} / t_{PHL}						
C → Q		min.	1,5	1,5	1,6	ns	
		max.	3,4	3,3	3,7	ns	
S, R → Q		min.	1,1	1,1	1,2	ns	
		max.	3,4	3,3	3,7	ns	
Set-up time	t_s	min.	1,5	1,0	1,5	ns	
Hold time	t_h	min.	0,9	0,75	0,9	ns	
Clock frequency	f_C	min.	200	200	200	MHz	
Transition rise and fall times	t_{TLH} / t_{THL}	min.	0,9	1,0	1,0	ns	between 20% and 80%
		max.	3,3	3,1	3,6	ns	

For **switching times test circuit measurement of propagation** and **waveforms** see Family Specifications.

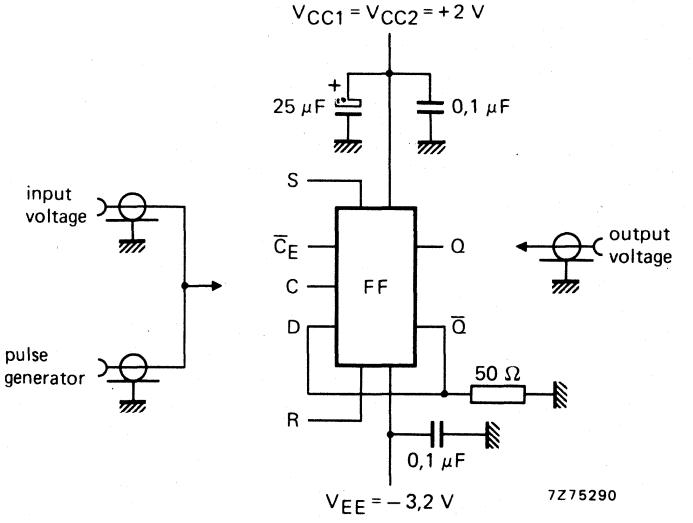


Fig. 5 Measurement of clock frequency.

1024-BIT, 1-BIT PER WORD RANDOM ACCESS MEMORIES

The GXB10415 devices are 1024-bit random access memories (RAMs) organized in 1024 one-bit words. They feature complete full address decoding, separate data input, non-inverted data output with wired-OR capabilities and one active LOW chip select input.

Input pull-down resistors (50 kΩ) on the chip select inputs allow these inputs to be left open if unused.

These circuits are intended for use in high-speed scratch pad, control and buffer storage applications.

They are voltage compensated and compatible with all GX family circuits, with maximum access times of 20, 15 and 10 ns.

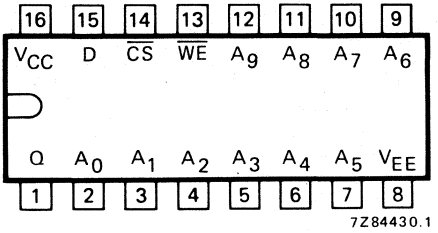


Fig. 1 Pin designation. GXB10415L; AL; BL.

Pin abbreviations:

$\overline{CS}$	chip select input	$\overline{WE}$	write enable input
A_0 to A_9	address inputs		
D	data input	V_{CC} = 0 V (ground)	
Q	data output	V_{EE} = −5,2 V	

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 ± 5% V
Operating ambient temperature range	T_{amb}		0 to +75 °C
Average propagation delay			
GXB10415	t_{PHL}	typ.	12 ns
10415A	t_{PHL}	typ.	8 ns
10415B	t_{PHL}	typ.	6 ns
Supply current	I_{EE}	typ.	115 mA
Output voltage HIGH state	V_{OH}	typ.	−880 mV
Output voltage LOW state	V_{OL}	typ.	−1720 mV
Power consumption per package (no load)	P_{av}	typ.	600 mW

For FAMILY DATA see Family Specifications.

PACKAGE OUTLINES

GXB10415LD; ALD; BLD; 16-lead DIL; ceramic (SOT-74).

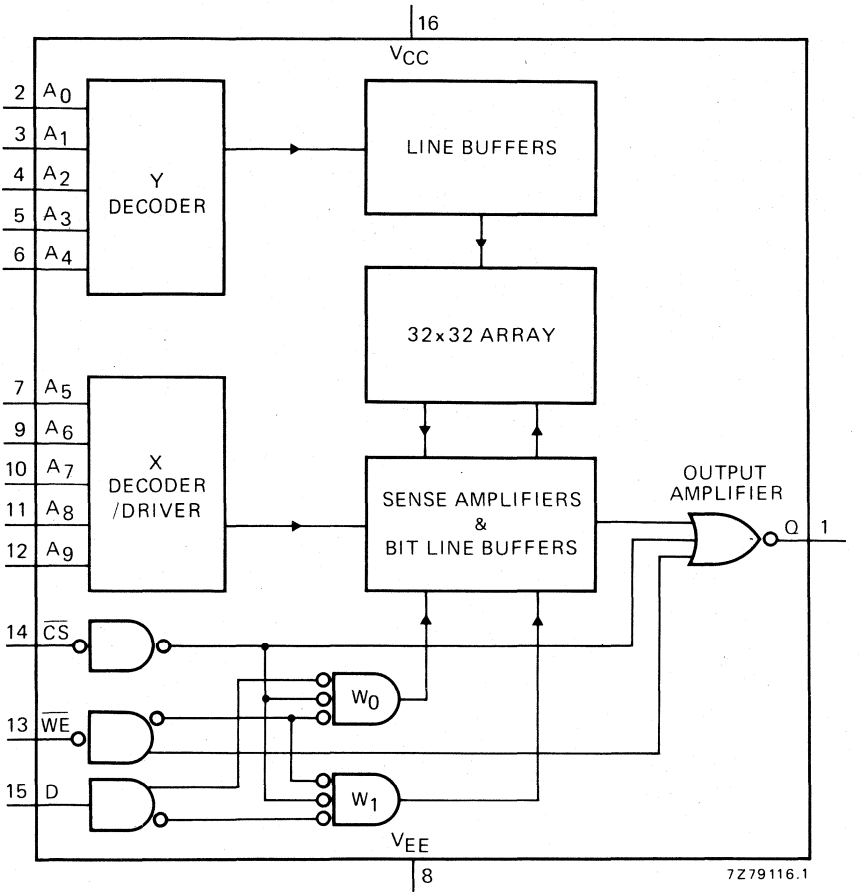


Fig. 2 Block diagram.

LOGIC FUNCTION

$W_0 = \overline{D} \,.\, WE \,.\, CS$
$W_1 = D \,.\, WE \,.\, CS$

FUNCTION TABLE

inputs			output	mode
$\overline{CS}$	$\overline{WE}$	D	Q	
H	X	X	L	not selected
L	L	L	L	write "0"
L	L	H	L	write "1"
L	H	X	D	read

Positive logic
H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0
X = state is immaterial

FUNCTIONAL DESCRIPTION

A_0 to A_9 (10-bit addresses) provide the bit selection; the active LOW chip select input and open emitter output allow memory expansion by using wired-OR connection. Read and write operations are controlled by the active LOW write enable ($\overline{WE}$). When $\overline{WE}$ is held in the LOW state and the chip select input ($\overline{CS}$) is LOW the data at D is written into the addressed location. When $\overline{WE}$ is held in the HIGH state and $\overline{CS}$ is LOW, data in the addressed location is read at Q. Q is LOW except when reading a stored HIGH state.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (d.c.)	V_{EE}	+0,5 to −7 V
Input voltage	V_I	0,5 V to V_{EE}
Output current	I_O	max. 30 mA
Storage temperature	T_{stg}	−55 to + 150 °C

D.C. CHARACTERISTICS *

V_{CC} = ground; V_{EE} = −5,2 V ± 5%

Each GX circuit has been designed to meet the d.c. specifications shown in the test table below, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed-circuit board and transverse air flow > 2,5 m/s is maintained.
Outputs are terminated via a 50 Ω resistor to −2,0 V. Test values for applied conditions are given in the table and defined in the figure.

	symbol	pin under test	T_{amb} (°C) 0	25	75	conditions pin	test value
Input current HIGH	I_{IH} max	2,13,15 14	220	220	220 µA	2,13,15 14	V_{IHmax}
Input current LOW	I_{IL} min.	2,13,15 14	−6 10	−6 10	−6 µA 10 µA	2,13,15 14	V_{ILmin}
Supply current	I_{EE} typ. max.	8	− 150	115 150	− mA 150 mA	all inputs	V_{ILmin}

* For FAMILY DATA see Family Specifications.

A.C. CHARACTERISTICS

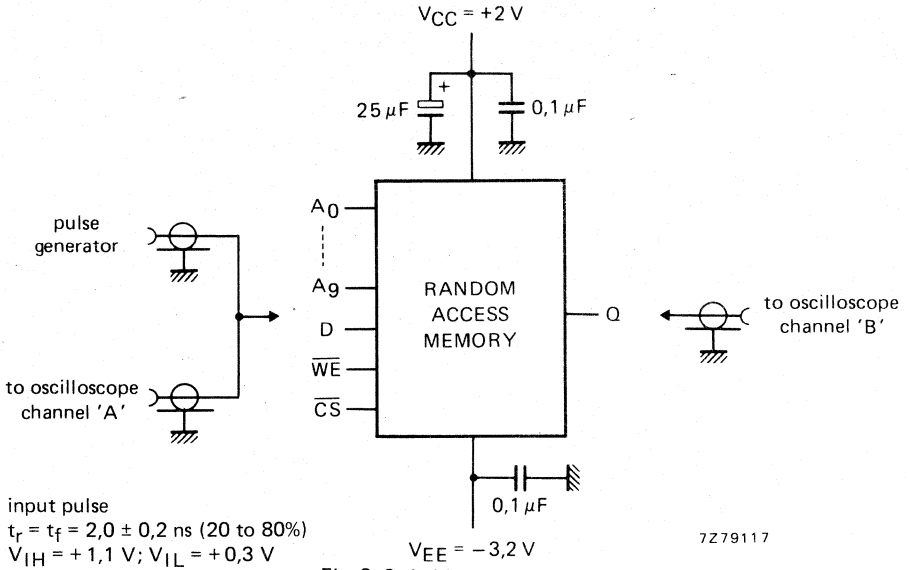
$V_{EE} = -5{,}2\ V \pm 5\%$; $T_{amb} = 0$ to $+75\ ^{o}C$

	symbol	pin under test	min.	typ.	max.	unit	conditions	remarks
Read mode								
Chip select								
access time	t_{ACS}	1	–	3	5	ns	see Fig. 4	
recovery time	t_{RCS}	1	–	3	5	ns		
Address								
access time	t_{AA}	1	–	12	20	ns	see Fig. 5	GXB10415
			–	8	15	ns		GXB10415A
			–	6	10	ns		GXB10415B
Write mode								
Write		1	12	8	–	ns	see Fig. 6	GXB10415
pulse duration	t_W	1	10	7	–	ns		GXB10415A
		1	8	6	–	ns		GXB10415B
Set-up times								
D → $\overline{WE}$	t_{WSD}	1	2	–	–	ns		
A → $\overline{WE}$	t_{WSA}	1	1	–	–	ns		
$\overline{CS}$ → $\overline{WE}$	t_{WSC}	1	2	–	–	ns		GXB10415 t_W = 12 ns
Hold times								GXB10415A t_W = 10 ns
$\overline{WE}$ → D	t_{WHD}	1	2	–	–	ns		GXB10415B t_W = 8 ns
$\overline{WE}$ → A	t_{WHA}	1	3	–	–	ns		
$\overline{WE}$ → $\overline{CS}$	t_{WHC}	1	2	–	–	ns		
Write								
disable time	t_{WS}	1	6	2	–	ns		
recovery time	t_{WR}	1	10	2	–	ns		
Transition							input pulse on all inputs except 13	
rise time	t_{TLH}	1	0,5	2	–	ns		
fall time	t_{THL}	1	0,5	2	–	ns		
Input								
Capacitance	C_{in}	15	–	–	5	pF		
Output								
Capacitance	C_{out}	1	–	–	5	pF		

Notes

1. Non-specified input pins should be connected to V_{ILmin} or left open.
2. Input and output cables to the oscilloscope are 50 Ω coaxial cables with equal length.
3. Input impedance of the oscilloscope is 50 Ω.
4. The unmatched wire stub between coaxial cable and pins under test must be less than 6 mm long for proper tests.

Set-up times are the minimum times before the transition of the write pulse.
Hold times are the minimum times after the transition of the write pulse.



input pulse
$t_r = t_f$ = 2,0 ± 0,2 ns (20 to 80%)
V_{IH} = +1,1 V; V_{IL} = +0,3 V

Fig. 3 Switching times test circuit.

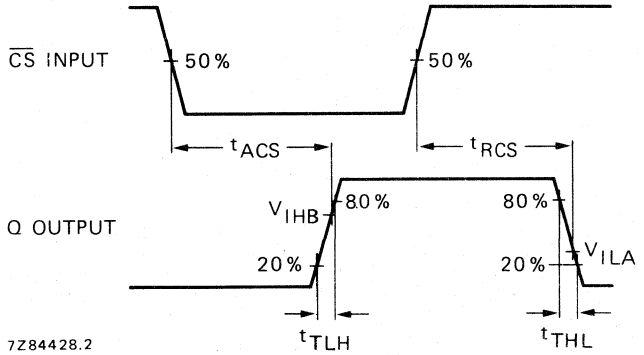


Fig. 4 Read mode propagation delay from chip select.

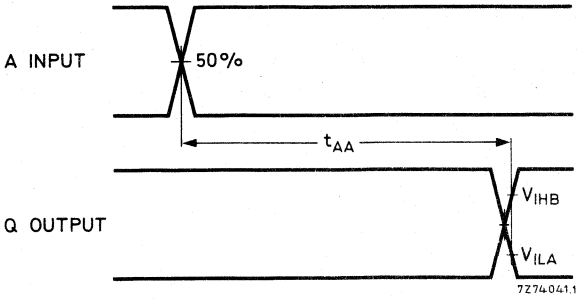


Fig. 5 Read mode propagation delay from address.

CHARACTERISTICS (continued)

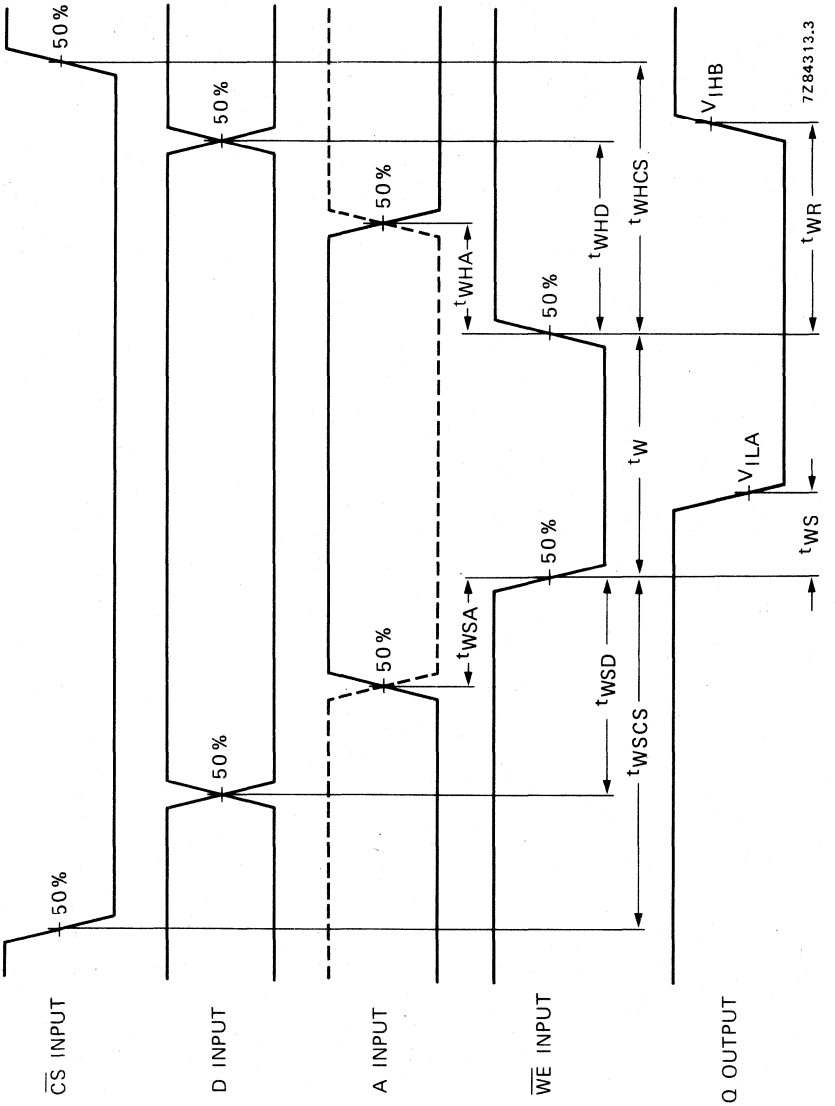


Fig. 6 Write mode waveforms.

256-WORD BY 4-BIT READ/WRITE RAM

The GXB10422 devices are 256-word by 4-bit fully decoded ECL read/write random access memories, containing voltage and temperature compensation circuits. They may be reconfigured as 512 x 2 or 1024 x 1 organization by utilizing the block select feature. Each block has its own, low active, block select to enable the output. Write enable, low active, enables the write function in selected blocks.

The outputs require external resistance terminations as they are not connected internally through resistance to the supply voltage. The input pull-down resistor to V_{EE} is 50 kΩ typical for the block selects.

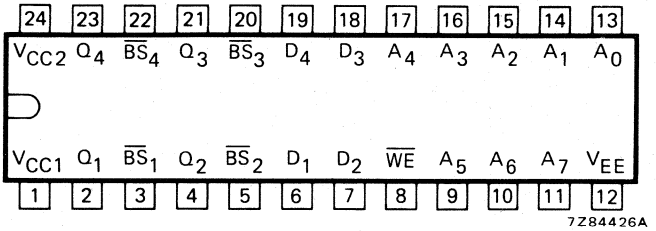


Fig. 1 Pin designation.

V_{EE} = −5,2 V; V_{CC1} = V_{CC2} = 0 V (ground).

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 ± 5% V
Operating ambient temperature range	T_{amb}		0 to 75 °C
Average propagation delay			
GXB10422	t_{PLH}	typ.	10 ns
GXB10422A	t_{PLH}	typ.	7,5 ns
GXB10422B	t_{PLH}	typ.	6 ns
Output voltage HIGH state	V_{OH}	nom.	−880 mV
Output voltage LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_{av}	typ.	980 mW

For FAMILY DATA see chapter Family Specifications.

PACKAGE OUTLINE

GXB10422D; GXB10422AD; GXB10422BD: 24-lead DIL; ceramic (slim cerdip); SOT-149.

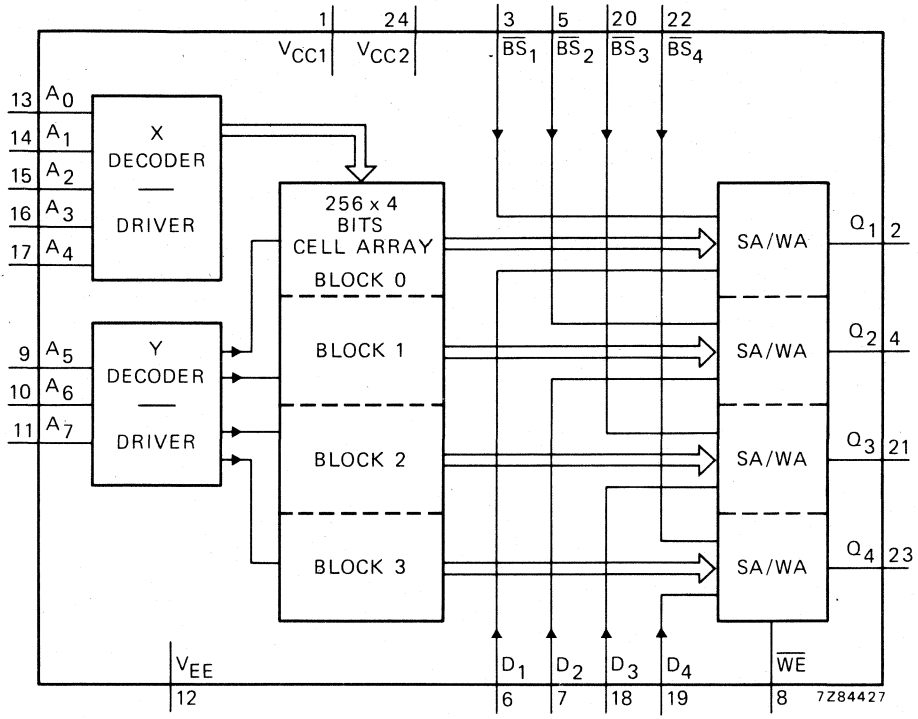


Fig. 2 Block diagram.

FUNCTION TABLE

inputs			outputs	mode
$\overline{BS}$	$\overline{WE}$	D	Q	
H	X	X	L	diable
L	L	L	L	write 0
L	L	H	L	write 1
L	H	X	Q	read

Positive logic:

H = HIGH state = 1
(the more positive voltage)

L = LOW state = 0
(the less positive voltage)

X = state is immaterial

$\overline{BS_1}$ to $\overline{BS_4}$	block select input
$\overline{WE}$	write enable input
D_1 to D_4	data inputs
A_0 to A_7	address inputs
Q_1 to Q_4	data inputs

V_{EE} = –5,2 V

V_{CC1}, V_{CC2} = 0 V (ground)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (d.c.)	V_{EE}	+0,5 to −7 V
Input voltage	V_I	0,5 V to V_{EE}
Output current (d.c.) HIGH state	I_O	30 mA
Storage temperature	T_{stg}	−55 to + 150 °C

D.C. CHARACTERISTICS* V_{CC} = ground; V_{EE} = −5,2 V ± 5%

Each GX circuit has been designed to meet the d.c. specifications shown in the test table below, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow > 2,5 m/s is maintained.
Outputs are terminated via a 50 Ω resistor to −2,0 V. Test values for applied conditions are given in the table and defined in the figure.

	symbol	pin under test	T_{amb} (°C) 0	25	75		conditions pin	test value
Output voltage HIGH	V_{OHB}	2	−1000	−960	−900	mV	6	V_{IHA}
	V_{OH} typ.	2	–	−880	–	mV		
	V_{OHA}	2	−840	−810	−720	mV		
Output voltage LOW	V_{OHB}		−1,870	−1,850	−1,830	V	6	V_{ILB}
	V_{OL} typ.	2	–	−1,720	–	V		
	V_{OHA}		−1,665	−1,650	−1,625	V		
Output threshold voltage HIGH	V_{OHC}	2	−1020	−980	−920	mV	6	V_{IHB}
Output threshold voltage LOW	V_{OLC}	2	−1,645	−1,630	−1,605	V	6	V_{ILA}
Input current HIGH	I_{IH} max.		220	220	220	μA		V_{IHA}
Input current LOW	I_{IL} min.	3,5,20,22 other inputs	10	10	10	μA	6,8,11	
			−6	−6	−6	μA	3	V_{ILB}
Supply current	I_{EE} typ.	12	–	−180	–	mA	every input	V_{ILB}
	I_{EE} max.		−210	−210	−210	mA		

* See for FAMILY DATA chapter Family Specifications.

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 0$ V; $V_{EE} = -5{,}2$ V ± 5% $R_L = 50\ \Omega$ to -2 V; $T_{amb} = 0$ to $+75$ °C

	symbol	min.	typ.	max.	unit	remarks
Read mode						
Block select						
access time	t_{ABS}	–	3	5	ns	
recovery time	t_{RBS}	–	3	5	ns	
Address						
access time	t_{AA}	–	10	20	ns	GXB10422
access time	t_{AA}	–	7,5	15	ns	GXB10422A
access time	t_{AA}	–	6	10	ns	GXB10422B
Write mode						
Write						
pulse duration	t_W	12	8	–	ns	GXB10422
pulse duration	t_W	10	7	–	ns	GXB10422A
pulse duration	t_W	8	5,5	–	ns	GXB10422B
Set-up times						
A → $\overline{WE}$	t_{WSA}	2	–	–	ns	GXB10422 t_W = 12 ns GXB10422A t_W = 10 ns GXB10422B t_W = 8 ns
$\overline{BS}$ → $\overline{WE}$	t_{WSBS}	3	–	–	ns	
D → $\overline{WE}$	t_{WSD}	3	–	–	ns	
Hold times						
$\overline{WE}$ → A	t_{WHA}	5	–	–	ns	
$\overline{WE}$ → $\overline{BS}$	t_{WHBS}	4	–	–	ns	
$\overline{WE}$ → D	t_{WHD}	4	–	–	ns	
Write						
disable time	t_{WS}	–	3	5	ns	
recovery time	t_{WR}	–	6	9	ns	
Output						
rise time	t_{TLH}	0,5	2	–	ns	
fall time	t_{THL}	0,5	2	–	ns	
Capacitance						
input pin	C_{IN}	–	–	8	pF	
output pin	C_{OUT}	–	–	8	pF	

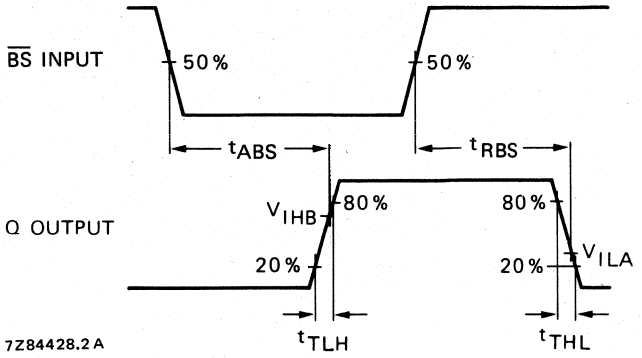


Fig. 3 Read mode propagation delay from block select.

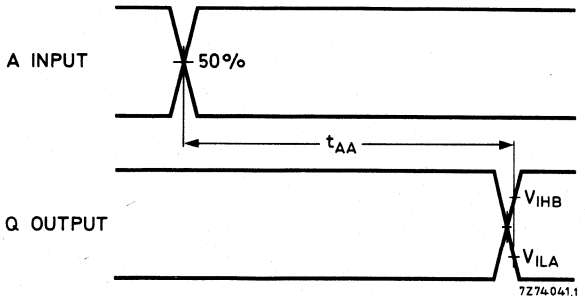


Fig. 4 Read mode propagation delay from address.

Notes

1. Non-specified input pins should be connected to V_{ILmin} or left open.
2. Input and output cables to the oscilloscope are 50 Ω coaxial cables with equal length.
3. Input impedance of the oscilloscope is 50 Ω.
4. The unmatched wire stub between coaxial cable and pins under test must be less than 6 mm long for proper tests.

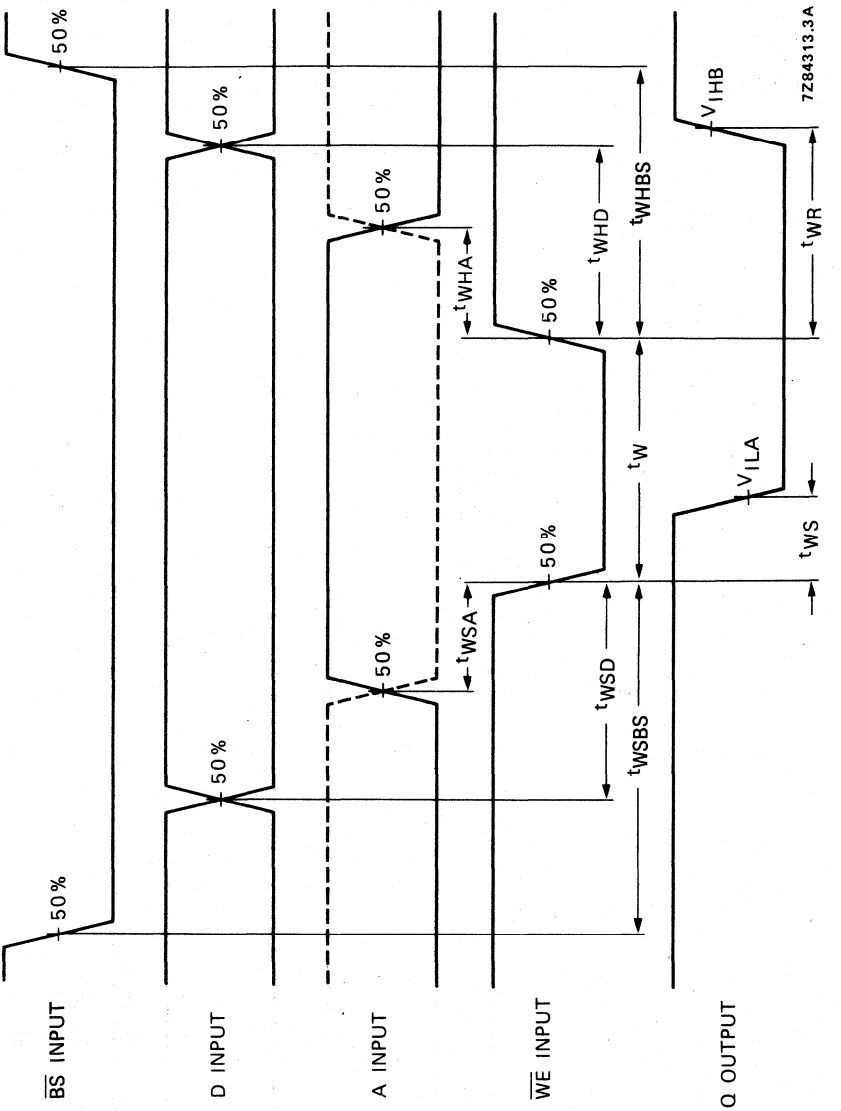


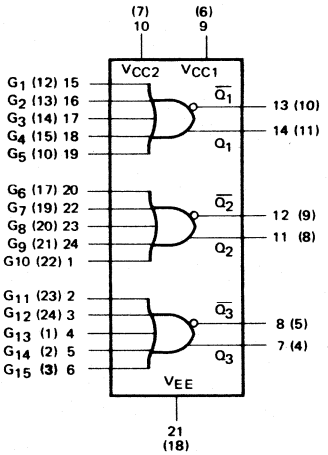
Fig. 5 Write mode waveforms.

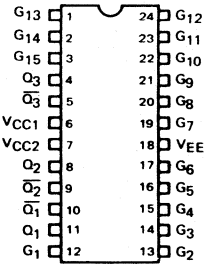
DEVICE DATA

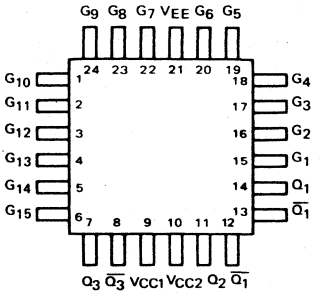
HX family (ECL100 000)

TRIPLE 5 - INPUT OR/NOR GATE

100101 is a triple 5 - Input OR/NOR gate.
Each gate has an OR and a NOR output.







Pin connections for flat pack and in ( ) for SLIM DIP packages.

QUICK REFERENCE DATA

Average propagation delay	t_P	typ.	0.8	ns
Power consumption per package	$P_{(AV)}$	typ.	120	mW

PACKAGE OUTLINE (See general section)

ORDERING INFORMATION : 100101 F (FO 44-24 lead ceramic flat pack)

100101 D (FO 72-24 lead Slim Cerdip)

TRUTH TABLE

Inputs					Outputs	
15 (12)	16 (13)	17 (14)	18 (15)	19 (16)	13 (10)	14 (11)
20 (17)	22 (19)	23 (20)	24 (21)	1 (22)	12 (9)	11 (8)
2 (23)	3 (24)	4 (1)	5 (2)	6 (3)	8 (5)	7 (4)
L	L	L	L	L	H	L
H	x	x	x	x	L	H
x	H	x	x	x	L	H
x	x	H	x	x	L	H
x	x	x	H	x	L	H
x	x	x	x	H	L	H

Positive logic : H = HIGH state (more positive voltage) = 1

L = LOW state (less positive voltage) = 0

x = Immaterial state (H or L).

RATINGS (See family specifications)

D.C. CHARACTERISTICS at V_{CC} = ground ; V_{EE} = −4.5 V
(for test table and diagram, see family specifications)

	Symbol		T_{amb} (°C) 0 to + 85		Conditions
Input current LOW	I_{IL}	min.	0.5	μA	Apply −1.81 ± 0.005 V to each input, one at a time, with all other inputs open.
Input current HIGH	I_{IH}	max.	340	μA	Apply − 0.88 ± 0.005 V to each input, one at a time, with all other inputs open.
Supply current	$-I_{EE}$	min. typ. max.	18 27 38	mA mA mA	Apply − 0.95 ± 0.005 V to all inputs.
			T_{amb} (° C) : 25		
Voltage compensation	$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	max	0.05		
	$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	max.	0.025		

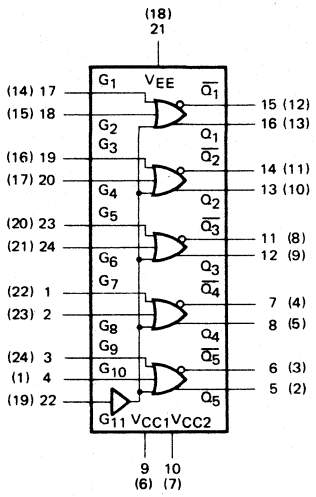
A.C CHARACTERISTICS at VCC = ground; V_{EE} = −4.5 V; load = 50 Ω to − 2 V; t_{amb} = 25° C

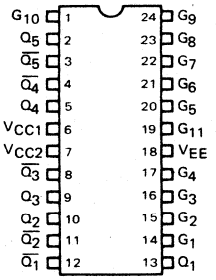
	Symbol		min.	typ.	max.	Conditions
Propagation Delay time OR-NOR	t_{PDQ}	(ns)	0.45		0.95	Apply a reference signal to each input, one at a time, with all other inputs open.
Rise time	t_{TLH}	(ns)	0.5		1.1	Same conditions.
Fall time	tTHL	(ns)	0.5		1.1	Same conditions.

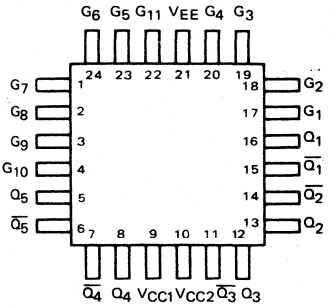
These limits are for flat pack.
Add 0.2 ns to max. values for SLIM DIP package propagation delays.

QUINTUPLE 2 - INPUT OR-NOR GATE WITH COMMON ENABLE

100102 circuit has five 3-input gates. One input is common to all five gates.







Pin connections for flat pack and in ( ) for SLIM DIP packages.

QUICK REFERENCE DATA

Average propagation delay	t_P	typ.	0.8	ns
Power consumption per package	$P_{(AV)}$	typ.	248	mW

PACKAGE OUTLINE (See general section)

ORDERING INFORMATION : 100102 F (FO 44-24 lead ceramic flat pack)
100102 D (FO 72-24 lead Slim Cerdip)

TRUTH TABLE

Inputs			Outputs	
4	3	22	5	6
2	1	22	8	7
24	23	22	12	11
20	19	22	13	14
18	17	22	16	15
x	x	H	H	L
x	H	x	H	L
H	x	x	H	L
L	L	L	L	H

Positive logic : H = HIGH state (more positive voltage) = 1
L = LOW state (less positive voltage) = 0
x = Immaterial state (H or L).

RATINGS (See family specifications)

D.C. CHARACTERISTICS at V_{CC} = ground ; V_{EE} = − 4.5 V
(for test table and diagram, see family specifications)

	Symbol		T_{amb} (°C) 0 to + 85	Conditions
Input current LOW	I_{IL}	min.	0.5 μA	Apply − 1.81 ± 0.005 V to each input, one at a time, with all other inputs open.
Input current HIGH	I_{IH}	max.	300 μA pin 22 (19) 350 μA other inputs	Apply − 0.88 ± 0.005 V to each input, one at a time, with all other inputs open.
Supply current	$-I_{EE}$	min. typ. max.	38 mA 55 mA 80 mA	Apply − 0.95 ± 0.005 V to all inputs.
			T_{amb} (° C) : 25	
Voltage compensation	$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	max	0.05	
	$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	max.	0.025	

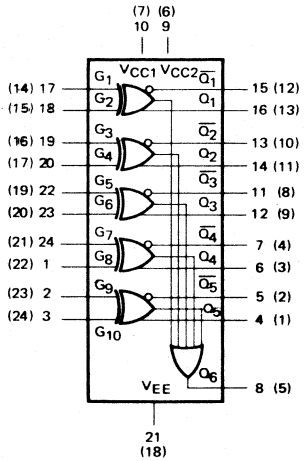
A.C CHARACTERISTICS at V_{CC} = ground; V_{EE} = − 4.5 V; load = 50 Ω to − 2 V; t_{amb} = 25° C

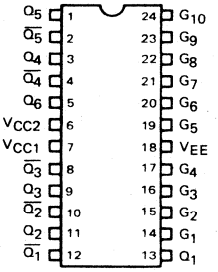
	Symbol		min.	typ.	max.	Conditions
Propagation Delay time OR-NOR	t_{PDQ}	(ns)	1.0 Pin 22 (19) 0.45 other pins		1.95 0.95	Apply a reference signal to each input one at a time, with all other inputs open.
Rise time	t_{TLH}	(ns)	0.5		1.10	Same conditions.
Fall time	t_{THL}	(ns)	0.5		1.10	Same conditions.

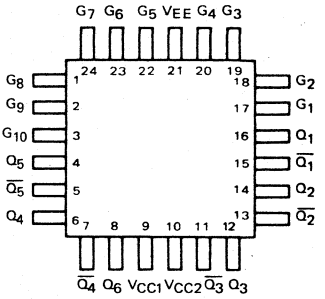
These limits are for flat pack.
Add 0.2 ns to max. values for SLIM DIP package propagation delays.

QUINTUPLE EXCLUSIVE OR-NOR GATE WITH COMPARE

100107 has five 2-input, 2-output exclusive OR-NOR gates with a compare output.







Pin connections for flat pack and in ( ) for SLIM DIP packages.

QUICK REFERENCE DATA

Average propagation delay	t_P	typ.	0.95	ns
Power consumption per package	$P_{(AV)}$	typ.	280	mW

PACKAGE OUTLINE (See general section)

ORDERING INFORMATION : 100107 F (FO 44-24 lead ceramic flat pack)
100107 D (FO 72-24 lead Slim Cerdip)

TRUTH TABLE

Inputs					Output
17 ⊕ 18 (14 ⊕ 15)	19 ⊕ 20 (16 ⊕ 17)	22 ⊕ 23 (19 ⊕ 20)	24 ⊕ 1 (21 ⊕ 22)	2 ⊕ 3 (23 ⊕ 24)	8 (5)
L	L	L	L	L	L
H	x	x	x	x	H
x	H	x	x	x	H
x	x	H	x	x	H
x	x	x	H	x	H
x	x	x	x	H	H

Inputs		Outputs	
17 (14)	18 (15)	16 (13)	15 (12)
19 (16)	20 (17)	14 (11)	13 (10)
22 (19)	23 (20)	12 (9)	11 (8)
24 (21)	1 (22)	6 (3)	7 (4)
2 (23)	3 (24)	4 (1)	5 (2)
L	L	L	H
L	H	H	L
H	L	H	L
H	H	L	H

⊕ = exclusive OR

Positive logic : H = HIGH state (more positive voltage) = 1
L = LOW state (less positive voltage) = 0
x = Immaterial state (H or L)

RATINGS (See family specifications)

D.C. CHARACTERISTICS at V_{CC} = ground ; V_{EE} = −4.5 V

(for test table and diagram, see family specifications)

	Symbol	T_{amb} (°C) 0 to + 85	Conditions
Input current LOW	I_{IL} min.	0.5 μA	Apply −1.81 ± 0.005 V to each input, one at a time, with all other inputs open.
Input current HIGH	I_{IH} max.	250 μA	Apply −0.88 ± 0.005 V to the listed inputs, one at a time, with all other inputs open.
	pin 3, 18, 20, 23, 24 (24) (15) (17) (20) (21)	250 μA	
	pin 1, 2, 17, 19 22 (22) (23)(14) (16) (19)	350 μA	Same conditions
Supply current	$-I_{EE}$ min.	46 mA	Apply − 0.95 ± 0.005 V to all inputs
	max.	96 mA	
		T_{amb} (°C): 25	
Voltage compensation	$\frac{\Delta V_{OH}}{\Delta V_{EE}}$ max.	0.025	
	$\frac{\Delta V_{OL}}{\Delta V_{EE}}$ max.	0.05	

A.C. CHARACTERISTICS at VCC = ground; V_{EE} = −4.5 V; load = 50 Ω to −2 V; T_{amb} = 25°C

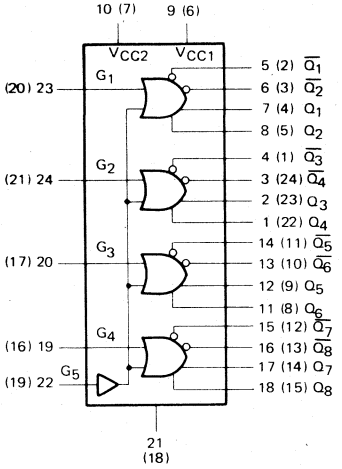
	Symbol	min.	typ.	max.	Conditions
Propagation delay time	t_{PDQ} (ns) pin 1, 2, 17, 19, 22 (22) (23) (14) (16) (19)	0.55		1.20	Apply a reference signal to each input, one at a time with all other inputs LOW. Repeat with all other inputs HIGH.
	other inputs	0.55		1.55	
Propagation delay time to pin 8 (5)	t_{PDQ} (ns)	1.25		2.75	Same conditions
Rise time	t_{TLH} (ns)	0.5		1.2	Apply a reference signal to each input, one at a time, with all other inputs open.
Fall time	t_{THL} (ns)	0.5		1.2	Same conditions

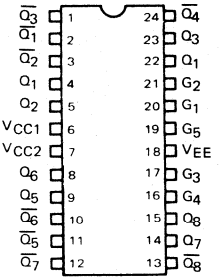
These limits are for flat pack.

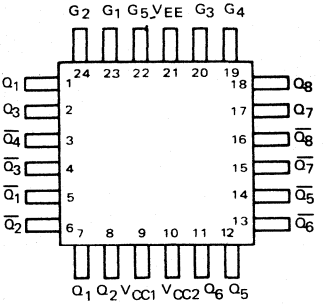
Add 0.2 ns to max. values for SLIM DIP package propagation delays.

QUADRUPLE DOUBLE FAN-OUT OR-NOR GATE

100112 has four 2-input OR-NOR gates, with one common input.
Each gate has two OR outputs and two NOR outputs.







Pin connections for flat pack and in ( ) for SLIM DIP packages.

QUICK REFERENCE DATA

Average propagation delay	t_P	typ.	1 1.3	ns ns	(Input 22)
Power consumption per package	$P_{(AV)}$	typ.	310	mW	

PACKAGE OUTLINE (See general section)

ORDERING INFORMATION : 100112 F (FO 44-24 lead ceramic flat pack)

100112 D (FO 72-24 lead Slim Cerdip)

TRUTH TABLE

Inputs		Outputs			
19 (16)	22 (19)	15 (12)	16 (13)	17 (14)	18 (15)
20 (17)	22 (19)	14 (11)	13 (10)	12 (9)	11 (8)
23 (20)	22 (19)	5 (2)	6 (3)	7 (4)	8 (5)
24 (21)	22 (19)	4 (1)	3 (24)	2 (23)	1 (22)
H	x	L	L	H	H
x	H	L	L	H	H
L	L	H	H	L	L

Positive logic : H = HIGH state (more positive voltage) = 1
L = LOW state (less positive voltage) = 0
x = Immaterial state (H or L)

RATINGS (See family specifications)

D.C. CHARACTERISTICS at V_{CC} = ground ; V_{EE} = −4.5 V
(for test table and diagram, see family specifications).

	Symbol		T_{amb} (°C) 0 to + 85	Conditions
Input current LOW	I_{IL}	min.	0.5 μA	Apply −1.81 ± 0.005 V to each input, one at a time, with all other inputs open.
Input current HIGH	I_{IH}	max.	450 μA pin22 (19) 550 μA other pins	Apply −0.88 ± 0.005 V to each input, one at a time, with all other inputs open.
Supply current	$-I_{EE}$	min. typ. max.	51 mA 71 mA 106 mA	Apply −0.95 ± 0.005 V to all inputs.
Voltage compensation	$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	max.	T_{amb} (°C): 25 0.025	
	$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	max.	0.05	

A.C. CHARACTERISTICS at V_{CC} = ground; V_{EE} = −4.5 V; load = 50 Ω to −2 V ; T_{amb} = 25°C

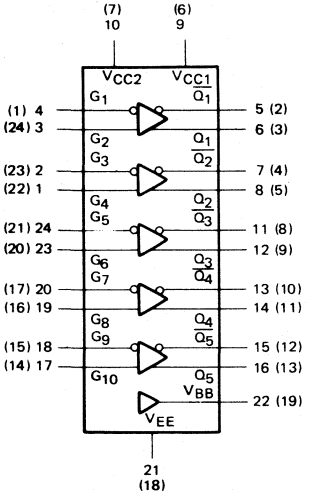
	Symbol	min.	typ.	max.	Conditions
Propagation delay	t_{PDQ} (ns) pin 19, 20, 23, 24 (16) (17) (20) (21)	0.55		1.20	Apply a reference signal to each input, one at a time, with all other inputs open.
	pin 22 (18)	0.85		1.70	
Rise time	t_{TLH} (ns)	0.45		1.4	Same conditions
Fall time	t_{THL} (ns)	0.45		1.4	Same conditions

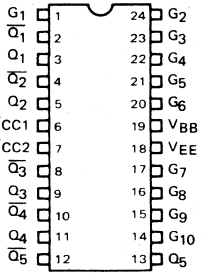
These limits are for flat pack.
Add. 0.2 ns to max. values, for SLIM DIP package propagation delays.

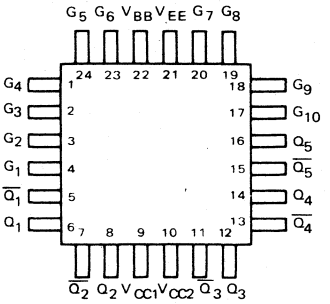
QUINTUPLE DIFFERENTIAL LINE RECEIVER

100114 contains five gates with differential inputs and complementary outputs. An internal reference is available (V_{BB}), which enables, when connected to a gate input, the other to operate as a standard 100 K ECL input.

The direct output of a gate goes LOW, and the complementary one goes HIGH, when both inputs are either open, or at V_{CC}, or have equal voltage applied.







Pin connections for flat pack and in ( ) for SLIM DIP packages.

QUICK REFERENCE DATA

Average propagation delay	t_P	typ.	1.40	ns
Power consumption per package	$P_{(AV)}$	typ.	390	mW
Operating high input voltage range			− 1.9 V to − 0.6 V	

PACKAGE OUTLINE (See general section)

ORDERING INFORMATION : 100114 F (FO 44-24 lead ceramic flat pack)
100114 D (FO 72-24 lead Slim Cerdip)

TRUTH TABLE

Inputs		Outputs	
18 (15)	17 (14)	15 (12)	16 (13)
20 (17)	19 (16)	13 (10)	14 (11)
24 (21)	23 (20)	11 (8)	12 (9)
2 (23)	1 (22)	7 (4)	8 (5)
4 (1)	3 (24)	5 (2)	6 (3)
H	V_{BB}	H	L
L	V_{BB}	L	H
V_{BB}	H	L	H
V_{BB}	L	H	L
$V_{ID} \geqslant 0$ V		H	L
$V_{ID} \leqslant -0.150$ V		L	H
-0.150 V $< V_{ID} < 0$ V		*	*
open	open	H	L
V_{CC}	V_{CC}	H	L

Positive logic : H = HIGH stage (more positive voltage) = 1
L = LOW state (less positive voltage) = 0
* = Indeterminate state
V_{BB} = Internal reference pin 22 (18)
V_{ID} = Complement to direct input voltage difference.

RATINGS (See family specifications)

D.C. CHARACTERISTICS at V_{CC} = ground ; V_{EE} = − 4.5 V
(for test table and diagram, see family specifications)

	Symbol		T_{amb} (°C) 0 to + 85	Conditions
Reference voltage	V_{BB}	min.	− 1.38 V	For I_{BB} from 0 to 475 μA
		typ.	− 1.32 V	
		max.	− 1.26 V	
Input current HIGH	I_{IH}		65 μA	V_{IN} = V_{IHA} second input to V_{BB} or open.
Supply current	− I_{EE}	min.	51 mA	Apply − 0.95 ± 0.005 V to all complement inputs and V_{BB} to all direct inputs.
		max.	110 mA	
Differential input voltage	V_{DIF}	typ.	150 mV	
Common mode voltage	V_{CM}	max.	0.65 V	Permissible common mode voltage with respect to V_{BB}.
			T_{amb} (°C): 25	
Voltage compensation	$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	max.	0.035	
	$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	max.	0.07	

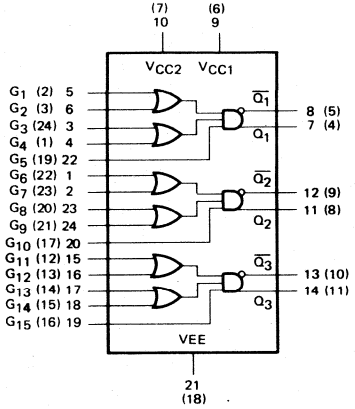
A.C. CHARACTERISTICS at V_{CC} = ground; V_{EE} = − 4.5 V; load = 50 Ω to − 2 V; T_{amb} = 25°C

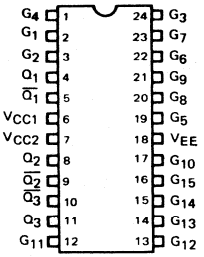
	Symbol		min.	typ.	max.	Conditions
Propagation delay time	t_{PDQ}	(ns)	0.65	1.40	2.2	Asymetric inputs : Apply V_{BB} to one input and a reference signal to the other inputs. Symetric inputs : Apply complementary signals to the inputs and measure delays to both outputs.
Rise time	t_{TLH}	(ns)	0.45	0.70	1.5	
Fall time	t_{THL}	(ns)	0.45	0.70	1.5	

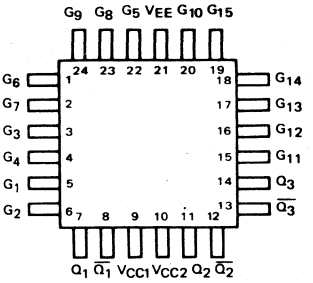
These limits are for flat pack.
Add 0.2 ns to max. values, for SLIM DIP package propagation delays.

TRIPLE 1 – 2 – 2 INPUT OR – AND, OR – NAND GATE

100117 has three 1 - 2 - 2 input OR/NAND gates with direct and complement outputs.







Pin connections for flat pack and in ( ) for SLIM DIP packages.

QUICK REFERENCE DATA

Average propagation delay	t_p	typ.	0.85	ns
			1.40	ns (OR input)
Power consumption per package	$P_{(AV)}$	typ.	245	mW

PACKAGE OUTLINE (See general section)

ORDERING INFORMATION : 100117 F (FO 44-24 lead ceramic flat pack)
100117 D (FO 72-24 lead Slim Cerdip)

TRUTH TABLE

Inputs					Outputs	
19 (16) 20 (17) 22 (19)	15 (12) 23 (20) 3 (24)	16 (13) 24 (21) 4 (1)	17 (14) 1 (22) 5 (2)	18 (15) 2 (23) 6 (3)	13(10) 12 (9) 8 (5)	14 (11) 11 (8) 7 (4)
L	x	x	x	x	H	L
x	L	L	x	x	H	L
x	x	x	L	L	H	L
H	H	x	H	x	L	H
H	x	H	x	H	L	H
H	H	x	x	H	L	H
H	x	H	H	x	L	H

Positive logic : H = HIGH state (More positive voltage) = 1
L = LOW state (Less positive voltage) = 0
x = Immaterial state (H or L)

RATINGS (See family specifications)

D.C. CHARACTERISTICS at V_{CC} = ground ; V_{EE} = − 4.5 V
(for test table and diagram see family specifications)

	Symbol	T_{amb} (°C) 0 to + 85	Conditions
Input current LOW	I_{IL} min.	0.5 μA	Apply −1.81 ± 0.005 V to each input, one at a time, with all other inputs open.
Input current HIGH	I_{IH} max.		Apply − 0.88 ± 0.005 V to each input, one at a time, with all other inputs open.
	OR inputs	220 μA	
	other inputs	350 μA	
Supply current	$-I_{EE}$ min.	37 mA	Apply −0.95 ± 0.005 V to all inputs.
	typ.	53 mA	
	max.	79 mA	
		T_{amb} (° C): 25	
Voltage compensation	$\frac{\Delta V_{OL}}{\Delta V_{EE}}$ max.	0.05	
	$\frac{\Delta V_{OH}}{\Delta V_{EE}}$ max.	0.025	

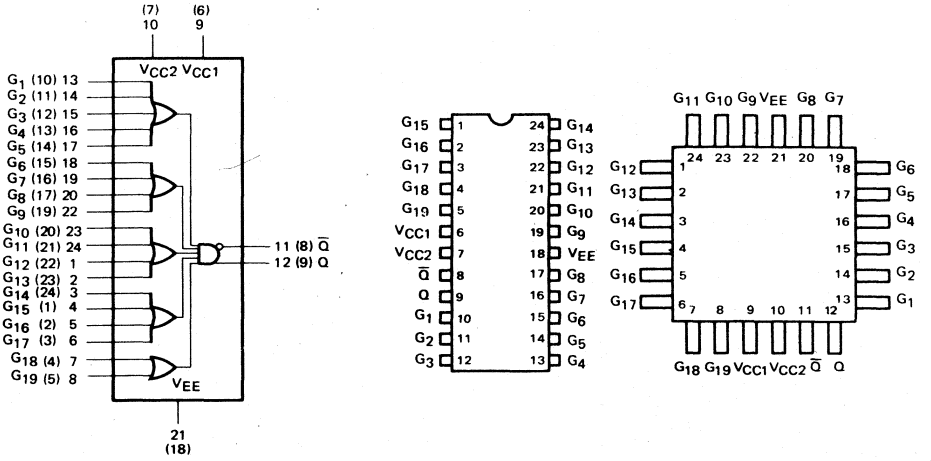
A.C. CHARACTERISTICS at V_{CC} = ground; V_{EE} = −4.5 V; load = 50 Ω to −2 V; T_{amb} = 25 °C

	Symbol	min.	typ.	max.	Conditions
Propagation delay	t_{PDQ} (ns)				Apply a reference signal to each input, one at a time, with all other inputs open.
	OR inputs	1.0		2.3	
	other inputs	0.45		0.95	
Rise time	t_{TLH} (ns)	0.45		1.1	same conditions
Fall time	t_{THL} (ns)	0.45		1.1	same conditions

These limits are for flat pack.
Add 0.2 ns to max. values for SLIM DIP package propagation delays.

2 – 4 – 4 – 4 – 5 INPUT OR – AND, OR – NAND GATE

100118 has one 2 - 4 - 4 - 4 - 5 input OR/NAND gate with direct and complement output.



Pin connections for flat pack and in ( ) for SLIM DIP packages.

QUICK REFERENCE DATA

Average propagation delay	t_P	typ.	1.15	ns
Power consumption per package	$P_{(AV)}$	typ.	200	mW

PACKAGE OUTLINE (See general section)

ORDERING INFORMATION : 100118 F (FO 44-24 lead ceramic flat pack)
100118 D (FO 72-24 lead Slim Cerdip)

TRUTH TABLE

Inputs																		Outputs	
13 (10)	15 (11)	15 (12)	16 (13)	17 (14)	18 (15)	19 (16)	20 (17)	22 (19)	23 (20)	24 (21)	1 (22)	2 (23)	3 (24)	4 (1)	5 (2)	6 (3)	7 (4)	8 (5)	11 (8)	12 (9)
L	L	L	L	L	x	x	x	x	x	x	x	x	x	x	x	x	x	x	H	L
x	x	x	x	x	L	L	L	L	x	x	x	x	x	x	x	x	x	x	H	L
x	x	x	x	x	x	x	x	x	L	L	L	L	x	x	x	x	x	x	H	L
x	x	x	x	x	x	x	x	x	x	x	x	x	L	L	L	L	x	x	H	L
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	L	L	H	L
other configurations																			L	H

Positive logic : H = HIGH state (more positive voltage) = 1
L = LOW state (less positive voltage) = 0
x = Immaterial state (H or L).

RATINGS (See family specifications)

D.C. CHARACTERISTICS at V_{CC} = ground ; V_{EE} = −4.5 V
(for test table and diagram see family specifications)

	Symbol		T_{amb} (°C) 0 to + 85		Conditions
Input current LOW	I_{IL}	min.	0.5	μA	Apply − 1.81 ± 0.005 V to each input, one at a time, with all other inputs open.
Input current HIGH	I_{IH}	max.	350	μA	Apply − 0.88 ± 0.005 V to each input, one at a time, with all other inputs open.
Supply current	$-I_{EE}$	min. typ. max.	32 45 65	mA mA mA	Apply − 0.95 ± 0.005 V to all inputs.
			25° C		
Voltage compensation	$\frac{\Delta V_{OL}}{\Delta V_{EE}}$		0.05		
	$\frac{\Delta V_{OH}}{\Delta V_{EE}}$		0.025		

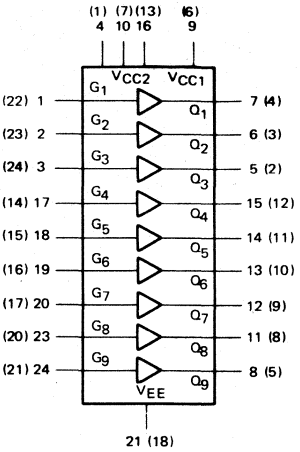
A.C. CHARACTERISTICS at V_{CC} = ground; V_{EE} = −4.5 V; load = 50 Ω to −2 V; T_{amb} = 25 °C

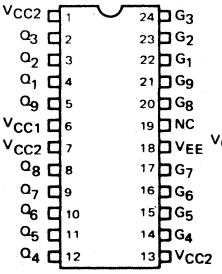
	Symbol	min.	typ.	max.	Conditions
Propagation delay	t_{PDQ} (ns) inputs 3, 4, 5, 6, 18, 19, 20, 22 (24) (1) (2) (3) (15) (16) (17) (19)	0.85		2.0	Apply a reference signal to each input, one at a time.
	other inputs	0.85		2.0	Same conditions
Rise time	t_{TLH} (ns)	0.50		1.2	Same conditions
Fall time	t_{THL} (ns)	0.50		1.2	Same conditions

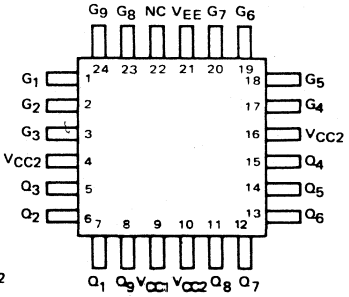
These limits ar for flat pack.
Add 0.2 ns to max. values, for SLIM DIP package propagation delays.

9 GATE BUFFER

100122 contains 9 buffer gates.







Pin connections for flat pack and in ( ) for SLIM DIP packages.

QUICK REFERENCE DATA

Average propagation delay	t_p	typ.	0.75	ns
Power consumption per package	$P_{(AV)}$	typ.	338	mW

PACKAGE OUTLINE (See general section)

ORDERING INFORMATION : 100122 F (FO 44 24-lead ceramic flat pack)
100122 D (FO 72 24-lead Slim Cerdip)

RATINGS (See family specifications)

D.C. CHARACTERISTICS at V_{CC} = ground ; V_{EE} = − 4.5 V
(for test table and diagram, see family specifications)

	Symbol		T_{amb} (°C) 0 to + 85		Conditions
Input current LOW	I_{IL}	min.	0.5	μA	Apply −1.81 ± 0.005 V to each input, one at a time, with all other inputs open.
Input current HIGH	I_{IH}	max.	350	μA	Apply −0.88 ± 0.005 V to each input, one at a time, with all other inputs open.
Supply current	$-I_{EE}$	min.	46	mA	Apply −0.95 ± 0.005 V to all inputs.
		max.	95.5	mA	
Voltage compensation			T_{amb} (°C) : 25		
	$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	max.	0.050		
	$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	max.	0.025		

A.C. CHARACTERISTICS at V_{CC} = ground; V_{EE} = −4.5 V; load = 50 Ω to −2V; T_{amb} = 25° C

	Symbol		min.	typ.	max.	Conditions
Propagation delay time	t_{PDQ}	(ns)	0.5		1.3	Apply a reference signal to each input one at a time, with all other inputs open.
Rise time	t_{TLH}	(ns)	0.5		1.6	Same conditions
Fall time	t_{THL}	(ns)	0.5		1.6	Same conditions

These limits are for flat pack.

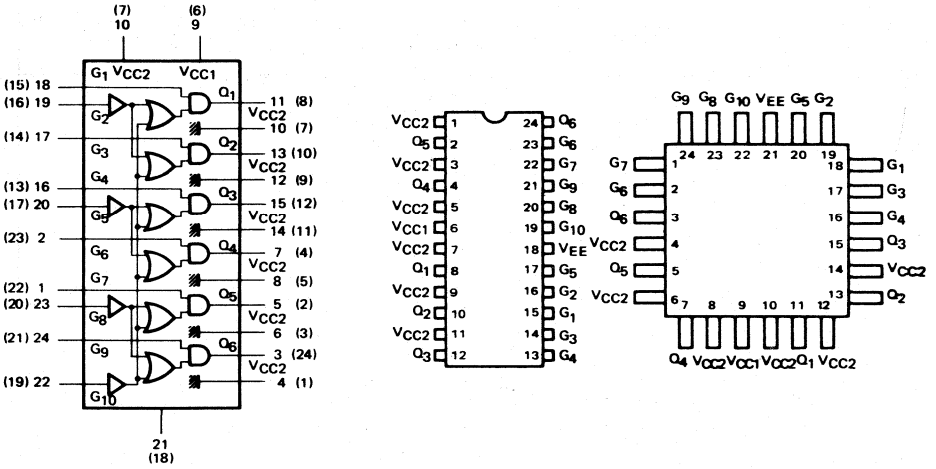
Add 0.2 ns to max. values for SLIM DIP package propagation delays.

100 123

HEX BUS DRIVER

100123 contains six bus driver capable of driving terminated lines with terminations as low as 25. Each output has its respective ground connection. The driver itself performs the positive logic AND of a data input and the OR of two enable inputs.

The output voltage low level is more negative than usual ECL outputs. This allows an emitter-follwer output transistor to turn off, when the termination supplu V_T is $-2.0\ V \pm 10\ \%$.



Pin connections for flat pack and in ( ) for SLIM DIP packages.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		$-4.5\ V$	
Output voltage low state	V_{OL}	max	$-2.2\ V$	dependent on VT
Power consumption per package	$P_{(AV)}$	typ.	730 mW	

PACKAGE OUTLINE (See general section)

ORDERING INFORMATION : 100123 F (FO 44-24 lead ceramic flat pack)
100123 D (FO 72-24 lead Slim Cerdip)

Inputs						Outputs	
22	(19)	23	(20)	24	(21)	3	(24)
22	(19)	23	(20)	1	(22)	5	(2)
22	(19)	20	(17)	2	(23)	7	(4)
22	(19)	20	(17)	16	(13)	15	(12)
22	(19)	19	(16)	17	(14)	13	(10)
22	(19)	19	(16)	18	(15)	11	(8)
x		x		L		L	
L		L		H		L	
H		x		H		H	
x		H		H		H	

Positive logic : H = HIGH state (more positive voltage) = 1
L = LOW state (less positive voltage) = 0
x = Immaterial state (H or L)

RATINGS (See family specifications)

D.C. CHARACTERISTICS at V_{CC} = ground ; V_{EE} = −4.5 V
(for test table and diagram, see family specifications)

	Symbol		T_{amb} (°C) 0 to + 85	Conditions
Input current LOW	I_{IL}	min.	0.5 μA	Apply −1.81 ± 0.005 V to each input, one at a time, with all other inputs open.
Input current HIGH	I_{IH}	max.		Apply −0.88 ± 0.005 V to each input, one at a time, with all other inputs open.
	pin 22 (19)		330 μA	
	other inputs		220 μA	
Output voltage HIGH state	V_{OH}	min.	− 1025 mV	Loaded by 25 Ω at − 2 V
	V_{OH}	max.	− 880 mV	
Output voltage LOW state	V_{OL}	max.	− 2200 mV	Loaded by 25 Ω at − 2,3 V
Supply current	$-I_{EE}$	min.	113 mA	Apply −0.95 ± 0.005 V to all inputs.
		max.	235 mA	
			T_{amb} (°C) : 25	
Voltage compensation	$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	max.	40 mV/V	Loaded by 25 Ω (between 4.2 V and 5.2 V)
	$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	max.	70 mV/V	
Low output voltage at I_{out} = 1 mA	ΔV_{OLW}	max.	− 2150 mV	

A.C. CHARACTERISTICS at V_{CC} = ground; V_{EE} = −4.5 V; load = 25 Ω to −2 V; T_{amb} = 25° C

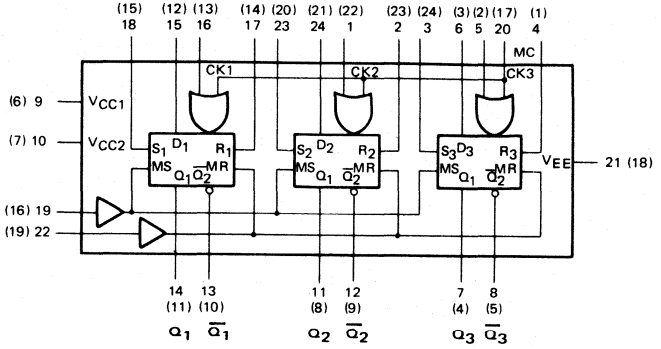
	Symbol		min.	typ.	max.	Conditions
Propagation delays : Data to output	t_{PDQ}	(ns)	1.00		4.15	Apply a reference signal to each data input, one at a time, pin 22 (19) to - 1.05 V, others open.
Dual enable to output	t_{PEQ}	(ns)	1.20		4.50	Apply a reference signal to enable input, one at a time, and data inputs to −1.05 V
Master enable to outputs	t_{PMQ}	(ns)	1.20		4.90	Apply a reference signal to enable input, one at a time, and data inputs to - 1.05 V
Rise time	t_{TLH}	(ns)	0.45		1.9	
Fall time	tTHL	(ns)	0.45		1.9	

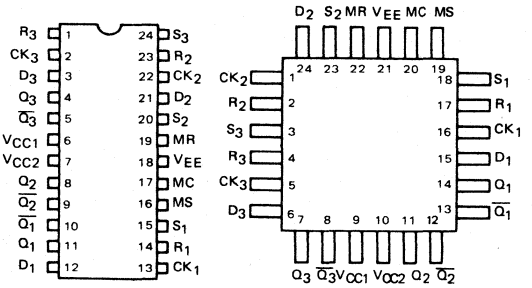
These limits are for flat pack.
Add 0.2 ns to max. values for SLIM DIP package propagation delays.

Preliminary data sheet

TRIPLE D FLIP–FLOP

100131 has three D-type master-slave flip-flops, with direct and complement output, separate clock, set and reset. In addition, all three flip-flops have a common clock, set and reset.





Pin connections for flat pack and in ( ) for SLIM DIP packages.

QUICK REFERENCE DATA

Average propagation delay	t_P	typ.	1.3	ns
Power consumption per package	$P_{(AV)}$	typ.	430	mW

PACKAGE OUTLINE (See general section)

ORDERING INFORMATION : 100131 F (FO 44-24 lead ceramic flat pack)
100131 D (FO 72-24 lead Slim Cerdip)

TRUTH TABLE

Inputs							Outputs	
15 (12)	20 (17)	16 (13)	19 (16)	18 (15)	22 (19)	17 (14)	14 (11)	13 (10)
24 (21)	20 (17)	1 (22)	19 (16)	23 (19)	22 (19)	2 (23)	11 (8)	12 (9)
6 (3)	20 (17)	5 (2)	19 (16)	3 (24)	22 (19)	4 (1)	7 (4)	8 (5)
D	MC	CK_i	MS	S	MR	R	Q_n+1	$\overline{Q}_n+1$
x	x	x	L	L	H	x	L	H
x	x	x	L	L	x	H	L	H
x	x	x	H	x	L	L	H	L
x	x	x	x	H	L	L	H	L
x	x	∫	L	L	L	L	Qn	$\overline{Q}$n
x	∫	H	L	L	L	L	Qn	$\overline{Q}$n
x	x	x	L	L	L	L	Qn	$\overline{Q}$n
H	∫	L	L	L	L	L	H	L
L	∫	L	L	L	L	L	L	H
H	L	∫	L	L	L	L	H	L
L	L	∫	L	L	L	L	L	H

D : Data Input ; MC : Master Clock ; CK_i : Clock ; MS : Master Set ; S : Set ; MR : Master Reset ; R : Reset ; Q : Direct output ; $\overline{Q}$: Complement output ; n : State before transition ; n +1 : State after transition ; ∫ : LOW to HIGH transition.

Data enters a master, when both clock and master clock are LOW, and transfers to the slave, when the clock or master clock (or both) go HIGH. If the set (or master set) is HIGH while the reset (or master reset) is HIGH, the output is undefined.

Positive logic : H = HIGH state (more positive voltage) = 1
L = LOW state (less positive voltage) = 0
x = Immaterial state (H or L).

RATINGS (See family specifications)

D.C. CHARACTERISTICS at V_{CC} = ground ; V_{EE} = − 4.5 V
(for test table and diagram, see family specifications)

	Symbol		T_{amb} (°C) 0 to + 85		Conditions
Input current LOW	I_{IL}	min.	0.5	μA	Apply −1.81 ± 0.005 V to each input, one at a time, with all other inputs open.
Input current HIGH	I_{IH}	max.			
	D		240	μA	Apply −0.88 ± 0.005 V to each input, one at a time, with all other inputs open.
	CK		240	μA	
	MC, MS, MR		450	μA	
	R, S		530	μA	
Supply current	$-I_{EE}$	min.	74	mA	Apply − 0.95 ± 0.005 V to all inputs.
		max.	149	mA	
			T_{amb} (°C) : 25		
Voltage compensation	$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	max.	0.07		
	$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	max.	0.035		

A.C. CHARACTERISTICS at V_{CC} = ground; V_{EE} = −4.5 V; load = 50 Ω to −2 V; T_{amb} = 25°C

	Symbol		min.	typ.	max.	Conditions
Propagation delay time MC to output	t_{PMCQ}	(ns)	0.75		1.65	Apply a reference signal to D inputs, and a signal to MC.
CK_i to output	t_{PCQ}	(ns)	0.7		1.5	
MS, MR to output	t_{PMQ}	(ns)	1.05		2.75	Apply a reference signal to MS or MR.
R_n, S_n to output	t_{PRQ} t_{PSQ}	(ns)	0.7		1.5	
Rise time	t_{TLH}	(ns)	0.45		1.3	
Fall time	t_{THL}	(ns)	0.45		1.3	
Max. Clock frequency	$f_{max.}$	(MHz)	400			
Data set-up time	t_{SCD}	(ns)	0.6			
Data hold time	t_{HCD}	(ns)	0.3			
Release time (R_n, S_n)	t_R		1.7	0.7		
Release time (MS, MR)	t_R		2.0	1.0		

These limits are for flat pack.
Add. 0.2 ns to max. values of propagation delays, to min. values of set-up and hold times, to typical values of release time, for SLIMDIP package.

Preliminary data sheet

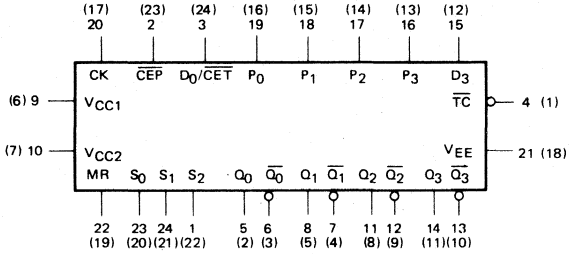
4 – BIT COUNTER – SHIFT REGISTER

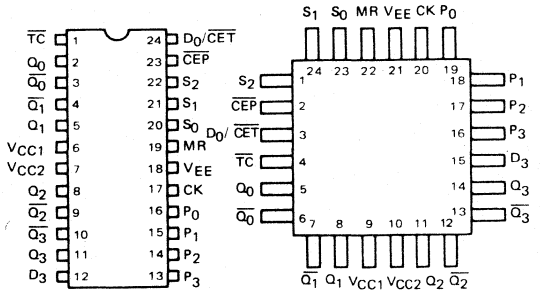
100136 operates as a 4-bit up/down counter, or as a 4-bit left/right shift register ; the operating mode is fixed by three selection inputs S_n.

These selection inputs also enable parallel loading, synchronous reset or complement of flip-flop outputs. D_O is the serial input for left shifting, D_3 for right shifting. A carry output $\overline{TC}$ goes low for 15 value in up counting mode, for 0 in down counting mode. In shifting mode, $\overline{TC}$ repeats output Q_3.

A high signal on MR enables asynchronous master reset.

Two count enables ($\overline{CEP}$, $\overline{CET}$) allow multi-stage counter cascading.





Pin connections for flat pack and in ( ) for SLIM DIP packages.

QUICK REFERENCE DATA

Average propagation delay (clock)	t_P	typ.	1.8	ns
Power consumption per package	$P_{(AV)}$	typ.	800	mW

PACKAGE OUTLINE (See family specifications)

ORDERING INFORMATION : 100136 F (FO 44-24 lead ceramic flat pack)
100136 D (FO 72-24 lead Slim Cerdip)

TRUTH TABLE

MR	S_0	S_1	S_2	$\overline{CEP}$	$D_0/\overline{CET}$	D_3	CP	Q_0	Q_1	Q_2	Q_3	TC	MODE
H	X	X	X	X	X	X	X	L	L	L	L	H	Master Reset
L	L	L	L	X	X	X	∫	P_0	P_1	P_2	P_3	L	Preset
L	L	L	H	L	L	X	∫	$(Q_0 - 3)$ minus 1				①	Count Down
L	L	L	H	H	L	X	X	Q_0	Q_1	Q_2	Q_3	①	Count Down with $\overline{CEP}$ not active
L	L	L	H	X	H	X	X	Q_0	Q_1	Q_2	Q_3	H	Count Down with $\overline{CET}$ not active
L	L	H	L	X	X	X	∫	Q_1	Q_2	Q_3	D_3	D_3	Shift Right
L	L	H	H	L	L	X	∫	$(Q_0 - 3)$ plus 1				②	Count Up
L	L	H	H	H	L	X	X	Q_0	Q_1	Q_2	Q_3	②	Count Up with $\overline{CEP}$ not active
L	L	H	H	X	H	X	X	Q_0	Q_1	Q_2	Q_3	H	Count Up with $\overline{CET}$ not active
L	H	L	L	X	X	X	∫	$\overline{Q_0}$	$\overline{Q1}$	$\overline{Q_2}$	$\overline{Q_3}$	L	Invert
L	H	L	H	X	X	X	∫	L	L	L	L	H	Clear
L	H	H	L		X	X	∫	D_0	Q_0	Q1	Q_2	Q_2	Shift Left
L	H	H	H	X	X	X	X	Q_0	Q_1	Q_2	Q_3	H	Hold

① L if $Q_0 - Q_3$ = LLLL ; ② L if $Q_0 - Q_3$ = HHHH

H if $Q_0 - Q_3 \neq$ LLLL ; H if $Q_0 - Q_3 \neq$ HHHH

SELECTION TABLE

S_0	S_1	S_2	Operating modes (synchronous)
L	L	L	Parallel load : Data available on P_n will be loaded with next clock pulse.
L	L	H	Down counter : Each clock pulse decreases the counter value.
L	H	L	Right shift : Each clock pulse shifts D_3 to Q_3, Q_n to Q_{n-1}.
L	H	H	Up counter : Each clock pulse increases the counter value.
H	L	L	Complement mode : contents of flip-flop can be synchronously inverted.
H	L	H	Reset : Enables a synchronous reset.
H	H	L	Left shift : Each clock pulse shifts Q_n to Q_{n+1}, D_0 to Q_0.
H	H	H	Hold mode : No change for Q_n.

The $\overline{C}/Q_3$ output of a 100136 can be connected to the $D_0/\overline{CET}$ input of another 100136, for multi stage counting of left shift operation.

Positive logic : H = HIGH state (more positive voltage) = 1
L = LOW state (less positive voltage) = 0

RATINGS (See family specifications)

D.C. CHARACTERISTICS at V_{CC} = ground ; $V_{EE} = -4.5$ V.
(for test table and diagram, see family specifications)

	Symbol		T_{amb} (°C) 0 to +85		Conditions
Input current LOW	I_{IL}	min.	0.5	μA	Apply -1.81 ± 0.005 V to each input, one at a time, with all other inputs open.
Input current HIGH	I_{IH}	max.			
	P_n, S_n		180	μA	
	$\overline{CEP}$		200	μA	Apply -0.88 ± 0.005 V to each input, one at a time, with all other inputs open.
	MR		240	μA	
	D_3		280	μA	
	CK		390	μA	
	$D_0/\overline{CET}$		530	μA	
Supplu current	$-I_{EE}$	min.	136	mA	Apply -0.95 ± 0.005 V to all inputs.
		typ.			
		max.	283	mA	
			T_{amb} (°C) : 25		
Voltage compensation	$\frac{\Delta V_{OI}}{\Delta V_{EE}}$	max.	0.070		
	$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	max.	0.035		

A.C. CHARACTERISTICS at V_{CC} = ground; V_{EE} = - 4.5 V; load = 50 Ω to - 2 V; T_{amb} = 25°C.

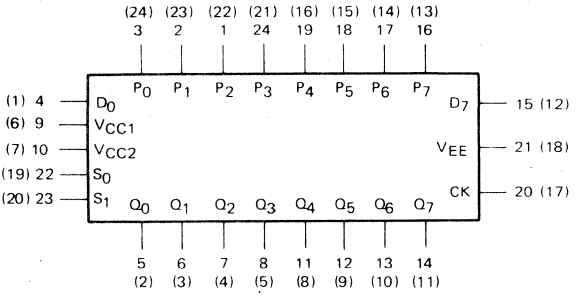
	Symbol		min.	typ.	max.	Conditions
Propagation delay time						
CK to Q_n, $\overline{Q_n}$	t_{PCQ}	(ns)	1.15		2.3	Apply a reference signal on P_n.
CK to $\overline{TC}$	t_{PCC}	(ns)	1.9		3.8	
MR to Q_n, $\overline{Q_n}$	t_{PMQ}	(ns)	1.6		2.8	Apply a reference signal to MR.
MR to $\overline{TC}$	t_{PMC}	(ns)	2.2		5.6	
D_0/$\overline{CET}$ to $\overline{TC}$	t_{PDC}	(ns)	1.6		2.85	
S_n to $\overline{TC}$	t_{PSC}	(ns)	1.6		4.8	
Rise time	t_{TLH}	(ns)	0.5		1.75	
Fall time	t_{THL}	(ns)	0.5		1.75	
Set-up time						
D_3	t_S	(ns)		0.7		
D_0				0.7		
D_n				0.95		
$\overline{CET}$, $\overline{CEP}$				0.9		
S_n				1.5		
Hold time						
D_3	t_H	(ns)		− 0.7		
D_0				− 0.7		
D_n				− 1.05		
$\overline{CET}$, $\overline{CEP}$				− 0.75		
S_n				− 1.5		
Release time	t_R	(ns)		1		
Max. Clock frequency	fmax.	(MHz)		300		

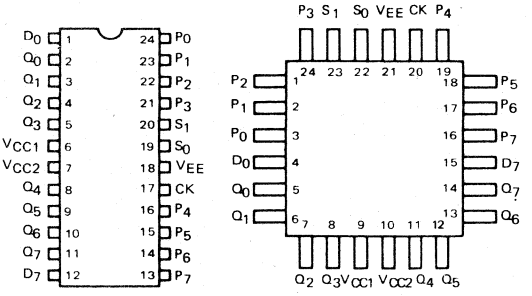
These limits are for flat pack.
Add. 0.2 ns to max. values of propagation delays, to min. values of set-up and hold times, to typical values of release time, for SLIMDIP package.

Preliminary data sheet

8 – BIT SHIFT REGISTER

100141 has eight D-type flip-flops, and two selection inputs S_0 , S_1 allowing a parallel loading or left shifting, or right shifting, or hold operation mode.





Pin connections for flat pack and in ( ) for SLIM DIP packages.

QUICK REFERENCE DATA

Average propagation delay (clock)	t_p	typ.	1.7	ns
Power consumption per package	$P_{(AV)}$	typ.	850	mW

PACKAGE OUTLINE (See general section)

ORDERING INFORMATION : 100141 F (FO 44-24 lead ceramic flat pack)
100141 D (FO 72-24 lead Slim Cerdip)

TRUTH TABLE

Mode	Inputs			Outputs							
	S_0	S_1	CK	7 Q_{n+1}	6 Q_{n+1}	5 Q_{n+1}	4 Q_{n+1}	3 Q_{n+1}	2 Q_{n+1}	1 Q_{n+1}	0 Q_{n+1}
Register load	L	L	⎍	7 P_n	6 P_n	5 P_n	4 P_n	3 P_n	2 P_n	1 P_n	0 P_n
Right shift	L	H	⎍	7 D_n	7 Q_n	6 Q_n	5 Q_n	4 Q_n	3 Q_n	2 Q_n	1 Q_n
Left shift	H	L	⎍	6 Q_n	5 Q_n	4 Q_n	3 Q_n	2 Q_n	1 Q_n	0 Q_n	0 D_n
Hold state	H	H	x	7 Q_n	6 Q_n	5 Q_n	4 Q_n	3 Q_n	2 Q_n	1 Qn	0 Q_n

POSITIVE LOGIC : H = HIGH state (more positive voltage) = 1
L = LOW state (less positive voltage) = 0
⎍ = LOW to HIGH transition
x = Immaterial state (H or L) or transition

n last state n + 1 next state after transition

RATINGS (See family specifications)

D.C. CHARACTERISTICS at V_{CC} = ground ; V_{EE} = − 4.5 V
(for test table and diagram, see family specifications)

	Symbol	T_{amb} (°C) 0 to + 85	Conditions
Input current LOW	I_{IL} min.	0.5 μA	Apply − 1.81 ± 0.005 V to each input, one at a time, with all other inputs open.
Input current HIGH	I_{IH} max.		Apply −0.88 ± 0.005 V to each input , one at a time, with all other inputs open.
	CK	640 μA	
	other inputs	220 μA	
Supply current	$-I_{EE}$ min.	120 mA	Apply −0.95 ± 0.005 V to all inputs
	max.	238 mA	
		T_{amb} (°C):25	
Voltage compensation	$\frac{\Delta V_{OL}}{\Delta V_{EE}}$ max.	0.05	
	$\frac{\Delta V_{OH}}{\Delta V_{EE}}$ max.	0.025	

A.C. CHARACTERISTICS at V_{CC} = ground; V_{EE} = − 4.5 V; load = 50 Ω to − 2 V; T_{amb} = 25°C.

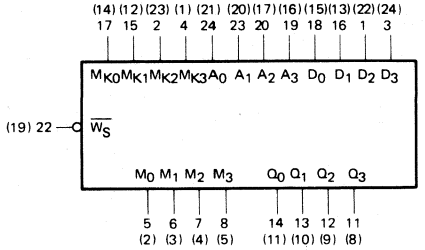
	Symbol	min.	typ.	max.	Conditions
Propagation delay time CK to outputs	t_{PCQ} (ns)	1.1		2.2	Apply a reference signal to Pn, Dn, and a signal to CK
Max. shift frequency	f_{max} (MHz)	380			
Rise time	t_{TLH} (ns)	0.55		1.65	
Fall time	t_{THL} (ns)	0.55		1.65	
Set up time					
Data (P_n, O_n)	t_{SCD} (ns)	1.0			
Select (S_n)	t_{SCS} (ns)	2.7			
Hold time					
Data (P_n, O_n)	t_{HCD} (ns)	0			
Select (S_n)	t_{HCS} (ns)	− 0.9			

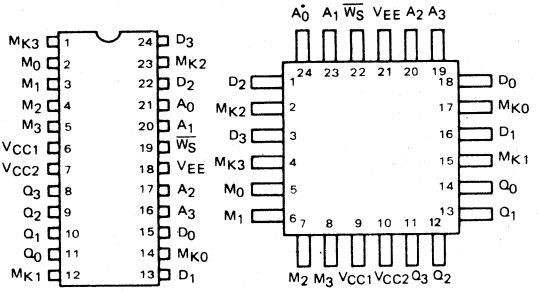
These limits are for flat pack.
Add. 0.2 ns to max. values of propagation delays, to min. values of set-up and hold times, to typical values of release time, for SLIMDIP package.

Preliminary data sheet

4 x 4 CONTENT ADRESSABLE MEMORY

100142 is a 4 word x 4 bit content addressable memory (CAM). Each word lication is selected by one address line. The mask input of a data input blocks data storage. When the mask is high, the data input word is simultaneously compared with each of the four memory words. If a search compare results in a match, this output will go low. A high mask input on any bit forces a match of that bit.





Pin connections for flat pack and in ( ) for SLIM DIP packages.

QUICK REFERENCE DATA

Average propagation delay	t_p	typ.		
Power consumption per package	$P_{(AV)}$	typ.	687	mW

PACKAGE OUTLINE (See general section)

ORDERING INFORMATION : 100142 F (FO 44-24 lead ceramic flat pack)
100142 D (FO 72-24 lead Slim Cerdip)

TRUTH TABLE

Operations	Inputs				Flip-flop	Outputs	
	$\overline{WS}$	A_i	D_j	M_{kj}	Q_{ij}	M_j	Q_j
Write disabled	X	H	X	X	NC	X	L
	X	L	X	H	NC	L	Q_{ijn-1}
	H	L	X	X	NC	L	Q_{ijn-1}
Write	L	L	H	L	H	L	H
	L	L	L	L	L	L	L
Read	H	L	X	X	H	X	H
	H	L	X	X	L	X	L
Match masked	H	X	X	H	NC	L	X
Match not satisfied	H	L	H	L	L	H	L
	H	H	H	L	L	H	L
	H	H	L	L	H	H	L
	H	L	L	L	H	H	H
Match satisfied	H	L	H	L	H	L	H
	H	H	H	L	H	L	L
	H	H	L	L	L	L	L
	H	L	L	L	L	L	L

Positive logic : H = HIGH state
L = LOW state
X = Immaterial state

i : for ith word
j : for jth bit
NC : No change from previous state
Q_{n-1} : Previous cell state

RATINGS (See family specifications)

D.C. CHARACTERISTICS at V_{CC} = ground ; V_{EE} = − 4.5 V
(for test table and diagram, see family specifications)

	Symbol	T_{amb} (°C) 0 to + 85	Conditions
Input current LOW	I_{IL} min.	0.5 μA	Apply − 1.81 ± 0.005 V to each input, one at a time, with all other inputs open.
Input current HIGH	I_{IH} max.	265 μA	Apply − 0.88 ± 0.005 V to each input , one at a time, with all other inputs open.
Supply current	$-I_{EE}$ min. max.	114 mA 288 mA	Apply − 0.95 ± 0.005 V to all inputs
Voltage compensation		T_{amb} (°C):25	
	$\frac{\Delta V_{OH}}{\Delta V_{EE}}$ max.	0.025	
	$\frac{\Delta V_{OL}}{\Delta V_{EE}}$ max.	0.050	

A.C. CHARACTERISTICS at V_{CC} = ground; V_{EE} = − 4.5 V; load = 50 Ω to − 2 V; T_{amb} = 25°C.

	Symbol	min.	typ.	max.	Conditions
Rise time	t_{TLH} (ns)	0.5		2	
Fall time	t_{THL} (ns)	0.5		2	
Propagation delays					
- Data in to new data out	t_{PDD} (ns)	2.6		5.7	
- Data in to match out	t_{PDM} (ns)		3.3		
- Address to data out	t_{PAD} (ns)		2.7		
- Mask in to enable partial match out	t_{PMM} (ns)		2.2		
- Write to new data out	t_{PWD} (ns)	3.2		6.5	
Set-up time					
- Data to write	t_{SWD} (ns)	−1			
- Address to write	t_{SWA} (ns)	1			
- Mask in to inhibit write	t_{SWM} (ns)		−1.1		
Hold time					
- Address to write	t_{HWA} (ns)	0			
- Mask in to inhibit write	t_{HWM} (ns)	1			
- Data to write	t_{HWD} (ns)	1			
- Write pulse width	t_W (ns)	3			

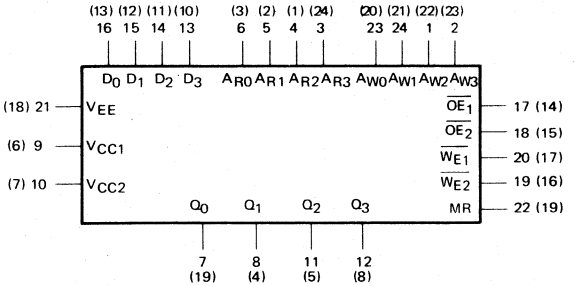
These limits are for flat pack.
Add. 0.2 ns to max. values of propagation delays, to min. values of set-up and hold times, to typical values of release time, for SLIMDIP package.

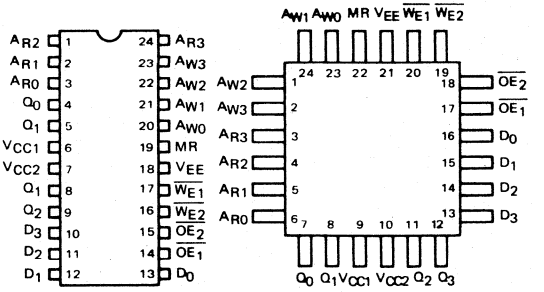
100 145

Preliminary data sheet

16 x 4 READ WHILE WRITE REGISTER FILE

100145 is a 64 bit register file organized as an array of 16 x 4. Separate address inputs for read (AR_n) and write (AW_n) are intended for shorter overall cycle time by allowing one address to be setting up, while the other is being executed. Four output latches, which store data from previous operation while writing is in progress, also increase operating speed. The write enable input ($\overline{WE}$) selects the read or write mode. In the read mode, the outputs can be foreced low by a high signal on either of the output enable ($\overline{OE}$). One $\overline{WE}$ input and one $\overline{OE}$ input can be tied together, to serve as a chip select ($\overline{CS}$). When $\overline{CS}$ input is high (with low other $\overline{OE}$), the circuit is in the read mode and the data are latched in the output latches, and become available as soon as $\overline{CS}$ goes low. The master reset signal (MR) clears all cells, forces the outputs low and resets the output katches.





Pin connections for flat pack and in ( ) for SLIM DIP packages.

QUICK REFERENCE DATA

Average propagation delay	t_p	typ.		
Power consumption per package	$P_{(AV)}$	typ.	900	mW

PACKAGE OUTLINE (See general section)

ORDERING INFORMATION : 100145 F (FO 44-24 lead ceramic flat pack)
100145 D (FO 72-24 lead Slim Cerdip)

FUNCTION TABLE

Inputs						Outputs			
Data 16-15-14-13	$\overline{WE_1}$ 20	$\overline{WE_2}$ 19	$\overline{OE_1}$ 17	$\overline{OE_2}$ 18	MR 22	Mode	Output latches	Q 7 8 11 12	
	L	L	L	L	L	Write	hold	Data from latches	(previous) (operation)
	H	X	L	L	L	Read	Data are latched	Read data	
	H	X	X	H	L	"	"	L	
	H	X	H	X	L	"	"	L	
	X	H	L	L	L	"	"	Read data	
	X	H	X	H	L	"	"	L	
	X	H	H	X	L	"	"	L	
	X	X	X	X	H		Reset	L	(clears) (all cells)

Positive logic : H = HIGH state
L = LOW state
X = Immaterial

RATINGS (See family specifications)

D.C. CHARACTERISTICS at V_{CC} = ground ; V_{EE} = − 4.5 V
(for test table and diagram, see family specifications)

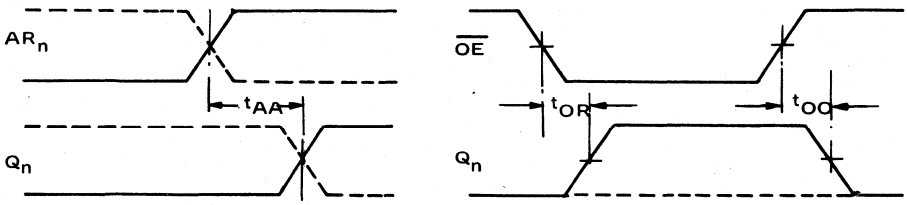
	Symbol	T_{amb} (°C) 0 to + 85	Conditions
Input current LOW	I_{IL} min.	0.5 μA	Apply − 1.81 ± 0.005 V to each input, one at a time, with all other inputs open.
Input current HIGH	I_{IH} max.	270 μA	Apply − 0.88 ± 0.005 V to each input, one at a time, with all other inputs open.
	WE inputs	270 μA	
	other inputs	220 μA	
Supply current	$-I_{EE}$ min.	119 mA	Apply − 0.95 ± 0.005 V to all inputs.
	max.	247 mA	
		T_{amb} (°C) : 25	
Voltage compensation	$\frac{\Delta V_{OH}}{\Delta V_{EE}}$ max.	0.025	
	$\frac{\Delta V_{OL}}{\Delta V_{EE}}$ max.	0.050	

A.C. CHARACTERISTICS at V_{CC} = ground; V_{EE} = − 4.5 V; load = 50 Ω to − 2 V; T_{amb} = 25°C.

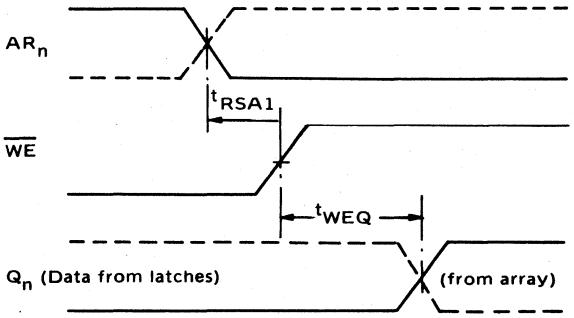
	Symbol		min.	typ.	max.	Conditions
Acess/Recovery timing						
Address access	t_{AA}	(ns)	2		7.2	
Output recovery	t_{OR}	(ns)	1		2.9	
Output disable	t_{OD}	(ns)	1		2.9	
Read timing						
Address set-up	t_{RSA1}	(ns)	3			
Output delay	t_{WEQ}	(ns)	2		5.9	
Output latch timing						
Address set-up	t_{RSA2}	(ns)	8.3			
Address hold	t_{RHA}		0			
Write timing						
Address set-up	t_{WSA}	(ns)	3			
Address hold	t_{WHA}	(ns)	0			
Data set-up	t_{WSD}	(ns)	5.5			
Data hold	t_{WHD}	(ns)	0			
Write pulse width	t_{W}	(ns)	5			
$\overline{WE}$ to $\overline{WE}$ set-up	t_{SW}	(ns)	0.5			
$\overline{WE}$ to $\overline{WE}$ hold	t_{HW}	(ns)	0			
Master reset timing						
Reset pulse width	t_{M}	(ns)	13.5			
$\overline{WE}$ hold to write	t_{MHW}	(ns)	18.2			
Output disable	t_{MQ}	(ns)			3.5	

These limits are for flat pack.
Add. 0.2 ns to max. values of propagation delays, to min. values of set-up and hold times, to typical values of release time, for SLIMDIP package.

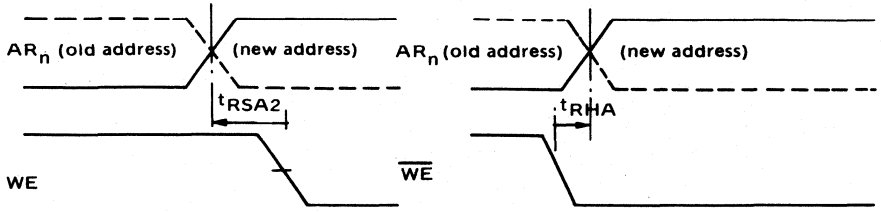
Access/Recovery times
($\overline{WE}_1$ or $\overline{WE}_2$ = H, $\overline{OE}_1$ = $\overline{OE}_2$ = L)



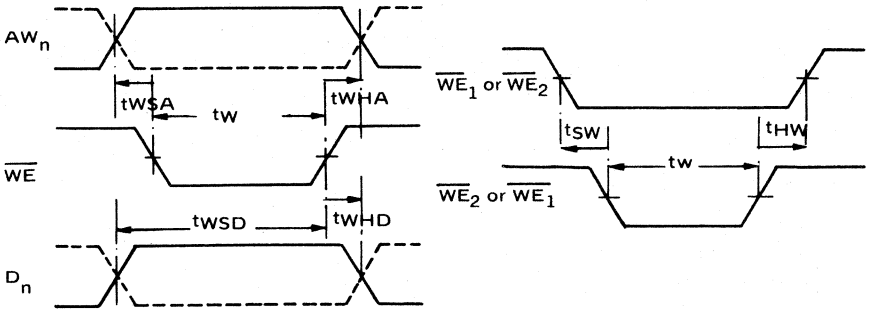
Read timing



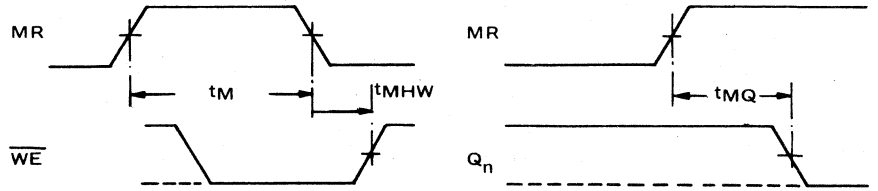
Output latch timing



Write timing

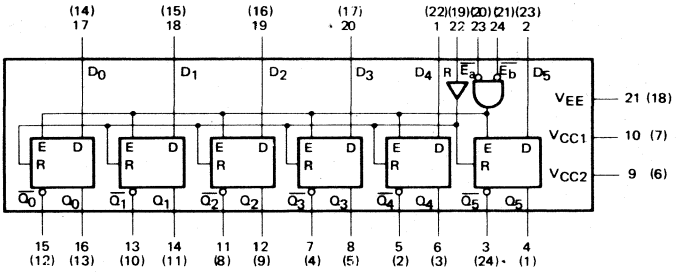


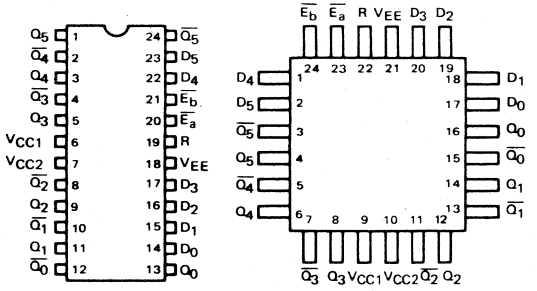
Master reset timing



HEX D LATCH FLIP-FLOP

100150 is composed of six latches with data inputs, complement and data outputs. All latches have a common reset and enable. The enable is driven by a 2 input negative AND gates.





Pin connections for flat pack and in ( ) for SLIM DIP packages.

QUICK REFERENCE DATA

Average propagation delay (Data)	t_P	typ.	0.9	ns
Power consumption per package	$P_{(AV)}$	typ.	450	mW

PACKAGE OUTLINE (See general section)

ORDERING INFORMATION : 100150 F (FO 44-24 lead ceramic flat pack)
100150 D (FO 72-24 lead SLIM CERDIP)

TRUTH TABLE

D	$\overline{E_a}$	$\overline{E_b}$	R	$\overline{Q}$	Q
17	23	24	22	15	16
18	23	24	22	13	14
19	23	24	22	11	12
20	23	24	22	7	8
1	23	24	22	5	6
2	23	24	22	4	3
H	L	L	L	L	H
L	L	L	L	H	L
X	X	H	L	No change	
X	H	X	L	No change	
X	X	X	H	H	L

Positive logic : H = HIGH state
L = LOW state
X = Immaterial state

RATINGS (See family specifications)

D.C. CHARACTERISTICS at V_{CC} = ground ; V_{EE} = − 4.5 V
(for test table and diagram, see family specifications)

	Symbol	T_{amb} (°C) 0 to + 85	Conditions
Input current LOW	I_{IL} min.	0.5 μA	Apply −1.81 ± 0.005 V to each input, one at a time, with all other inputs open.
Input current HIGH	I_{IH} max.		Apply −0.88 ± 0.005 V to each inputs, one at a time, with all other inputs open.
	Pin 22	450 μA	
	Pins 23-24	520 μA	
	Pins 1-2-17-18 19-20	340 μA	
Supply current	$-I_{EE}$ min.	79 mA	Apply −0.95 ± 0.005 V to all inputs
	max.	159 mA	
		T_{amb} (°C):25	
Voltage compensation	$\frac{\Delta V_{OH}}{\Delta V_{EE}}$ max.	0.035	
	$\frac{\Delta V_{OL}}{\Delta V_{EE}}$ max.	0.070	

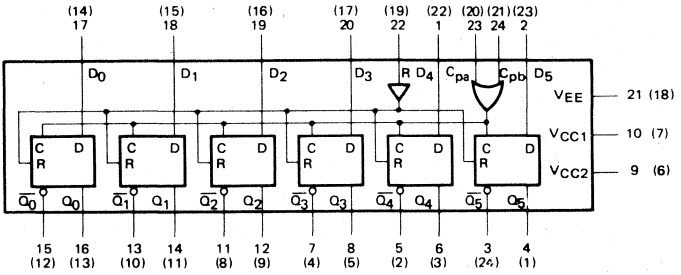
A.C. CHARACTERISTICS at V_{CC} = ground; V_{EE} = − 4.5 V; load = 50 Ω to − 2 V; T_{amb} = 25°C.

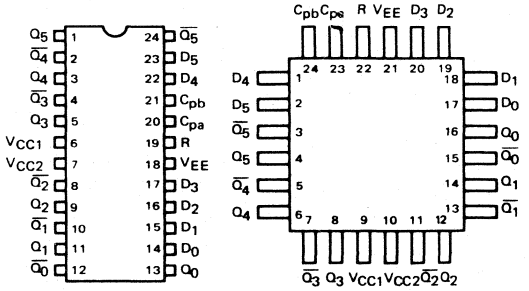
	Symbol	min.	typ.	max.	Conditions
Rise time	t_{TLH} (ns)	0.55		1.5	
Fall time	t_{THL} (ns)	0.55		1.5	
Data propagation delay time	t_{PDQ} (ns)	0.6		1.2	
Enable propagation delay time	t_{PEQ} (ns)	0.75		1.7	
Reset propagation delay time	t_{PRQ} (ns)	1.15		2.5	
Delay set-up time	t_{SED} (ns)	1			
Data hold time	t_{HED} (ns)	0.5			
Release time	t_R (ns)	2.0	1.2		

These limits are for flat pack.
Add. 0.2 ns to max. values of propagation delays, to min. values of set-up and hold times, to typical values of release time, for SLIMDIP package.

HEX D MASTER-SLAVE FLIP-FLOP

100151 contains six flip-flops with complement and data outputs, a common reset (MR) and a pair of common clock inputs. Data enter the flip-flop on the low to high transition of one of the two clock inputs.





Pin connections for flat pack and in ( ) for SLIM DIP packages.

QUICK REFERENCE DATA

Average propagation delay	t_P	typ.		
Power consumption per package	$P_{(AV)}$	typ.	630	mW

PACKAGE OUTLINE (See general section)

ORDERING INFORMATION : 100151 F (FO 44-24 lead ceramic flat pack)
100151 D (FO 72-24 lead SLIM CERDIP)

FUNCTION TABLE

Inputs				Outputs	
D	CP_a	CP_b	R	$\overline{Q}$	Q
17	23	24	22	15	16
18	23	24	22	13	14
19	23	24	22	11	12
20	23	24	22	7	8
1	23	24	22	5	6
2	23	24	22	4	3
H	L	⎍	L	L	H
L	L	⎍	L	H	L
H	⎍	L	L	L	H
L	⎍	L	L	H	L
X	X	H	L	No change	
X	H	X	L	No change	
X	X	X	H	H	L
X	L	L	L	No change	

Positive logic : H = HIGH state
L = LOW state
X = State is immaterial (may be high, low or switching)
⎍ = LOW to HIGH transition.

RATINGS (See family specifications)

D.C. CHARACTERISTICS at V_{CC} = ground ; V_{EE} = − 4.5 V
(for test table and diagram, see family specifications)

	Symbol	T_{amb} (°C) 0 to + 85	Conditions
Input current LOW	I_{IL} min.	0.5 μA	Apply − 1.81 ± 0.005 V to each input, one at a time, with all other inputs open.
Input current HIGH	I_{IH} max.		Apply − 0.88 ± 0.005 V to each input , one at a time, with all other inputs open.
	Pins 1-2-17-18 19-20	225 μA	
	Pins 23-24	520 μA	
	Pin 22	450 μA	
Supply current	$-I_{EE}$ min.	98 mA	Apply −0.95 ± 0.005 V to all inputs
	max.	198 mA	
		T_{amb} (°C):25	
Voltage compensation	$\frac{\Delta V_{OH}}{\Delta V_{EE}}$ max.	0.035	
	$\frac{\Delta V_{OL}}{\Delta V_{EE}}$ max.	0.070	

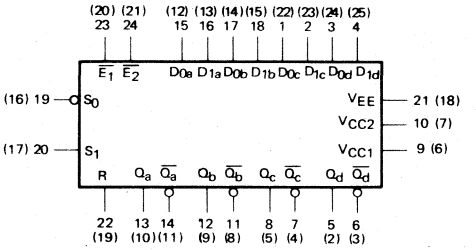
A.C. CHARACTERISTICS at V_{CC} = ground; V_{EE} = − 4.5 V; load = 50 Ω to − 2 V; T_{amb} = 25°C.

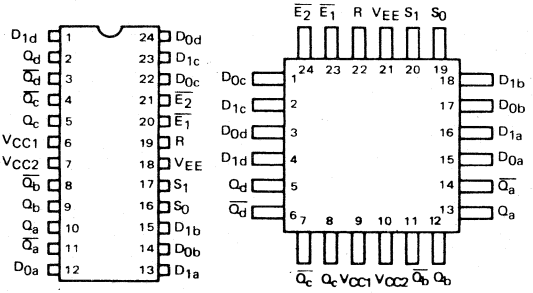
	Symbol	min.	typ.	max.	Conditions
Rise time	t_{TLH} (ns)	0.55		1.5	
Fall time	t_{THL} (ns)	0.55		1.5	
Clock propagation delay time	t_{PCQ} (ns)	0.95		2.10	
Reset propagation delay time	t_{PRQ} (ns)	1.35		3	
Set-up time data to clock	t_{PCD} (ns)	0.6			
Hold time data to clock	t_{HCD} (ns)	0.3			
Release time	t_R (ns)	1.7	0.7		
Toggle frequency	f_{max} (MHz)	400			

These limits are for flat pack.
Add. 0.2 ns to max. values of propagation delays, to min. values of set-up and hold times, to typical values of release time, for SLIMDIP package.

QUADRUPLE 2 – WAY MULTIPLEXER-LATCH

100155 has four flip-flops with complement and data outputs, a common reset and a common clock, fed by a 2-input negative AND gate, data inputs from a 2-way multiplexer. Each multiplexer has two data inputs selected by two common address inputs (S_0, S_1). One address input is complemented, so the address inputs can be bied together, to form a single select input.





Pin connections for flat pack and in ( ) for SLIM DIP packages.

QUICK REFERENCE DATA

Average propagation delay (Data)	t_p	typ.	1	ns
Power consumption per package	$P_{(AV)}$	typ.	450	mW

PACKAGE OUTLINE (See general section)

ORDERING INFORMATION : 100155 F (FO 44-24 lead ceramic flat pack)
100155 D (FO 72-24 lead Slim Cerdip)

TRUTH TABLE

Inputs							Outputs	
							$\overline{Q}$	Q
Reset	Enable		Address		Data			
22	23	24	20	19	16	15	14	13
					18	17	11	12
					2	1	7	8
					4	3	6	5
H	x	x	x	x	x	x	H	L
L	L	L	H	H	H	x	L	H
L	L	L	H	H	L	x	H	L
L	L	L	L	L	x	H	L	H
L	L	L	L	L	x	L	H	L
L	L	L	L	H	x	x	H	L
L	L	L	H	L	H	x	L	H
L	L	L	H	L	x	H	L	H
L	L	L	H	L	L	L	H	L
L	H	x	x	x	x	x	No change	
L	x	H	x	x	x	x	No change	

Positive logic : H = HIGH state
L = LOW state
x = Immaterial state

RATINGS (See family specifications)

D.C. CHARACTERISTICS at V_{CC} = ground ; V_{EE} = − 4.5 V
(for test table and diagram, see family specifications)

	Symbol	T_{amb} (°C) 0 to + 85	Conditions
Input current LOW	I_{IL} min.	0.5 μA	Apply −1.81 ± 0.005 V to each input, one at a time, with all other inputs open.
Input current HIGH	I_{IH} max.		Apply − 0.88 ± 0.005 V to each input, one at a time, with all other inputs open.
	Pins 2-4-6-18 1-3-15-17	340 μA	
	Pins 19-20	220 μA	
	Pins 23-24	350 μA	
	Pin 22	430 μA	
Supply current	$-I_{EE}$ min.	66 mA	Apply −0.95 ± 0.005 V to all inputs
	typ.	105 mA	
	max.	133 mA	
		T_{amb} (°C):25	
Voltage compensation	$\frac{\Delta V_{OH}}{\Delta V_{EE}}$ max.	0.035	
	$\frac{\Delta V_{OL}}{\Delta V_{EE}}$ max.	0.070	

A.C. CHARACTERISTICS at V_{CC} = ground; V_{EE} = − 4.5 V; load = 50 Ω to − 2 V; T_{amb} = 25°C.

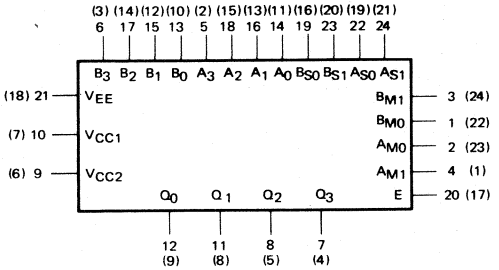
	Symbol	min.	typ.	max.	Conditions
Rise time	t_{TLH} (ns)	0.7		1.65	
Fall time	t_{THL} (ns)	0.7		1.65	
Propagation delays					
Data to output	t_{PDQ} (ns)	0.7		1.55	
Address to output					
Pins 19, 20	t_{PAQ} (ns)	1.5		3.25	
Enable to output	t_{PEQ} (ns)	1		2.2	
Reset to output	t_{PRQ} (ns)	1		2.7	
Set-up time					
Data to enable	t_{SED} (ns)	0.6			
Address to enable	t_{SEA} (ns)	2.3			
Hold time					
Data to enable	t_{HED} (ns)	0.3			
Address to enable	t_{HEA} (ns)	− 0.5			
Release time	t_R (ns)	2.0	1.2		

These limits are for flat pack.
Add. 0.2 ns to max. values of propagation delays, to min. values of set-up and hold times, to typical values of release time, for SLIMDIP package.

Preliminary data sheet

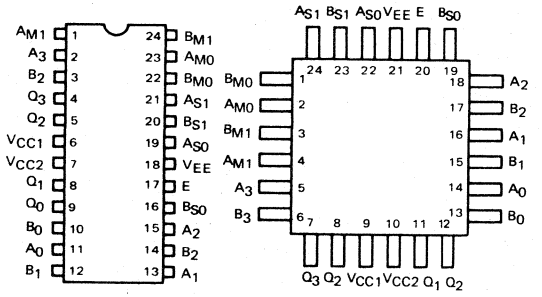
MASK – MERGE SELECTOR

100156 merges 4-bit words to form a 4 bit output word. The merge of A_n into B_n, or B_n into A_n by one, two, three (per the A_{sj} or B_{sj} value) from the left, is allowed by the AM_j or BM_j enable. The B_n merge overrides the A_n merge, when both are enabled (A_n merges into B_n, then B_n into A_n). A B_n address (BS_j) greater than or equal to the A_n address forces the outputs to all B_n. The merge outputs feed 4 latches with a common enable.



Pin names

E	Latch enable inputs
Q_n	Data outputs
A_n	Data inputs
B_n	Data inputs
BM_j	B merge enable inputs
AM_j	A merge enable inputs
AS_j	A_n adress input
BS_j	B_n adress input



Pin connections for flat pack and in ( ) for SLIM DIP packages.

QUICK REFERENCE DATA

Average propagation delay (Data)	t_p	typ.	1.2	ns
Power consumption per package	$P_{(AV)}$	typ.	689	mW

PACKAGE OUTLINE (See general section)

ORDERING INFORMATION : 100156 F (FO 44-24 lead ceramic flat pack)
100156 D (FO 72-24 lead Slim Cerdip)

TRUTH TABLE

Inputs									Outputs				
3 BM_1	1 BM_0	4 AM_1	2 AM_0	23 BS_1	19 BS_0	24 AS_1	22 AS_0	20 E	12 Q_0	11 Q_1	8 Q_2	7 Q_3	
X	X	H	X	X	X	X	X	L	B_0	B_1	B_2	B_3	Pass B_n
H	X	X	X	X	X	X	X	L	B_0	B_1	B_2	B_3	Pass B_n
L	L	L	L	X	X	X	X	L	A_0	A_1	A_2	A_3	Pass A_n
L	L	L	H	X	X	L	L	L	B_0	B_1	B_2	B_3	
L	L	L	H	X	X	L	H	L	A_0	B_1	B_2	B_3	Merge of
L	L	L	H	X	X	H	L	L	A_0	A_1	B_2	B_3	A_n into B_n
L	L	L	H	X	X	H	H	L	A_0	A_1	A_2	B_3	
L	H	L	L	L	L	X	X	L	A_0	A_1	A_2	A_3	
L	H	L	L	L	H	X	X	L	B_0	A_1	A_2	A_3	merge of
L	H	L	L	H	L	X	X	L	B_0	B_1	A_2	A_3	B_n into A_n
L	H	L	L	H	H	X	X	L	B_0	B_1	B_2	A_3	
L	H	L	H	L	L	L	H	L	A_0	B_1	B_2	B_3	the B_n merge
L	H	L	H	L	L	H	L	L	A_0	A_1	B_2	B_3	overrides
L	H	L	H	L	L	H	H	L	A_0	A_1	A_2	B_3	the A_n merge
L	H	L	H	L	H	H	L	L	B_0	A_1	A_2	B_3	
L	H	L	H	L	H	H	H	L	B_0	A_1	A_2	B_3	
L	H	L	H	H	L	H	H	L	B_0	B_1	A_2	A_3	
L	H	L	H	H	H	H	H	L	B_0	B_1	B_2	B_3	
L	H	L	H	H	H	H	L	L	B_0	B_1	B_2	B_3	Address BS
L	H	L	H	H	H	L	H	L	B_0	B_1	B_2	B_3	$\geqslant$ address
L	H	L	H	H	H	L	L	L	B_0	B_1	B_2	B_3	AS forces the
L	H	L	H	H	L	H	L	L	B_0	B_1	B_2	B_3	outputs to
L	H	L	H	H	L	L	H	L	B_0	B_1	B_2	B_3	all B_n
L	H	L	H	H	L	L	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	L	H	L	H	L	B_0	B_1	B_2	B_3	
L	H	L	H	L	H	L	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	L	L	L	L	L	B_0	B_1	B_2	B_3	
X	X	X	X	X	X	X	X	H	Q_0	Q_1	Q_2	Q_3	

Positive logic : H = HIGH state
L = LOW state
X = Immaterial state

RATINGS (See family specifications)

D.C. CHARACTERISTICS at V_{CC} = ground ; V_{EE} = − 4.5 V
(for test table and diagram, see family specifications).

	Symbol	T_{amb} (° C) 0 to+ 85	Conditions
Input current LOW	I_{IL} min.	0.5 μA	Apply − 1.81 ± 0.005 V to each input, one at a time, with all other inputs open.
Input current HIGH	I_{IH} max.		
	Pin 20	250 μA	Apply −0.88 ± 0.005 V to each input, one at a time, with all other inputs open.
	Pins 19-22-23-24	230 μA	
	Pins 1-2-3-4	265 μA	
	Pins 13-18-5-6	340 μA	
Supply current	$-I_{EE}$ min.	80 mA	Apply −0.95 ± 0.005 V to all inputs
	max.	200 mA	
		T_{amb} (° C) :25	
Voltage compensation	$\frac{\Delta V_{OH}}{\Delta V_{EE}}$ max.	0.035	
	$\frac{\Delta V_{OL}}{\Delta V_{EE}}$ max.	0.070	

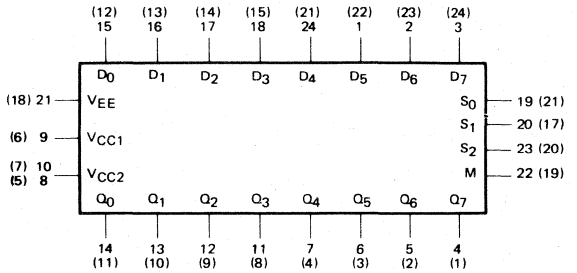
A.C. CHARACTERISTICS at V_{CC} = ground; V_{EE} = − 4.5 V; load= 50 Ω to − 2 V; T_{amb} = 25°C.

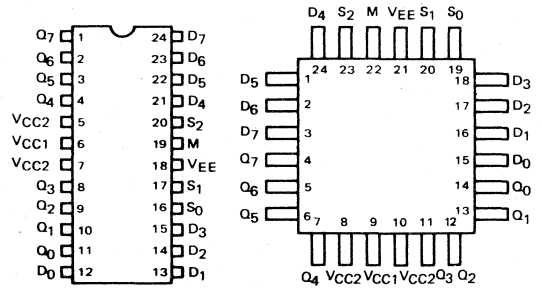
	Symbol		min.	typ.	Max.	Conditions
Rise time	t_{TLH}	(ns)	0.5		2.5	
Fall time	t_{THL}	(ns)	0.5		2.5	
Propagation delay						
Merge enable (AM_j, BM_j) to output	t_{PMQ}	(ns)	1.6		4.1	
Address to output	t_{PAQ}	(ns)	1.6		3.7	
Data to output	t_{PDQ}	(ns)	0.7		1.85	
Enable (E) to output	t_{PEQ}	(ns)	1.1		2.65	
Set-up time						
Data to enable (E)	t_{SED}	(ns)	0			
Marge enable (AM_j, BM_j) to enable (E)	t_{SEM}	(ns)	2.3			
Address to enable (E)	t_{SEA}	(ns)	2.3			
Hold time						
Data to enable (E)	t_{HED}	(ns)	2			
Merge enable (AM_j, BM_j) to enable (E)	t_{HEM}	(ns)	0.2			
Address to enable (E)	t_{HEA}	(ns)	0.3			

These limits are for flat pack.
Add 0.2 ns to max. values of propagation delays and to values of set-up, hold times, for SLIM DIP package.

8 BIT SHIFT MATRIX

100158 circuit shifts data bits. The three S inputs give the shift count from zero to seven. The M input forces a low level on the higher order bits for fill shift, or enables and end around shift.





Pin connections for flat pack and in ( ) for SLIM DIP packages.

QUICK REFERENCE DATA

Average propagation delay (Data)	t_P	typ.	1.9	ns
Power consumption per package	$P_{(AV)}$	typ.	540	mW

PACKAGE OUTLINE (See general section)

ORDERING INFORMATION : 100158 F (FO 44-24 lead ceramic flat pack)
100158 D (FO 72-24 lead Slim Cerdip)

TRUTH TABLE

	Inputs				Outputs							
	22 M	23 S_2	20 S_1	19 S_0	4 Q_7	5 Q_6	6 Q_5	7 Q_4	11 Q_3	12 Q_2	12 Q_1	14 Q_0
No shift	X	L	L	L	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Left shift	L	L	L	H	L	D_7	D_6	D_5	D_4	D_3	D_2	D_1
	L	L	H	L	L	L	D_7	D_6				
	L	L	H	H	L	L	L	D_7	D_6			
	L	H	L	L	L	L	L	L	D_7	D_6		
	L	H	L	H	L	L	L	L	L	D_7	D_6	
	L	H	H	L	L	L	L	L	L	L	D_7	D_6
	L	H	H	L	L	L	L	L	L	L	L	D_7
End around carry	H	L	L	H	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1
	H	L	H	L	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2
	H	L	H	H	D2	D_1	D_0	D_7	D_6	D_5	D_4	D_3
	H	H	L	L	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4
	H	H	L	H	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5
	H	H	H	L	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6
	H	H	H	H	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7

Positive logic : H = HIGH state
L = LOW state
blank = Immaterial state

RATINGS (See family specifications)

D.C. CHARACTERISTICS at V_{CC} = ground ; V_{EE} = − 4.5 V
(for test table and diagram, see family specifications)

	Symbol	T_{amb} (°C) 0 to + 85	Conditions
Input current LOW	I_{IL} min.	0.5 μA	Apply − 1.81 ± 0.005 V to each input, one at a time, with all other inputs open.
Input current HIGH	I_{IH} max.		
	Pins 19-20-22-23	220 μA	Apply −0.88 ± 0.005 V to each input, one at a time, with all other inputs open.
	Pins 1-2-3-15-16-17-18-19	220 μA	
Supply current	$-I_{EE}$ min.	84 mA	Apply −0.95 ± 0.005 V to all inputs.
	typ.	120 mA	
	max.	168 mA	
		T_{amb} (°C): 25	
Voltage compensation	$\frac{\Delta V_{OH}}{\Delta V_{EE}}$ max.	0.025	
	$\frac{\Delta V_{OL}}{\Delta V_{EE}}$ max.	0.055	

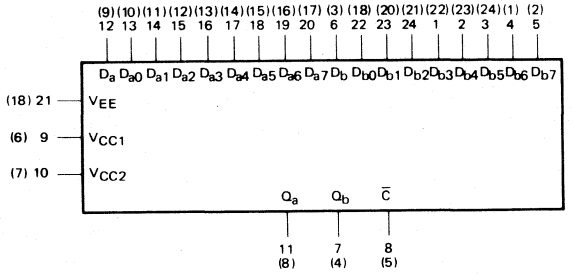
A.C. CHARACTERISTICS at V_{CC} = ground; V_{EE} = −4.5 V; load = 50 Ω to −2 V; T_{amb} = 25° C

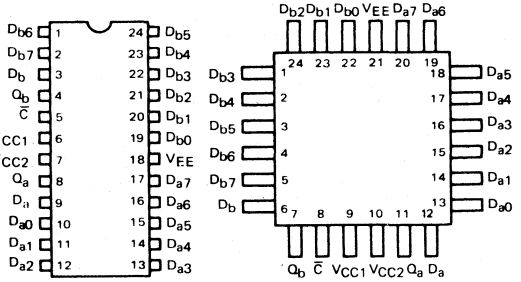
	Symbol	min.	typ.	max.	Conditions
Rise time	t_{TLH} (ns)	0.5		2.2	
Fall time	t_{THL} (ns)	0.5		2.2	
Propagation delays					
S0 - S_1 - S_2 to outputs	t_{PSQ} (ns)	1.9		4.7	Appy a reference signal to pins 19 - 20 - 23.
Data to outputs	t_{PDQ} (ns)	1.1		2.7	Apply a reference signal to pins 15 - 16 - 17 - 18 - 2 - 4 - 1 - 3
M to outputs	t_{PMQ} (ns)	2		4.9	Apply a reference signal to pin 22

These limits are for flat packs.
Add 0.2 ns to max. values for SLIM DIP package propagation delays.

DUAL 9-BIT PARITY GENERATOR / 8-BIT COMPARATOR

100160 is a dual 9-bit parity generator. It generates high parity outputs for an even number of high inputs on respective 9 bit input groups. The circuit alson compares 8 pairs of inputs and has a low output (C), if all 8 pairs are equal. The inputs Da, Db have the shorter through-put delay and can serve for generating parity for 16 or more bits.





Pin connections for flat pack and in ( ) for SLIM DIP packages.

QUICK REFERENCE DATA

Average propagation delay	t_P	typ.		
Power consumption per package	$P_{(AV)}$	typ.	405	mW

PACKAGE OUTLINE (See general section)

ORDERING INFORMATION : 100160 F (FO 44-24 lead ceramic flat pack)
100160 D (FO 72-24 lead Slim Cerdip)

TRUTH TABLE

Inputs		Outputs		
Data (a) 12 to 20	Data (b) 1 to 6, 22, 23,24	Q_a 11	Q_b 7	$\overline{C}$ 8
Sum of H inputs ODD Sum of H inputs EVEN		L H		
	Sum of H inputs ODD Sum of H inputs EVEN		L H	
13 = 14 and 15 = 16 and 17 = 18 and 19 = 20 and 22 = 23 and 24 = 1 and 4 = 5 ; 6 and 12 = X				L
Any other combination				H

Positive logic : H = HIGH state
L = LOW state
X = Immaterial state

RATINGS (See family specifications)

D.C. CHARACTERISTICS at V_{CC} = ground ; V_{EE} = − 4.5 V
(for test table and diagram, see family specifications)

	Symbol	T_{amb} (°C) 0 to + 85	Conditions
Input current LOW	I_{IL} min.	0.5 μA	Apply − 1.81 ± 0.005 V to each input, one at a time, with all other inputs open.
Input current HIGH	I_{IH} max.		Apply − 0.88 ± 0.005 V to each
	Pins 6 -12	340 μA	input, one at a time, with all
	all other inputs	220 μA	other inputs open.
Supply current	$-I_{EE}$ min.	57 mA	Apply − 0.95 ± 0.005 V to all
	typ.	90 mA	inputs.
	max.	115 mA	
		T_{amb} (°C): 25	
Voltage compensation	$\frac{\Delta V_{OH}}{\Delta V_{EE}}$ max.	0.025	
	$\frac{\Delta V_{OL}}{\Delta V_{EE}}$ max.	0.050	

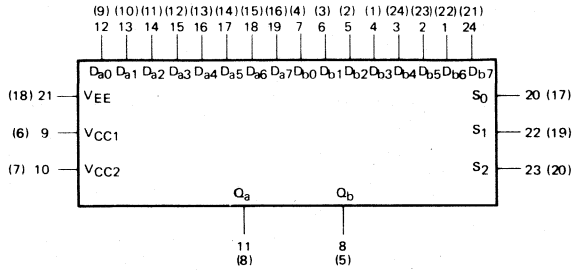
A.C. CHARACTERISTICS at V_{CC} = ground; V_{EE} = −4.5 V; load = 50 Ω to -2 V; T_{amb} = 25° C

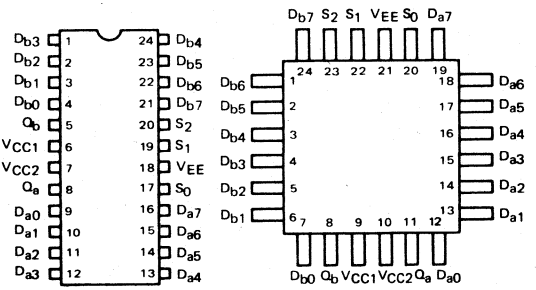
	Symbol	min.	typ.	max.	Conditions
Propagation delays					
Data to parity output	t_{PDP} (ns)				
Pin 6 - 12		0.6		1.4	
Other pins		1.5		3.9	
Data to compare output	t_{PDC} (ns)	1.2		2.9	
Rise time	t_{TLH} (ns)	0.4		1.65	
Fall time	t_{THL} (ns)	0.4		1.65	

These limits are for flat packs.
Add 0.2 ns to max. values for SLIM DIP package propagation delays.

DUAL 8-BIT MULTIPLEXER

100163 circuit is two 8-way multiplexers fed by 3 common address inputs. The 3-bit address select one of eight data lines in each multiplexer, wgich is gated to the output. Ground may be substituted for H on the address input, without changing output limits.





Pin connections for flat pack and in ( ) for SLIM DIP packages.

QUICK REFERENCE DATA

Average propagation delay (Data)	t_P	typ.	1.25	ns
Power consumption per package	$P_{(AV)}$	typ.	550	mW

PACKAGE OUTLINE (See general section)

ORDERING INFORMATION : 100163 F (FO 44-24 lead ceramic flat pack)
100163 D (FO 72-24 lead Slim Cerdip)

FUNCTION TABLE

Inputs										Output
Address			Data							
23	22	20	19 24	18 1	17 2	16 3	15 4	14 5	13 6	12 7	11 8
L	L	L	X	X	X	X	X	X	X	L	L
L	L	L	X	X	X	X	X	X	X	H	H
L	L	H	X	X	X	X	X	X	L	X	L
L	L	H	X	X	X	X	X	X	H	X	H
L	H	L	X	X	X	X	X	L	X	X	L
L	H	L	X	X	X	X	X	H	X	X	H
L	H	H	X	X	X	X	L	X	X	X	L
L	H	H	X	X	X	X	H	X	X	X	H
H	L	L	X	X	X	L	X	X	X	X	L
H	L	L	X	X	X	H	X	X	X	X	H
H	L	H	X	X	L	X	X	X	X	X	L
H	L	H	X	X	H	X	X	X	X	X	H
H	H	L	X	L	X	X	X	X	X	X	L
H	H	L	X	H	X	X	X	X	X	X	H
H	H	H	L	X	X	X	X	X	X	X	L
H	H	H	H	X	X	X	X	X	X	X	H

Positive logic : H = HIGH state
L = LOW state
X = Immaterial state

RATINGS (See family specifications)

D.C. CHARACTERISTICS at V_{CC} = ground ; V_{EE} = − 4.5 V
(for test table and diagram, see family specifications)

	Symbol	T_{amb} (°C) 0 to + 85	Conditions
Input current LOW	I_{IL} min.	0.5 μA	Apply − 1.81 ± 0.005 V to each input, one at a time, with all other inputs open.
Input current HIGH	I_{IH} max.		Apply − 0.88 ± 0.005 V to each
	Pins 20-22-23	265 μA	input, one at a time, with all
	all other inputs	340 μA	other inputs open.
Supply current	$-I_{EE}$ min.	76 mA	Apply − 0.95 ± 0.005 V to all
	max.	153 mA	inputs.
		T_{amb} (°C) : 25	
Voltage compensation	$\frac{\Delta V_{OH}}{\Delta V_{EE}}$ max.	0.025	
	$\frac{\Delta V_{OL}}{\Delta V_{EE}}$ max.	0.050	

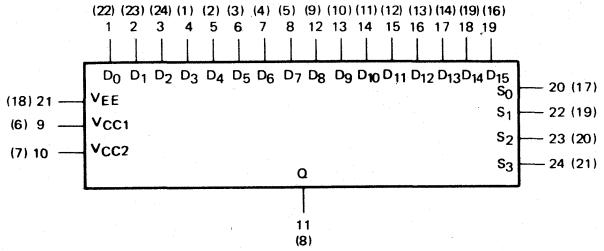
A.C. CHARACTERISTICS at V_{CC} = ground; V_{EE} = −4.5 V; load = 50 Ω to −2 V; T_{amb} = 25° C

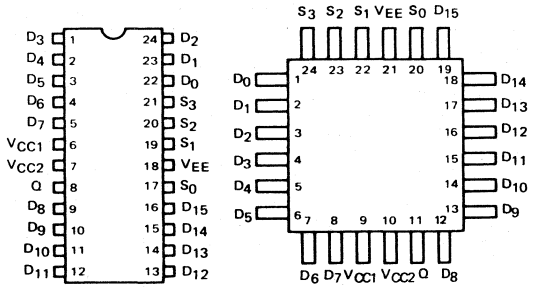
	Symbol		min.	typ.	max.	Conditions
Propagation delays						
Data to output	t_{PDQ}	(ns)	0.8		1.7	
Address to output	t_{PAQ}	(ns)	1.4		2.6	
Rise time	t_{TLH}	(ns)	0.5		1.7	
Fall time	t_{THL}	(ns)	0.5		1.7	

These limits are for flat packs.
Add 0.2 ns to max. values for SLIM DIP package propagation delays.

16 INPUT MULTIPLEXER

100164 is a 16 way multiplexer for one bit.
Four adress inputs select one of the 16 input bits which is gated to the output.





Pin connections for flat pack and in ( ) for SLIM DIP packages.

QUICK REFERENCE DATA

Average propagation delay	t_P (data)	typ.	1.6	ns
Power consumption per package	$P_{(AV)}$	typ.	325	mW

PACKAGE OUTLINE (See general section)

ORDERING INFORMATION : 100164 F (FO 44-24 lead ceramic flat pack)
100164 D (FO 72-24 lead Slim Cerdip)

TRUTH TABLE

Inputs				Output
S_3 24	S_2 23	S_1 22	S_0 20	Q 11
L	L	L	L	D_0
L	L	L	H	D_1
L	L	H	L	D_2
L	L	H	H	D_3
L	H	L	L	D_4
L	H	L	H	D_5
L	H	H	L	D_6
L	H	H	H	D_7
H	L	L	L	D_8
H	L	L	H	D_9
H	L	H	L	D_{10}
H	L	H	H	D_{11}
H	H	L	L	D_{12}
H	H	L	H	D_{13}
H	H	H	L	D_{14}
H	H	H	H	D_{15}

Positive logic : H = HIGH state
L = LOW state

RATINGS (See family specifications)

D.C. CHARACTERISTICS at V_{CC} = ground ; V_{EE} = −4.5 V
(for test table and diagram, see family specifications)

	Symbol	T_{amb} (°C) 0 to + 85	Conditions
Input current LOW	I_{IL} min.	0.5 μA	Apply −1.81 ± 0.005 V to each input, one at a time, with all other inputs open.
Input current HIGH	I_{IH} max.		Apply −0.88 ± 0.005 V to each
	Pins 20-22	240 μA	input, one at a time, with all
	Pins 23-24	240 μA	other inputs open.
	all other inputs	280 μA	
Supply current	$-I_{EE}$ min.	49 mA	Apply −0.95 ± 0.005 V to all
	max.	98 mA	inputs.
		T_{amb} (°C): 25	
Voltage compensation	$\frac{\Delta V_{OH}}{\Delta V_{EE}}$ max.	0.025	
	$\frac{\Delta V_{OL}}{\Delta V_{EE}}$ max.	0.050	

A.C. CHARACTERISTICS at V_{CC} = ground; V_{EE} = −4.5 V; load = 50 Ω to −2 V; T_{amb} = 25° C

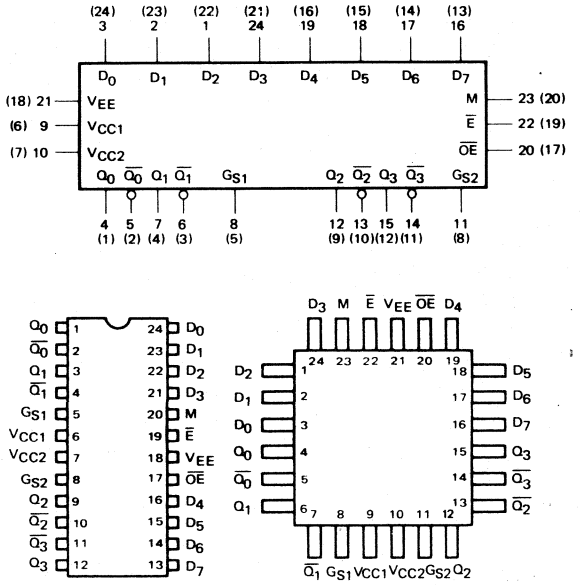
	Symbol	min.	typ.	max.	Conditions
Propagation delays					
Address to output	t_{PAQ} (ns)				
S_2, S_3 pins 23-24		1.1		2.4	
S_0, S_1 pins 20-22		1.45		3.2	
Data to output	t_{PDQ} (ns)	1		2.15	
Rise time	t_{TLH} (ns)	0.65		1.6	
Fall time	t_{THL}				

These limits are for flat pack.
Add 0.2 ns to max. values for SLIM DIP package propagation delays.

100 165

UNIVERSAL PRIORITY ENCODER

100165 operates as a dual 4 input decoder, or as a single 8 input decoder, the operating mode is fixed by the mode control input. The circuit contains eight latch inputs with a common enable (E), and generates the binary address (Q) of the highest priority input, having a high signal and a relevant group signal output (GS). A high signal on the output enable output (OE) forces all outputs low.
The GS output of a higher priority group and the OE input of the next lower priority group can be tied together to accomodate more inputs.



Pin connections for flat pack and in ( ) for SLIM DIP packages.

QUICK REFERENCE DATA

Average propagation delay	t_P	typ.		
Power consumption per package	$P_{(AV)}$	typ.	585	mW

PACKAGE OUTLINE (See gneral section)

ORDERING INFORMATION : 100165 F (FO 44-24 lead ceramic flat pack)
100165 D (FO 72-24 lead Slim Cerdip)

TRUTH TABLE

Inputs											Outputs					
E	OE	M	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Q_0	Q_1	Q_2	Q_3	GS_1	GS_2
22	20	23	3	2	1	24	19	18	17	16	4	7	12	15	8	11
L	L	L	H	X	X	X					L	L			H	
L	L	L	L	H	X	X					H	L			H	
L	L	L	L	L	H	X					L	H			H	
L	L	L	L	L	L	H					H	H			H	
L	L	L	L	L	L	L					L	L			L	
L	L	L					H	X	X	X			L	L		H
L	L	L					L	H	X	X			H	L		H
L	L	L					L	L	H	X			L	H		H
L	L	L					L	L	L	H			H	H		H
L	L	L					L	L	L	L			L	L		L
L	L	H	H	X	X	X	X	X	X	X	L	L	L	L	H	H
L	L	H	L	H	X	X	X	X	X	X	H	L	L	L	H	H
L	L	H	L	L	H						L	H	L	L	H	H
L	L	H	L	L	L	H					H	H	L	L	H	H
L	L	H	L	L	L	L	H				L	L	H	L	H	H
L	L	H	L	L	L	L	L	H			H	L	H	L	H	H
L	L	H	L	L	L	L	L	L	H		L	H	H	L	H	H
L	L	H	L	L	L	L	L	L	L	H	H	H	H	L	H	H
L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L
X	H	X	X	X	X	X	X	X	X	X	L	L	L	L	L	L
H	L	L	Given by $D_0 - D_7$ when E = L and M = L													
H	L	H	Given by $D_0 - D_7$ when E = L and M = H													

Positive logic : H = HIGH state
L = LOW state
X = blank = Immaterial

RATINGS (See family specifications)

D.C. CHARACTERISTICS at V_{CC} = ground ; V_{EE} = −4.5 V
(for test table and diagram, see family specifications)

	Symbol		T_{amb} (°C) 0 to + 85		Conditions
Input current LOW	I_{IL}	min.	0.5	μA	Apply −1.81 ± 0.005 V to each input, one at a time, with all other inputs open.
Input current HIGH	I_{IH}	max.	230	μA	Apply −0.88 ± 0.005 V to each input, one at a time, with all other inputs open.
Supply current	$-I_{EE}$	min. typ. max.	77 130 154	mA mA mA	Apply −0.95 ± 0.005 V to all inputs.
			T_{amb} (°C): 25		
Voltage compensation	$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	max.	0.025		
	$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	max.	0.050		

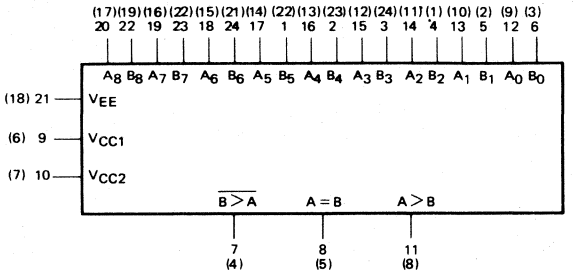
A.C. CHARACTERISTICS at V_{CC} = ground; V_{EE} = −4.5 V; load = 50 Ω to −2 V; T_{amb} = 25° C

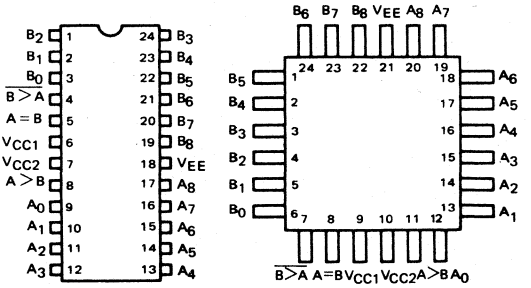
	Symbol		min.	typ.	max.	Conditions
Propagation delays						
Data to Q	t_{PDQ}	(ns)	1.4		3.9	
Data to GS	t_{PDG}	(ns)	1.4		3.9	
$\overline{OE}$ to Q	t_{POQ}	(ns)	1		3.4	
$\overline{OE}$ to GS	t_{POG}	(ns)	1		3.4	
M to Q	t_{PMQ}	(ns)	1		3.4	
$\overline{E} \rightarrow Q$	t_{PEQ}	(ns)	1.6		4.3	
Set-up time	t_{SED}	(ns)	0.6			
Hold time	t_{HED}	(ns)	0.75			
Rise time	t_{TLH}	(ns)	0.5		1.7	
Fall time	t_{THL}	(ns)	0.5		1.7	

These limits are for flat pack.
Add. 0.2 ns to max. values of propagation delays, to min. values of set-up and hold times, to typical values of release time, for SLIMDIP package.

9 – BIT COMPARATOR

100166 is a 9–bit comparator which compares the arithmetic value of two 9–bit words and indicates whether one word is greater or equal to the other one.





Pin connections for flat pack and in ( ) for SLIM DIP packages.

QUICK REFERENCE DATA

Average propagation delay	t_P	typ.	2.2	ns
Power consumption per package	$P_{(AV)}$	typ.	720	mW

PACKAGE OUTLINE (See general section)

ORDERING INFORMATION : 100166 F (FO 44-24 lead ceramic flat pack)
100166 D (FO 72-24 lead Slim Cerdip)

TRUTH TABLE

Inputs									Outputs		
20 19 A_8 B_8	19 23 A_7 B_7	18 24 A_6 B_6	17 1 A_5 B_5	16 2 A_4 B_4	15 3 A_3 B_3	14 4 A_2 B_2	13 5 A_1 B_1	12 6 A_0 B_0	11 $A > B$	7 $B > A$	8 $A = B$
H L L H ↑ $A_8 = B_8$									H	L	H
	H L L H ↑ $A_7 = B_7$								L	H	H
		H L L H ↑ $A_6 = B_6$							H	L	H
			H L L H ↑ $A_5 = B_5$						L	H	H
				H L L H ↑ $A_4 = B_4$					H	L	H
					H L L H ↑ $A_3 = B_3$				L	H	H
						H L L H ↑ $A_2 = B_2$			H	L	H
							H L L H $A_1 = B_1$ $A_1 = B_1$ $A_1 = B_1$		L	H	H
								H L L H $A_0 = A_0$	H	L	H
									L	H	H
									H	L	H
									L	H	H
									H	L	H
									L	H	H
									H	L	H
									L	H	H
									H	L	H
									L	H	H
									H	L	H
									L	H	H
									H	L	H
									L	H	H
									H	L	H
									L	H	H
									L	L	L

Positive logic : H = HIGH state
L = LOW state
blank = Immaterial

RATINGS (See family specifications)

D.C. CHARACTERISTICS at V_{CC} = ground ; V_{EE} = − 4.5 V
(for test table and diagram, see family specifications)

	Symbol		T_{amb} (°C) 0 to + 85		Conditions
Input current LOW	I_{IL}	min.	0.5	μA	Apply − 1.81 ± 0.005 V to each input, one at a time, with all other inputs open.
Input current HIGH	I_{IH}	max.	250	μA	Apply −0.88 ± 0.005 V to each input, one at a time, with all other inputs open.
Supply current	$-I_{EE}$	min. typ. max.	119 160 238	mA mA mA	Apply − 0.95 ± 0.005 V to all inputs.
Voltage compensation			T_{amb} (°C): 25		
	$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	max.	0,035		
	$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	max.	0.070		

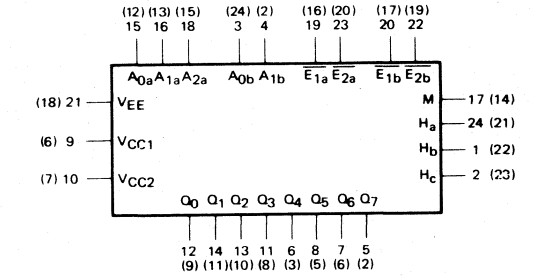
A.C. CHARACTERISTICS at V_{CC} = ground; V_{EE} = - 4.5 V; load = 50 Ω to −2 V; T_{amb} = 25° C

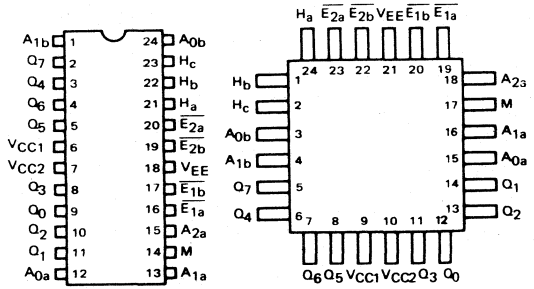
	Symbol		min.	typ.	max.	Conditions
Propagation delays Data to output	t_{PDQ}	(ns)	1.4		4.3	
Rise time	t_{TLH}	(ns)	0.45		1.8	
Fall time	t_{THL}	(ns)	0.45		1.8	

These limits are for flat packs.
Add 0.2 ns to max. values, for SLIM DIP package propagation delays.

UNIVERSAL DEMUX/DECODER

100170 operates as a dual 1 or 4 decoder, or as a single 1 or 8 decoder ; the operating mode is fixed by the mode control input (M). The inputs H_a, H_b, H_c, determine whether the outputs are active low or high. In the 1 of 8 mode, the two pairs of active low enables can be tied together (pin 19 to 20 and 22 to 23), to provide two active low enables.





Pin connections for flat pack and in ( ) for SLIM DIP packages.

QUICK REFERENCE DATA

Average propagation delay (Data : A)	t_P	typ.	1.8	ns
Power consumption per package	$P_{(AV)}$	typ.	495	mW

PACKAGE OUTLINE (See general section)

ORDERING INFORMATION : 100170 F (FO 44-24 lead ceramic flat pack)
100170 D (FO 72-24 lead Slim Cerdip)

TRUTH TABLE

Dual 1 of 4 mode : $M = A_{2a} = H_c$ = LOW

Inputs				Outputs							
				$H_a = H_b$ = HIGH				$H_a = H_b$ = LOW			
$\overline{E_1}$	$\overline{E_2}$	A_1	A_0	Q_0	Q_1	Q_2	Q_3	Q_0	Q_1	Q_2	Q_3
19	23	16	15	12	14	13	11	12	14	13	11
20	20	4	3	6	8	7	5	6	8	7	5
H	x	x	x	L	L	L	L	H	H	H	H
x	H	x	x	L	L	L	L	H	H	H	H
L	L	L	L	H	L	L	L	L	H	H	H
L	L	L	H	L	H	L	L	H	L	H	H
L	L	H	L	L	L	H	L	H	H	L	H
L	L	H	H	L	L	L	H	H	H	H	L

Single 1 of 8 mode : M = HIGH, $A_{0b} = A_{1b} = H_b$ = LOW

Inputs					Outputs														
					H_c = HIGH								H_c = LOW						
E_1	E_2	A_{2a}	A_{1a}	A_{0a}	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
19-20	20-23	18	16	15	12	14	13	11	6	8	7	5	12	14	13	11	6	8	7	5
H	x	x	x	x	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H
x	H	x	x	x	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H
L	L	L	L	L	H	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	L	H	L	H	L	L	L	L	L	L	H	L	H	H	H	H	H	H
L	L	L	H	L	L	L	H	L	L	L	L	L	H	H	L	H	H	H	H	H
L	L	L	H	H	L	L	L	H	L	L	L	L	H	H	H	L	H	H	H	H
L	L	H	L	L	L	L	L	L	H	L	L	L	H	H	H	H	L	H	H	H
L	L	H	L	H	L	L	L	L	L	H	L	L	H	H	H	H	H	L	H	H
L	L	H	H	L	L	L	L	L	L	L	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L

Positive logic : H = HIGH state
L = LOW state
x = Immaterial state

RATINGS (See family specifications)

D.C. CHARACTERISTICS at V_{CC} = ground ; V_{EE} = − 4.5 V
(for test table and diagram, see family specifications)

	Symbol	T_{amb} (°C) 0 to + 85	Conditions
Input current LOW	I_{IL} min.	0.5 μA	Apply −1.81 ± 0.005 V to each input, one at a time, with all other inputs open.
Input current HIGH	I_{IH} max.		Apply − 0.88 ± 0.005 V to each
	Pins 1-15-16-18	310 μA	input, one at a time, with all other
	other inputs	250 μA	inputs open.
Supply current	$-I_{EE}$ min.	76 mA	Apply − 0.95 ± 0.005 V to all
	typ.	110 mA	inputs.
	max.	153 mA	
		T_{amb} (°C): 25	
Voltage compensation	$\frac{\Delta V_{OH}}{\Delta V_{EE}}$ max.	0.025	
	$\frac{\Delta V_{OL}}{\Delta V_{EE}}$ max.	0.050	

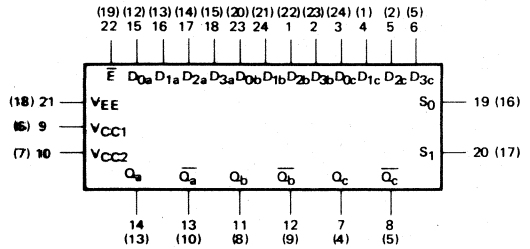
A.C. CHARACTERISTICS at V_{CC} = ground; V_{EE} = − 4.5 V; load = 50 Ω to −2 V; T_{amb} = 25° C

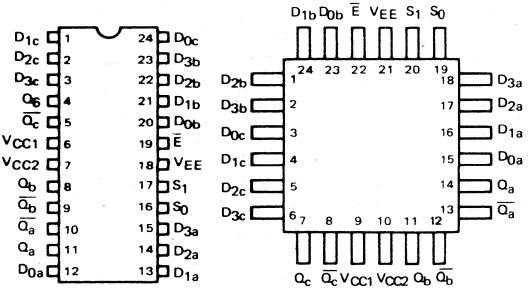
	Symbol		min.	typ.	max.	Conditions
Propagation delays						
Enable to outputs	t_{PEQ}	(ns)	0.7		2.05	
Inputs (A) to outputs	t_{PAQ}	(ns)	1.25		2.5	
Inputs (H) to outputs	t_{PHQ}	(ns)	1.2		2.85	
Mode control to output	t_{PMQ}	(ns)	1.5		3.9	
Rise time	t_{TLH}	(ns)	0.55		3.2	
Fall time	t_{THL}	(ns)	0.55		3.2	

These limits are for flat packs.
Add 0.2 ns to max. values, for SLIM DIP package propagation delays.

TRIPLE BIT 4 WAY MULTIPLEXER

100171 is a triple bit, 4 way multiplexer fed by 2 common address inputs, with complement and data outputs. A high state on the enable input (E) forces all true outputs low.





Pin connections for flat pack and in ( ) for SLIM DIP packages.

QUICK REFERENCE DATA

Average propagation delay (Data)	t_P	typ.	0.95	ns
Power consumption per package	$P_{(AV)}$	typ.	340	mW

PACKAGE OUTLINE (See general section)

ORDERING INFORMATION : 100171 F (FO 44-24 lead ceramic flat pack)
100171 D (FO 72-24 lead Slim Cerdip)

TRUTH TABLE

Inputs							Outputs	
22	20	19	15	16	17	18	13	14
22	20	19	23	24	1	2	12	11
22	20	19	3	4	5	6	8	7
E	S_0	S_1	D_0	D_1	D_2	D_3	Q	$\overline{Q}$
H	x	x	x	x	x	x	H	L
L	L	L	L	x	x	x	H	L
L	L	L	H	x	x	x	L	H
L	L	H	x	L	x	x	H	L
L	L	H	x	H	x	x	L	H
L	H	L	x	x	L	x	H	L
L	H	L	x	x	H	x	L	H
L	H	H	x	x	x	L	H	L
L	H	H	x	x	x	H	L	H

Positive logic : H = HIGH state
L = LOW state
x = Immaterial state

RATINGS (See family specifications)

D.C. CHARACTERISTICS at V_{CC} = ground ; V_{EE} = − 4.5 V
(for test table and diagram, see family specifications)

	Symbol	T_{amb} (°C) 0 to + 85	Conditions
Input current LOW	I_{IL} min.	0.5 μA	Apply − 1.81 ± 0.005 V to each input, one at a time, with all other inputs open.
Input current HIGH	I_{IH} max.		Apply − 0.88 ± 0.005 V to each
	Pins 19-20-22	300 μA	input, one at a time, with all other
	other inputs	340 μA	inputs open.
Supply current	$-I_{EE}$ min.	56 mA	Apply − 0.95 ± 0.005 V to all
	typ.	75 mA	inputs.
	max.	114 mA	
		T_{amb} (°C): 25	
Voltage compensation	$\frac{\Delta V_{OH}}{\Delta V_{EE}}$ max.	0.035	
	$\frac{\Delta V_{OL}}{\Delta V_{EE}}$ max.	0.070	

A.C. CHARACTERISTICS at V_{CC} = ground; V_{EE} = −4.5 V; load = 50 Ω to −2 V; T_{amb} 25° C

	Symbol		min.	typ.	max.	Conditions
Propagation delays						
Enable to outputs	t_{PEQ}	(ns)	0.9		2.2	
Data to outputs	t_{PDQ}	(ns)	0.55		1.5	
Address to outputs	t_{PAQ}	(ns)	1.25		2.6	
Rise time	t_{TLH}	(ns)	0.45		1.35	
Fall time	t_{THL}	(ns)	0.45		1.35	

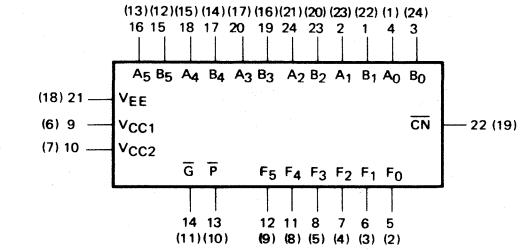
These limits are for flat packs.
Add 0.2 ns to max. values, for SLIM DIP package propagation delays.

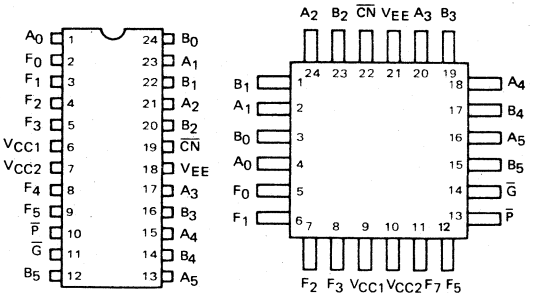
100 180

Preliminary data sheet

FAST 6 BIT ADDER

100180 is a high speed 6 bit adder which performs a full 6 bit addition of 2 operands in 2 ns. The inputs are : carrying (CN) (active low), operands A (An), operands B (Bn) ; the outputs are : function (Fn), carry generate (G) (active low), carry propagate (P) (active low).





Pin connections for flat pack and in ( ) for SLIM DIP packages.

Pin connections for flat pack (SLIM DIP) package.

QUICK REFERENCE DATA

Average propagation delay	t_P	typ.	2	ns
Power consumption per package	$P_{(AV)}$	typ.	968	mW

PACKAGE OUTLINE (See general section)

ORDERING INFORMATION : 100180 F (FO 44-24 lead ceramic flat pack)
100180 D (FO 72-24 lead Slim Cerdip)

$F_0 = P_0 \oplus C_N$

$F_1 = P_1 \oplus (G_0 + P_0 C_N)$

$F_2 = P_2 \oplus (G_1 + P_1 G_0 + P_1 P_0 C_N)$

$F_3 = P_3 \oplus (G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_N)$

$F_4 = P_4 \oplus (G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 C_N)$

$F_5 = P_5 \oplus (G_4 + P_4 G_3 + P_4 P_3 G_2 + P_4 P_3 P_2 G_1 + P_4 P_3 P_2 P_1 G_0 + P_4 P_3 P_2 P_1 P_0 C_N)$

$\overline{P} = \overline{P_0 P_1 P_2 P_3 P_4 P_5}$

$\overline{G} = \overline{G_5 + P_5 G_4 + P_5 P_4 G_3 + P_5 P_4 P_3 G_2 + P_5 P_4 P_3 P_2 G_1 + P_5 P_4 P_3 P_2 P_1 G_0}$

$P_i = A_i \oplus B_i$

$G_i = A_i \cdot B_i$

$(i = 0, 1, 2, 3, 4, 5)$

RATINGS (See family specifications)

D.C. CHARACTERISTICS at V_{CC} = ground ; V_{EE} = −4.5 V
(for test table and diagram, see family specifications)

	Symbol		T_{amb} (°C) 0 to + 85	Conditions
Input current LOW	I_{IL}	min.	0.5 μA	Apply −1.81 ± 0.005 V to each input, one at a time, with all other inputs open.
Input current HIGH	I_{IH}	max.	220 μA	Apply − 0.88 ± 0.005 V to each input, one at a time, with all other inputs open.
Supply current	$-I_{EE}$	typ.	215 mA	Apply − 0.95 ± 0.005 V to all inputs.
			T_{amb} (°C): 25	
Voltage compensation	$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	max.	0.025	
	$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	max.	0.050	

A.C. CHARACTERISTICS at V_{CC} = ground; V_{EE} = −4.5 V; load = 50 Ω to −2 V; T_{amb} = 25° C

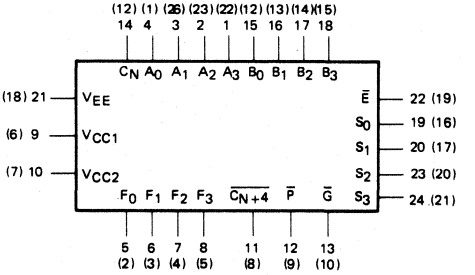
	Symbol		min.	typ.	max.	Conditions
Rise time	t_{TLH}	(ns)		1.1		
Fall time	t_{THL}	(ns)				
Propagation delays						
Operands to F_n outputs	t_{POF}	(ns)		2		
Operands to carry propagate ($\overline{P}$)	t_{POP}	(ns)		1.9		
Operands to carry generate ($\overline{G}$)	t_{POG}	(ns)		1.9		
Carry in ($\overline{CN}$) to F_n outputs	t_{PCF}	(ns)		2		

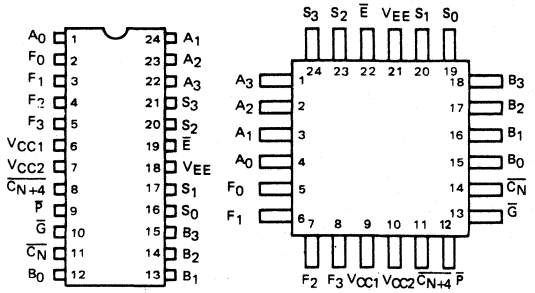
These limits are for flat packs.
Add 0.2 ns to max. values, for SLIM DIP package propagation delays.

Preliminary data sheet

4–BIT BINARY/BCD ALU

100181 is a 4–bit Binary/BCD Arithmetic Logic Unit which performs eight logic operations and eigh arithmetic operations on two 4–bit words. Arithmetic and logic operations are selected by a 4–bit select input (S_0, S_3). The circuit performs BCD addition and substraction, in supplement of binary arithmetic.
It contains four output latches, in order to increase operating speed. The latches are transparent, when the enable input ($\overline{E}$) is open. The internal look ahead carry minimizes delay to the F outputs and to the ripple carry output ($\overline{C_{N+4}}$). Group carry look ahead propagate ($\overline{P}$) and generate ($\overline{G}$) outputs are also provided with independance from carry in ($\overline{C_0}$). P output goes low when a plus operation produces fifteen (or nine in BCD), or when a minus operation produces zero. $\overline{G}$ output goes low when the sum of word A and word B is greater than fifteen (or nine in BCD), or when their difference is greater than zero in a minus mode.





Pin connections for flat pack and in ( ) for SLIM DIP packages.

QUICK REFERENCE DATA

Average propagation delay	t_p	typ.		
Power consumption per package	$P_{(AV)}$	typ.	950	mW

PACKAGE OUTLINE (See general section)

ORDERING INFORMATION : 100181 F (FO 44-24 lead ceramic flat pack)
100181 D (FO 72-24 lead Slim Cerdip)

LOGIC TABLE

S_3	S_2	S_1	S_0	Functions	
				$\overline{C_0}$ = H	$\overline{C_0}$ = L
L	L	L	L	A plus B (BCD)	A plus B plus 1 (BCD)
L	L	L	H	A minus B (BCD)	A minus B plus 1 (BCD)
L	L	H	L	B minus A (BCD)	B minus A plus 1 (BCD)
L	L	H	H	O minus B (BCD)	O minus B plus 1 (BCD)
L	H	L	L	A plus B (Binary)	A plus B plus 1 (Binary)
L	H	L	H	A minus B (Binary)	A minus B plus 1 (Binary)
L	H	H	L	B minus A (Binary)	B minus A plus 1 (Binary)
L	H	H	H	O minus B (Binary)	O minus B plus 1 (Binary)
H	L	L	L	$F_n = A_n B_n + \overline{A_n B_n}$	← SAME LOGIC
H	L	L	H	$F_n = A_n \overline{B_n} + \overline{A_n} B_n$	
H	L	H	L	$F_n = A_n = B_n$	
H	L	H	H	$F_n = A_n$	
H	H	L	L	$F_n = \overline{B_n}$	
H	H	L	H	$F_n = B_n$	
H	H	H	L	$F_n = A_n \cdot B_n$	
H	H	H	H	F_n = LOW	

Positive logic : L = LOW state
H = HIGH state.

When $\overline{C_0}$ is low, BCD substractions are performed in ten's complement, or binary substractions are performed in one's complement.

RATINGS (See family specifications)

D.C CHARACTERISTICS at V_{CC} = ground ; V_{EE} = − 4.5 V.
(for test table and diagram, see family specifications)

	Symbol	T_{amb} (°C) 0 to + 85	Conditions
Input current LOW	I_{IL} min.	0.5 μA	Apply − 1.81 ± 0.005 V to each input, one at a time, with all other inputs open.
Input current HIGH	I_{IH} max.		Apply − 0.88 ± 0.005 V to each inputs, one at a time, with all other inputs open.
	Pins 19-20		
	22-23-24	350 μA	
	other inputs	250 μA	
Supply current	$-I_{EE}$ min.	135 mA	Apply − 0.95 ±0.005 V to all inputs.
	max.	270 mA	
		T_{amb} (°C): 25	
Voltage compensation	$\frac{\Delta V_{OH}}{\Delta V_{EE}}$ max.	0.025	
	$\frac{\Delta V_{OL}}{\Delta V_{EE}}$ max.	0.050	

A.C. CHARACTERISTICS at V_{CC} = ground; V_{EE} = −4.5 V; load = 50 Ω to −2 V; T_{amb} = 25°C

	Symbol		min.	typ.	max.	conditions
Rise time	t_{TLH}	(ns)	0.5		3.5	
Fall time	t_{THL}	(ns)	0.5		3.5	
- Propagation delays						
Operands (A_n, B_n) to (F_n) output	t_{POF}	(ns)	2.1		7.9	
Operands (A_n, B_n) to ($\overline{C_{N+4}}$) carry out	t_{POC}	(ns)	2.4		7.6	
Operands (A_n, B_n) to ($\overline{P}$) carry out	t_{POP}	(ns)	1.4		6.3	
Operands (A, B) to ($\overline{G}$) carry generate	t_{POG}	(ns)	1.4		6.3	
Carry in ($\overline{C}$) to (F_n) output	t_{PCF}	(ns)	1.6		5	
Carry in ($\overline{C}$) to ($\overline{C_{N+4}}$) carry out	t_{PCC}	(ns)	1.3		2.6	
Enable ($\overline{E}$) to (F_n) output	t_{PEF}	(ns)	1.3		3.2	
Select (S_n) to (F_n) output	t_{PSF}	(ns)	1.6		8.3	
Select (S_n) to ($\overline{P}$) carry propagate	t_{PSP}	(ns)	2		5.9	
Select (S_n) to ($\overline{G}$) carry generate	t_{PSG}	(ns)	2		5.9	
Select (S_n) to ($\overline{C_{N+4}}$) carry out	t_{PSC}	(ns)	3		8.4	
- Set-up time						
Operands (A_n, B_n) to ($\overline{E}$) enable	t_{SEO}	(ns)	5.4			
Select (S_n) to ($\overline{E}$) enable	t_{SES}	(ns)	8.4			
Carry in ($\overline{C_N}$) to ($\overline{E}$) enable	t_{SEC}	(ns)	2.7			
- Hold time						
Operands (A_n, B_n) to ($\overline{E}$) enable	t_{HEO}	(ns)	−1			
Select (S_n) to ($\overline{E}$) enable	t_{HES}	(ns)	−1.3			
Carry in ($\overline{C_N}$) to ($\overline{E}$) enable	t_{HEC}	(ns)	−0.5			

These limits are for flat pack.
Add. 0.2 ns to max. values of propagation delays, to min. values of set-up and hold times, to typical values of release time, for SLIMDIP package.

ECL100 000 TO TTL INTERFACE

The HXA100255 is a quint bidirectional ECL100 000 to TTL translator. The ECL inputs are compatible with the temperature and voltage compensated ECL100 000 series. A mode control input selects the translation and the CE input enables the translation. M and CE are ECL inputs.

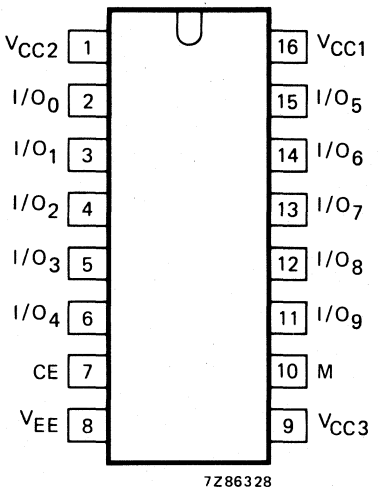


Fig. 1 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground); I/O_0 to I/O_4 are ECL inputs/outputs I/O_5 to I/O_9 are TTL compatible input/outputs. $V_{EE} = -4{,}5$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	$-4{,}5 \pm 5\%$	V
Operating ambient temperature range	T_{amb}	-30 to $+85$	°C
Average propagation delay ECL	t_{TLH}/t_{THL}	$>$ 0,75	ns
TTL	t_{TLH}/t_{THL}	$>$ 1,0	ns

FAMILY DATA see Family Specifications.

PACKAGE OUTLINE (see section package outlines)

HXA100255D: 16-lead DIL, ceramic (SOT-74).

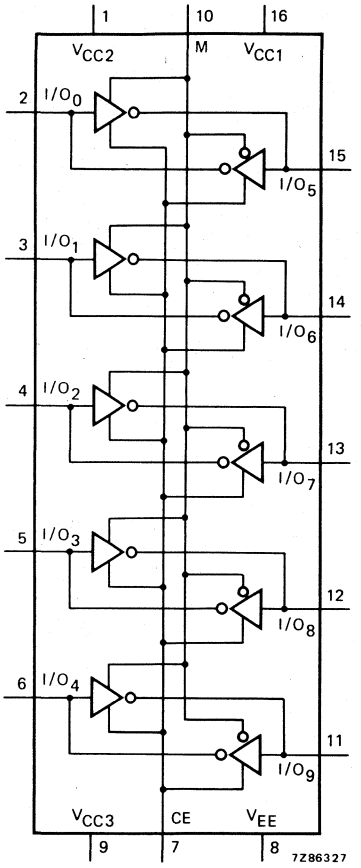


Fig. 2 Logic diagram.

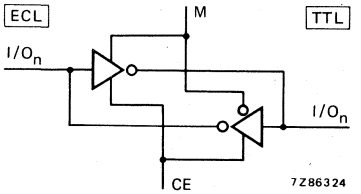


Fig. 3 Logic function.

H = HIGH state = 1
(the more positive voltage)
L = LOW state = 0
(the more negative voltage)
X = state is immaterial
* ECL output in off state; $V_O = V_T$
Z = High impedance TTL output.

Truth table

CE	M	ECL input	TTL output
L	X	L	Z*
H	H	H	L
H	H	L	H

CE	M	TTL input	ECL output
H	L	H	L
H	L	L	H

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 0$ V (ground); $V_{EE} = -4{,}5$ V; $V_{CC3} = 5$ V

ECL output load = $R_L = 25\ \Omega$ to -2 V; $T_{amb} = 0$ to $+85$ °C.

	symbol	min.	typ.	max.	unit	remarks
Input current HIGH						
pins 7, 10	I_{IH}	–	–	350	μA	Apply −0,88 V to each ECL input one at a time
pins 2, 3, 4, 5, 6	I_{IH}	–	–	350	μA	
pins 11, 12, 13, 14, 15	I_{IH}	–	–	40	μA	Apply 2,4 V to each TTL input; one at a time; 0,88 V to pin 7
pins 11, 12, 13, 14, 15	I_{IH}	–	–	1	nA	Apply 5,5 V to each TTL input one at a time; 0,88 V to pin 7
Input current LOW						
pins 7, 10	I_{IL}	0,5			μA	Apply −1,81 V to each input; one at a time
pins 11, 12, 13, 14, 15	I_{IL}	−1,6	–	–	mA	Apply 0,4 V to each TTL input; one at a time; −0,88 V to pin 7
Supply current						
pins 11, 12, 13, 14, 15, and 9	I_{EE}	29	–	44	mA	Apply −0,88 V to ECL inputs, M and CE*
pins 11, 12, 13, 14, 15, and 9	I_{EE}	24	–	36	mA	Apply −1,81 V to ECL inputs; −0,88 V to pins * 7 and 10; $T_{amb} = 25$ °C for all modes
pins 2, 3, 4, 5, 6 and 8	I_{EE}	100	–	135	mA	
Output voltage pins 11, 12, 13, 14, 15						
HIGH	V_{OH}	2,4	–	–	V	$I_O = -2$ mA; $V_{CC3} = 4{,}75$ V
LOW	V_{OL}	–	–	0,4	V	$I_O = 20$ mA; $V_{CC3} = 4{,}75$ V

DEVELOPMENT SAMPLE DATA

* TTL inputs open.

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 0$ V (ground); $V_{EE} = -4{,}5$ V; $V_{CC3} = 5$ V; ECL output load = 25 Ω to −2 V.

	symbol	min.	typ.	max.	unit	remarks *
Transition times ECL outputs rise and fall	$\frac{t_{TLH}}{t_{THL}}$	0,75	—	—	ns	see Fig. 5
TTL outputs rise and fall	$\frac{t_{TLH}}{t_{THL}}$	1,0	—	—	ns	see Fig. 4
Propagation delay times ECL ⟶ TTL	$\frac{t_{PLH}}{t_{PHL}}$	—	—	7	ns	see Fig. 4
TTL ⟶ ECL	$\frac{t_{PLH}}{t_{PHL}}$	—	—	8	ns	see Fig. 5
CE ⟶ ECL	$\frac{t_{PLH}}{t_{PHL}}$	—	—	8	ns	

* Unused ECL outputs connected to −2 V via $R_L = 25\ \Omega$.

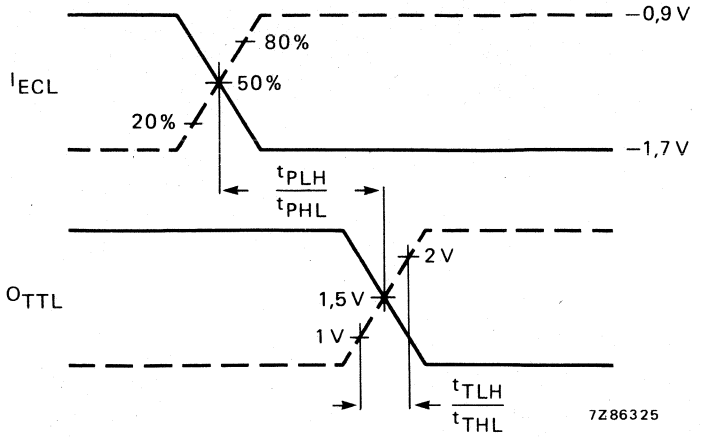


Fig. 4 Waveforms interface ECL to TTL.

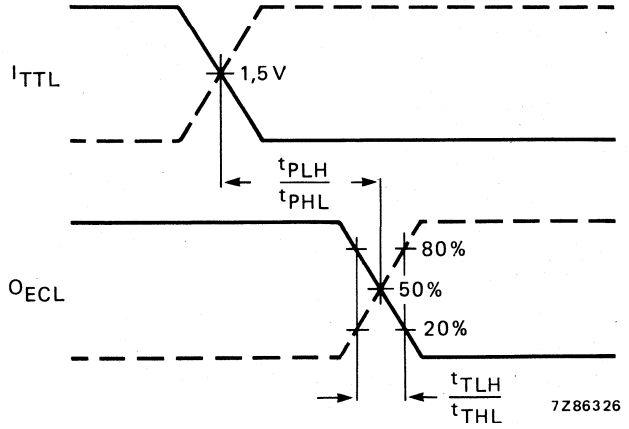


Fig. 5 Waveforms interface TTL to ECL.

1024 x 1-BIT RANDOM ACCESS MEMORIES

The HXA100415 circuits are fully decoded read/write ECL random access memories; organized in 1024-words by 1-bit with a maximum access time of 20, 15 and 10 ns respectively.

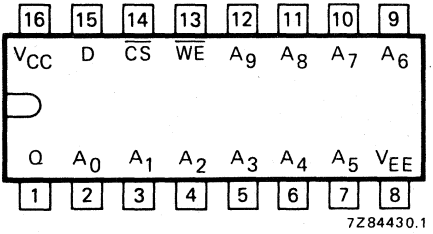


Fig. 1 Pin designation for HXA100415; A and B.

V_{EE} = –4,5 V; V_{CC} = 0 V (ground).

QUICK REFERENCE DATA

Supply voltage	V_{EE}		–4,5 ± 5% V
Operating ambient temperature range	T_{amb}		0 to + 85 °C
Average propagation delay			
HXA100415	t_{PLH}	typ.	12 ns
HXA100415A	t_{PLH}	typ.	8 ns
HXA100415B	t_{PLH}	typ.	6 ns
Output voltage, HIGH state	V_{OH}	typ.	–0,955 V
Output voltage, LOW state	V_{OL}	typ.	–1,715 V
Power consumption per package (no load)	$P_{(AV)}$	typ.	520 mW

For **FAMILY DATA** see Family Specifications.

PACKAGE OUTLINE

HXA100415; A and B 16-lead DIL, ceramic (SOT-74C).

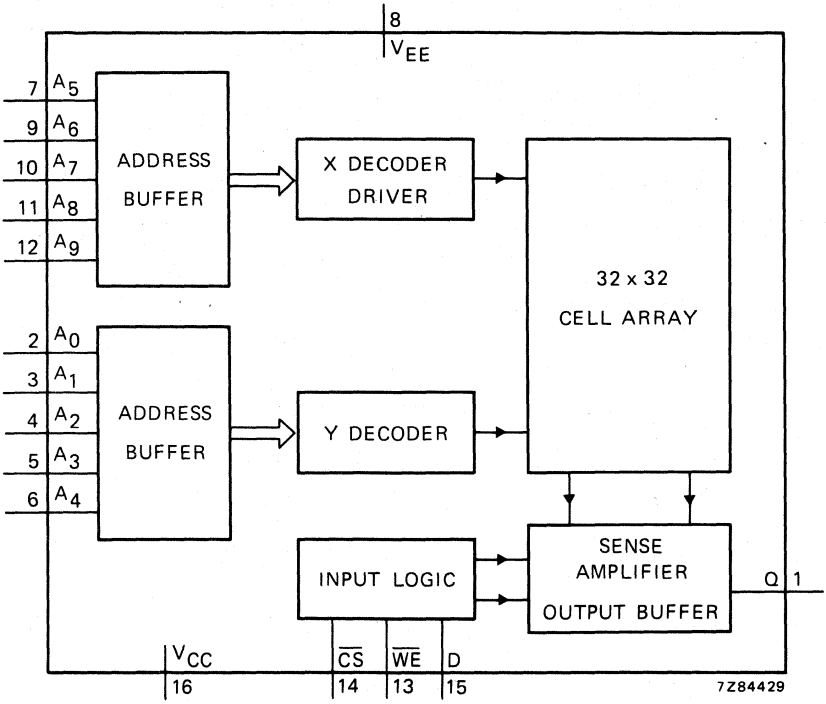


Fig. 2 Block diagram.

FUNCTION TABLE

inputs			output	mode
$\overline{CS}$	$\overline{WE}$	D	Q	
H	X	X	L	disable
L	H	X	X	read mode
L	L	H	write 1	write mode
L	L	L	write 0	write mode

Positive logic:

H = HIGH state = 1
(the more positive voltage)

L = LOW state = 0
(the less positive voltage)

X = state is immaterial

A_0 to A_4	address inputs (y-decoder)
A_5 to A_9	address inputs (x-decoder)
$\overline{CS}$	chip select input
D	data input
$\overline{WE}$	write enable input
V_{CC}	substrate = 0 V = ground
V_{EE}	negative supply (−4,5 V)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{EE}	+0,5 to −7 V
Input voltage	V_I	+0,5 to V_{EE}
Output current	I_O	30 mA
Storage temperature	T_{stg}	−55 to + 150 °C
Operating ambient temperature	T_{amb}	0 to + 85 °C

D.C. CHARACTERISTICS *

V_{CC} = 0 V (ground); V_{EE} = −4,5 V ± 5%. Outputs are terminated via a 50 Ω resistor to −2 V. The circuit is in a test socket or mounted on a printed-circuit board and transverse air flow > 2,5 m/s is maintained. T_{amb} = 0 to 85 °C.

	symbol	min.	typ.	max.	unit	remarks
Input current HIGH	I_{IH}	–	–	220	μA	V_{IHA}
Input current LOW	I_{IL}	−6	–	–	μA	V_{ILB}
Input current chip select LOW	I_{ILCS}	10	–	–	μA	
Supply current	I_{EE}	–	−115	−150	mA	

* For FAMILY DATA see Family Specifications.

A.C. CHARACTERISTICS

V_{CC} = ground; V_{EE} = −4,5 V; load = 50 Ω to −2 V; T_{amb} = 0 to + 75 °C.

	symbol	min.	typ.	max.	unit	remarks
Read mode						
Chip select						
access time	t_{ACS}	–	3	5	ns	see Fig. 3
recovery time	t_{RCS}	–	3	5	ns	see Fig. 3
Address						
access time	t_{AA}	–	12	20	ns	HXA100415
access time	t_{AA}	–	8	15	ns	HXA100415A
access time	t_{AA}	–	6	10	ns	HXA100415B
Write mode						
Write						
pulse duration	t_W	12	8	–	ns	HXA100415
pulse duration	t_W	10	7	–	ns	HXA100415A
pulse duration	t_W	8	6	–	ns	HXA100415B
Set-up times						
A → $\overline{WE}$	t_{WSA}	1	–	–	ns	
CS → $\overline{WE}$	t_{WSCS}	2	–	–	ns	
D → $\overline{WE}$	t_{WSD}	2	–	–	ns	t_W = 12 ns HXA100415
Hold times						t_W = 10 ns HXA100415A
$\overline{WE}$ → A	t_{WHA}	3	–	–	ns	t_W = 8 ns HXA100415B
$\overline{WE}$ → $\overline{CS}$	t_{WHCS}	2	–	–	ns	
$\overline{WE}$ → D	t_{WHD}	2	–	–	ns	
Write						
disable time	t_{WS}	6	2	–	ns	
recovery time	t_{WR}	10	2	–	ns	
Transition						
rise time	t_{TLH}	0,5	2	–	ns	
fall time	t_{THL}	0,5	2	–	ns	
Capacitance						
input pin	C_{IN}	–	–	5	pF	
output pin	C_{OUT}	–	–	5	pF	

INPUT WAVEFORM (100 K FAMILY)

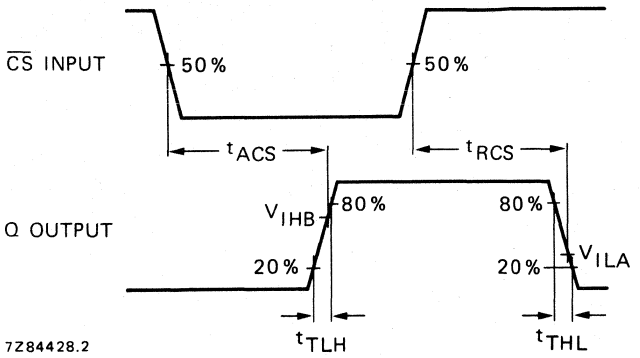


Fig. 3 Read mode propagation delay from chip select.

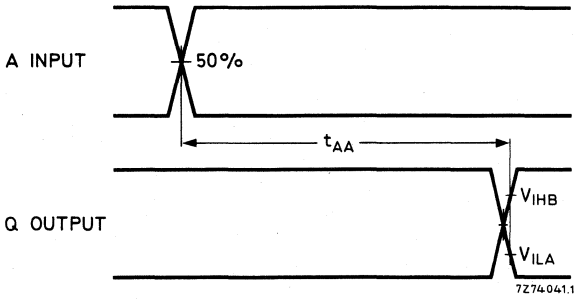


Fig. 4 Read mode propagation delay from address.

Notes

1. Non-specified input pins should be connected to V_{ILmin} or left open.
2. Input and output cables to the oscilloscope are 50 Ω coaxial cables with equal length.
3. Input impedance of the oscilloscope is 50 Ω.
4. The unmatched wire stub between coaxial cable and pins under test must be less than 6 mm long for proper tests.

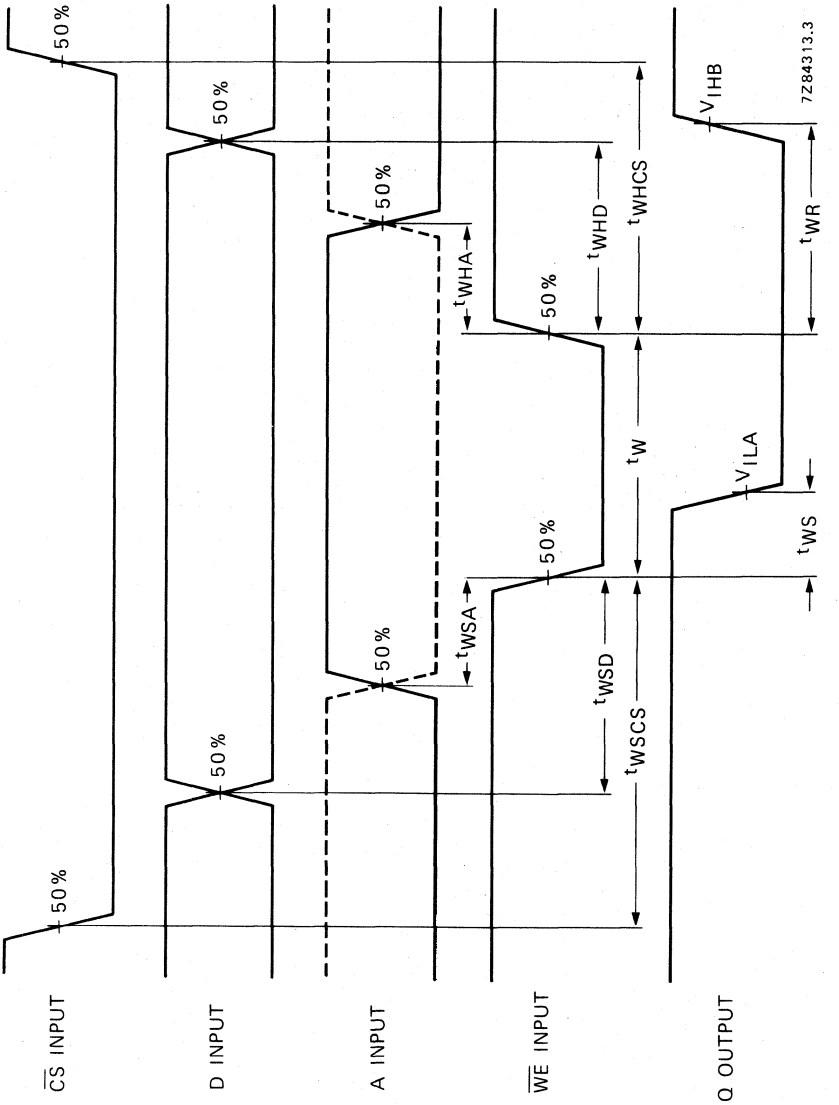


Fig. 5 Write mode waveforms.

256 x 4-BIT RANDOM ACCESS MEMORIES

The devices are 256-word by 4-bit fully decoded ECL read/write random access memories with a maximum access time of 20 ns, 15 ns and 10 ns respectively.

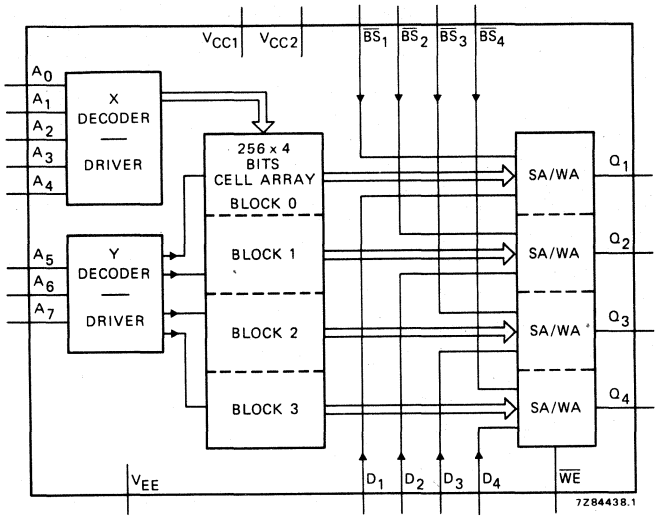


Fig. 1 Block diagram.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−4,5 ± 5% V
Operating ambient temperature	T_{amb}		0 to +85 °C
Average propagation delay			
HXA100422	t_{PHL}	typ.	10 ns
HXA100422A	t_{PHL}	typ.	7,5 ns
HXA100422B	t_{PHL}	typ.	6 ns
Output voltage, HIGH state	V_{OH}	typ.	−0,955 V
Output voltage, LOW state	V_{OL}	typ.	−1,705 V
Power consumption per package (no load)	$P_{(AV)}$		810 mW

For FAMILY DATA see chapter Family Specifications

PACKAGE OUTLINES (see section General)

HXA100422F; AF; BF: 24-lead flat-pack, ceramic, SOT-138.
HXA100422D; AD; BD: 24-lead DIL; ceramic (slim Cerdip), SOT-149

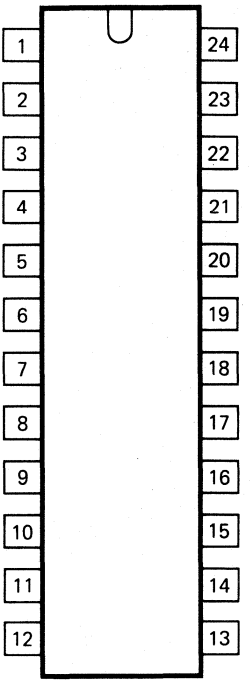


Fig. 2 Pin connections SOT-149.

1 = D_4	13 = D_2
2 = $\overline{BS}_3$	14 = $\overline{WE}$
3 = Q_3	15 = A_5
4 = $\overline{BS}_4$	16 = A_6
5 = Q_4	17 = A_7
6 = V_{CC2}	18 = V_{EE}
7 = V_{CC1}	19 = A_0
8 = Q_1	20 = A_1
9 = $\overline{BS}_1$	21 = A_2
10 = Q_2	22 = A_3
11 = $\overline{BS}_2$	23 = A_4
12 = D_1	24 = D_3

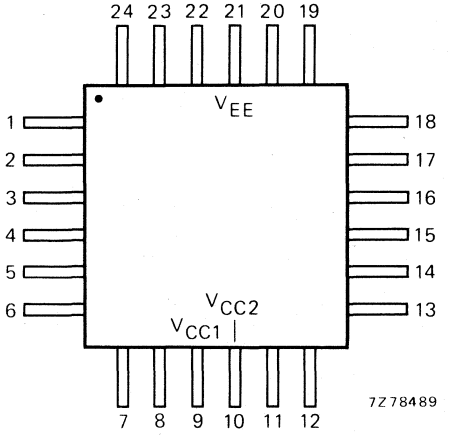


Fig. 3 Pin connections SOT-138.

1 = A_3	13 = Q_2
2 = A_4	14 = $\overline{BS}_2$
3 = D_3	15 = D_1
4 = D_4	16 = D_2
5 = $\overline{BS}_3$	17 = $\overline{WE}$
6 = Q_3	18 = A_5
7 = $\overline{BS}_4$	19 = A_6
8 = Q_4	20 = A_7
9 = V_{CC2}	21 = V_{EE}
10 = V_{CC1}	22 = A_0
11 = Q_1	23 = A_1
12 = $\overline{BS}_1$	24 = A_2

FUNCTION TABLE

inputs			output	mode
$\overline{BS}$	$\overline{WE}$	D	Q	
H	X	X	L	disable
L	L	L	L	write 0
L	L	H	L	write 1
L	H	X	Q	read

Positive logic:

H = HIGH state = 1
(the more positive voltage)

L = LOW state = 0
(the less positive voltage)

X = state is immaterial.

$\overline{BS_1}$ to $\overline{BS_4}$	block select inputs
$\overline{WE}$	write enable
Q_1 to Q_4	data outputs
A_0 to A_4	address inputs (x-decoder)
A_5 to A_7	address inputs (y-decoder)
D_1 to D_4	data inputs
V_{EE}	= −4,5 ± 5% V

$V_{CC1} = V_{CC2} = 0$ V (ground)

RATINGS

Supply voltage	V_{EE}	+ 0,5 to −7	V
Input voltage	V_I	+ 0,5 V to V_{EE}	
Output current (d.c.) HIGH state	I_O	max. 30	mA
Storage temperature	T_{stg}	−55 to + 150	°C

D.C. CHARACTERISTICS (see also chapter Family Specifications)

$V_{CC} = 0$ V (ground); $V_{EE} = -4{,}5$ V ± 5% $R_L = 50\ \Omega$ to −2 V; $T_{amb} = 0$ to 85 °C.
The circuit is in a test socket or mounted on a printed-circuit board and transverse air flow > 2,5 m/s is maintained.

	symbol	min.	typ.	max.	unit	remarks
Input voltage HIGH	V_{IHA}			−880	mV	
	V_{IH}		−950		mV	
	V_{IHB}	−1025			mV	
Input voltage LOW	V_{ILA}			−1620	mV	
	V_{IL}		−1710		mV	
	V_{ILB}	−1810			mV	
Input current HIGH	I_{IH}	−	−	220	μA	V_{IHA}
Input current LOW	I_{IL}	10	−	−	μA	block select
		−6	−	−	μA	other inputs
Supply current	I_{EE}	−	−180	−220	mA	

A.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −4,5 V ± 5%; R_L = 50 Ω to −2 V; T_{amb} = 0 to +85 °C.

	symbol	min.	typ.	max.	unit	remarks
Read mode						
Block select						
access time	t_{ABS}	–	3	5	ns	
recovery time	t_{RBS}	–	3	5	ns	
Address						
access time	t_{AA}	–	10	20	ns	HXA100422
access time	t_{AA}	–	7,5	15	ns	HXA100422A
access time	t_{AA}	–	6	10	ns	HXA100422B
Write mode	t_W	12	8			HXA100422
Write	t_W	10	7	–	ns	HXA100422A
pulse duration	t_W	8	5,5	–	ns	HXA100422
Set-up times						
A → $\overline{WE}$	t_{WSA}	2	–	–	ns	t_W = 12 ns HXA100422 t_W = 10 ns HXA100422A t_W = 8ns HXA100422B
$\overline{BS}$ → $\overline{WE}$	t_{WSBS}	3	–	–	ns	
D → $\overline{WE}$	t_{WSD}	3	–	–	ns	
Hold times						
$\overline{WE}$ → A	t_{WHA}	5	–	–	ns	
$\overline{WE}$ → $\overline{BS}$	t_{WHBS}	4	–	–	ns	
$\overline{WE}$ → D	t_{WHD}	4	–	–	ns	
Write						
disable time	t_{WS}	–	3	5	ns	
recovery time	t_{WR}	–	6	9	ns	
Transition						
rise time	t_{TLH}	–	3	–	ns	between 20% and 80%
fall time	t_{THL}	–	3	–	ns	
Capacitance						
input pin	C_{IN}	–	–	8	pF	
output pin	C_{OUT}	–	–	8	pF	

INPUT WAVEFORMS

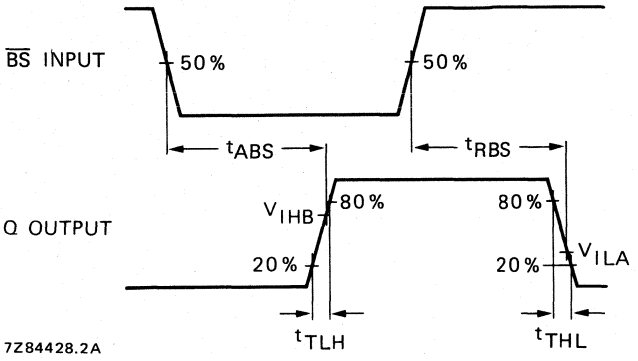


Fig. 4 Read mode propagation delay from block select.

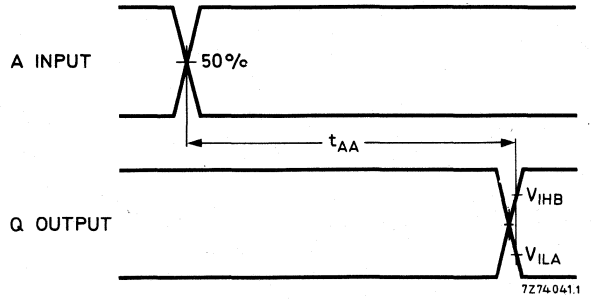


Fig. 5 Read mode propagation delay from address.

Notes

1. Non-specified input pins should be connected to V_{ILmin} or left open.
2. Input and output cables to the oscilloscope are 50 Ω coaxial cables with equal length.
3. Input impedance of the oscilloscope is 50 Ω.
4. The unmatched wire stub between coaxial cable and pins under test must be less than 6 mm long for proper tests.

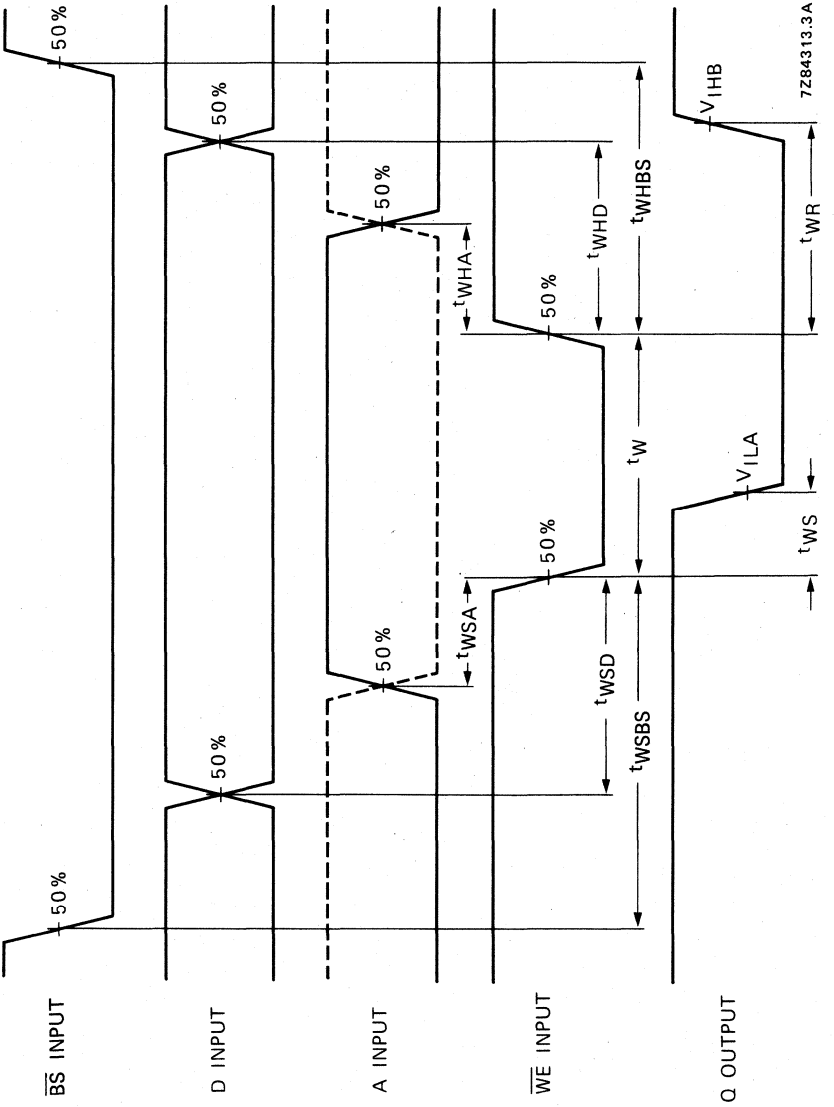


Fig. 6 Write mode waveforms.

MASTER-SLICE LOGIC ARRAY (MLA)

Master-slice logic arrays (MLA) provide the high-performance functional capability of LSI without the costs and delays inherent in full customization. They are especially suitable for computer main-frame and advanced-peripheral application, but also find uses in digital communication systems, real-time data processing, as well as fast instrumentation and test systems.

Using Current Mode Logic (CML) internally, with ECL 100K I/O translation, equivalent gate speeds are down to 0,35 ns. Combined with a gate dissipation of 2,5 mW, this results in speed-power products below 1 picojoule.

The HXA220-XXX (MLA24) and HXA230-XXX (MLA36) have complexities of 500 and 800 equivalent gates, respectively. These are organized into 30 input cell sites, 24 or 36 logic cell sites, and 8 output cell sites. There are a further 20 optional input or output cell sites and 10 minor cell sites. A standard cell library with development software facilitates quick, economic realization of a wide range of LSI logic functions.

External voltage levels and supply requirements make these devices fully compatible with the HXA100 000 family of ECL subnanosecond logic.

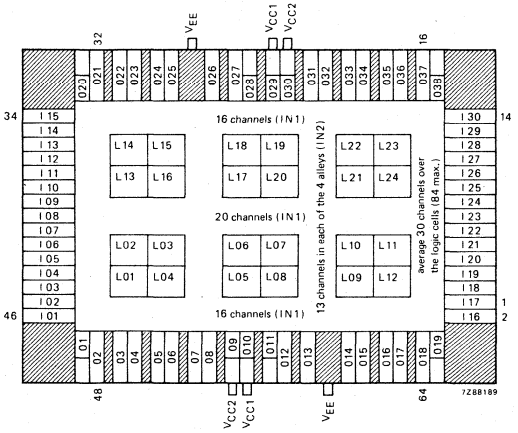


Fig. 1 Cell site locations of HXA220-XXX (MLA24).

Not to scale.
(For HXA230-XXX see page 2.)

QUICK REFERENCE DATA

Supply voltage	V_{EE}	−4,5 ±5%	V
Operating junction temperature range	T_j	30 to 125	°C
Propagation delay time (internal gate)	t_{PLH} typ.	0,5	ns
Power consumption per package (no load)			
HXA220-XXX	P_{av} typ.	1,8	W
HXA230-XXX	P_{av} typ.	2,3	W

PACKAGE OUTLINES

64-pin (FO-75).

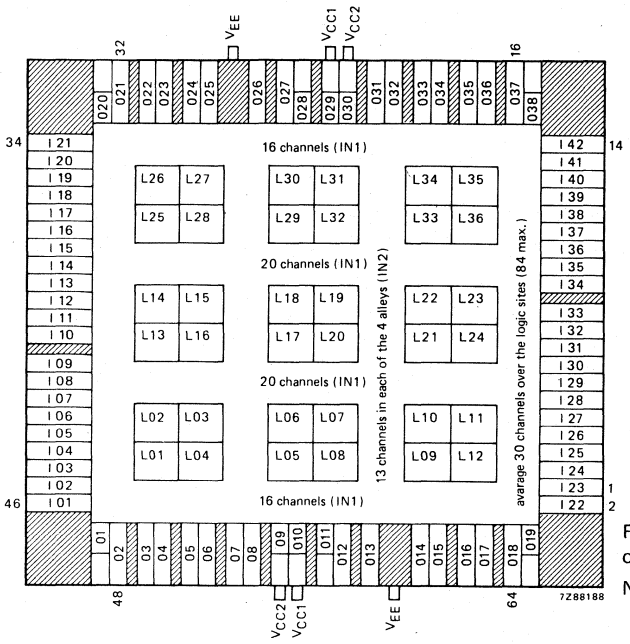


Fig. 2 Cell site location of HXA230-XXX (MLA36).

Not to scale.

The HXA220-XXX and HXA230-XXX contain five basic types of cell sites:

- logic cell sites: 6 or 9 groups of 4 sites each containing 38 transistors, 16 resistors and 4 capacitors;
- input cell sites: each containing 7 transistors and 6 resistors;
- output cell sites: each containing 20 transistors and 11 resistors;
- input/output cell sites: also containing 20 transistors and 11 resistors;
- minor logic cell sites: limited-area for simple functions.

Any logic cell from the cell library can be applied to any suitable cell site, within the limitations imposed by the layout rules. Certain regions of each cell site are always voltage generators. Thus, all necessary bias levels are automatically connected to each logic cell selected.

Features

- Customer-programmable LSI
- Macro-function cell structure
- 500 or 800 equivalent gates
- 3-level customization: 2 metal interconnect layers and one bias layer
- Structure complete with input logic and output cells - all MSI
- SUBILO technology: walled emitters, oxide isolation
- Fully compatible with ECL 100K externally
- 450 mV swing CML internally
- Duplicated V_{CC} pins for increased noise immunity
- 64-pin standard package, 26,92 mm (1,06 inch) square
- 6 supply pins, at least 30 input pins, and up to 28 output pins
- Design process similar to that for MSI devices on p.c.bs, but quicker
- CML gate speed 0,5 ns
- CAD support available
- Fully characterized library of 46 cells

description	HXA220-XXX (MLA24)	HXA230-XXX (MLA36)	unit	remarks
Chip size	28	36	mm^2	
Cell sites				
X-axis: input	30	42		30 input pins
logic	24	36		
Y-axis: output	8	8		8 output pins
output/input	20	20		
minor	10	10		pins on customers
total	92	116		choice
Number of gates				
typical	300	500		
maximum	500	800		
Connection channels				
first metal layer	52 (16 + 20 + 16)	72 (16 + 20 + 20 + 16)		
second metal layer				
maximum	84	84		*
average	52 + 30	52 + 30		52 = 4 x 13
power supply	6	6		
Number of pins	64	64		
Terminal				
output impedance	50	50	Ω	

* These channels cross over the sites and their number may be limited by the cells in the sites.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	$-V_{EE}$	max.	7 V
Output current			
V_I = 100 mV; t_p = 10 μs; δ = 0,01	I_Q	max.	50 mA
Total power dissipation			
HXA220-XXX	P_{tot}	typ.	1,8 W
HXA230-XXX	P_{tot}	typ.	2,3 W
Junction temperature	T_j		30 to 125 °C
Storage temperature	T_{stg}		−65 to + 150 °C

D.C. CHARACTERISTICS*

$V_{CC1} = V_{CC2} = 0$ V (ground); $-V_{EE}$ = 4,5 V ± 5%; R_L = 50 Ω to −2 V.

Supply current			
(typical value defined for each type)	I_{EE}	min.	0,7 I_{typ}
		max.	1,4 I_{typ}
Input current	I_i		0,5 to 265 μA
Output voltage HIGH			
V_{IH} = 0,88 V	$-V_{OHA}$		0,88 V
	$-V_{OH}$	typ.	0,955 V
	$-V_{OHB}$		1,025 V
Output voltage LOW			
V_{IL} = −1,810 V	$-V_{OLA}$		1,620 V
	$-V_{OL}$	typ.	1,705 V
	$-V_{OLB}$		1,810 V

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 0$ V (ground); V_{EE} = −4,5 V ± 5%; R_L = 50 Ω to −2 V.
T_j = 30 to 125 °C.

Propagation delay time			
rise and fall			
internal gate → output	t_{PLH}/t_{PHL}	typ.	0,5 ns
equivalent gate → output	t_{PLH}/t_{PHL}	typ.	0,4 ns
Propagation delay deviation			
test conditions V_I			
$t_r = t_f$ = 0,7 ns	$\pm \Delta t$	max.	40 %
Transition rise			
and fall time			
between 20% and 80%	t_{TLH}/t_{THL}	typ.	1,0 ns

* See also Family Specifications.

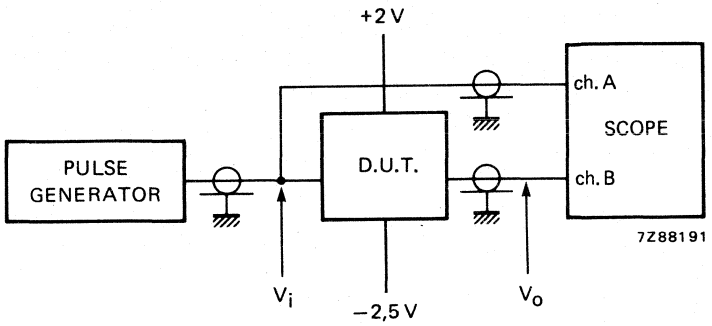


Fig. 3 A.C. test circuit.

V_{CC} = +2 V, V_{EE} = 2,5 V. Input and output connections are 50 Ω coax. Oscilloscope input impedance: 50 Ω.

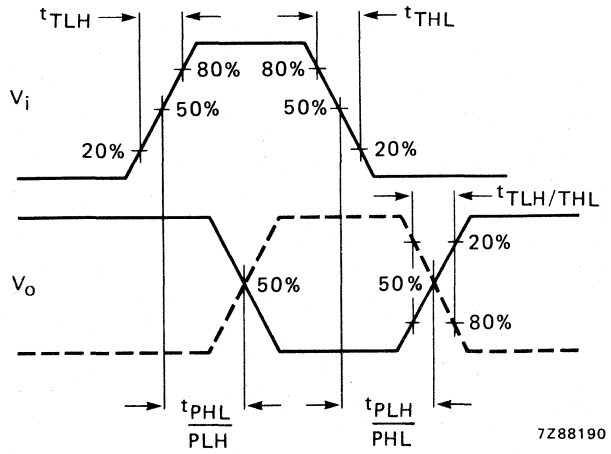


Fig. 4 Switching waveforms.

Input voltage V_{IH} = +1,045 V, V_{IL} = +0,295 V, t_{TLH}/t_{THL} = 0,7 ns.

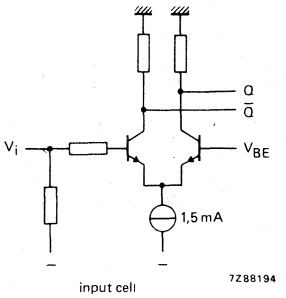


Fig. 5 Input cell.

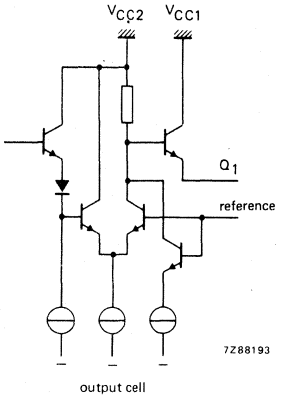


Fig. 7 Output cell.

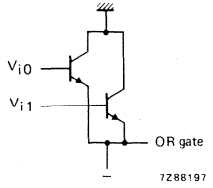


Fig. 9 Expander gates and their connections. Expander gates must be connected to an expander input, therefore to a wired OR-gate.

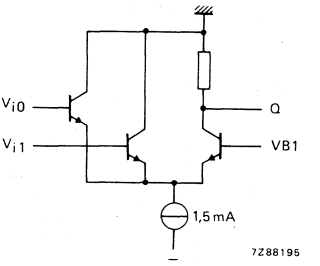


Fig. 6 Basic OR.

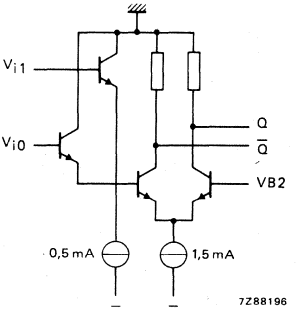


Fig. 8 Basic OR-NOR gate with expander input.

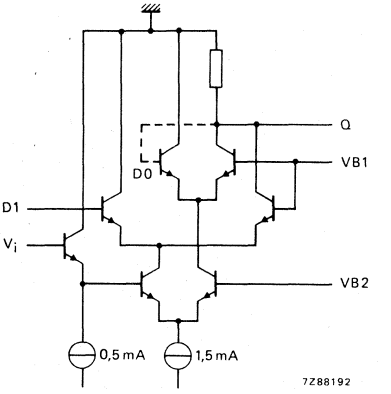


Fig. 10 Basic two-input multiplexer with latch.

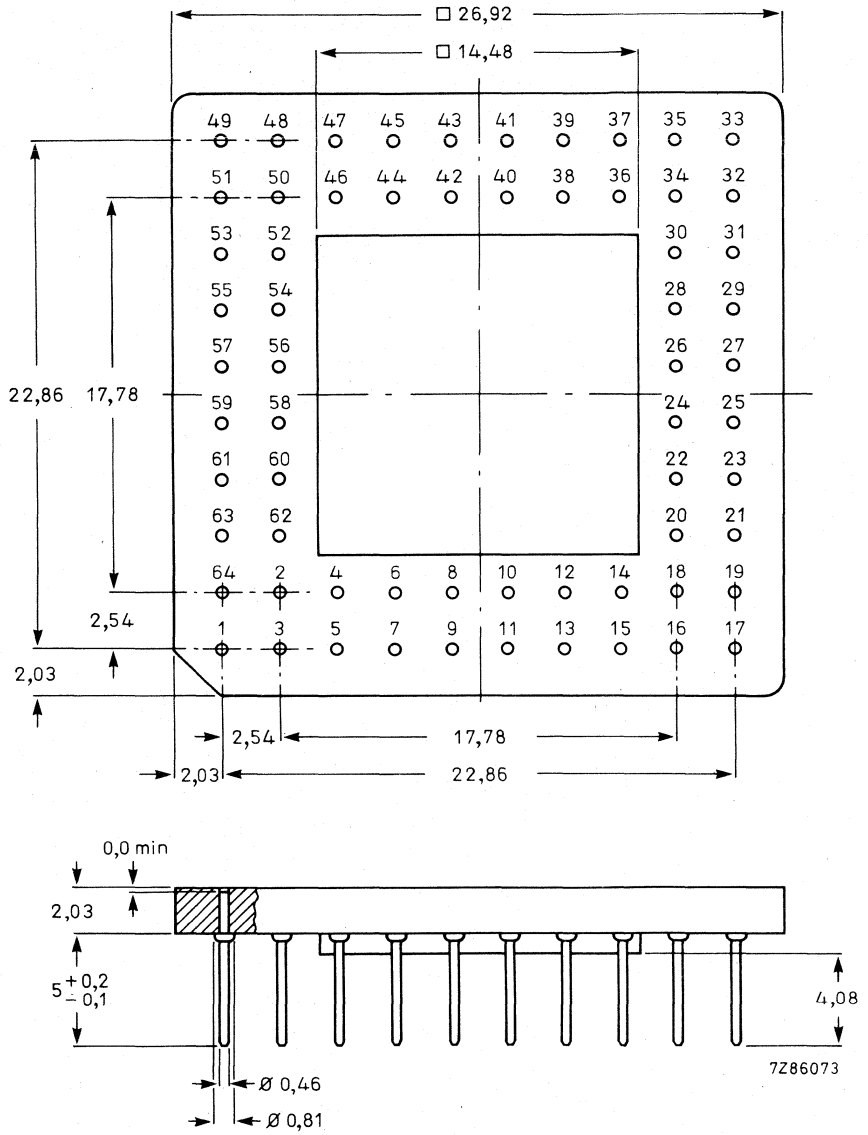


Fig. 11 Mechanical data: 64-pin plug-in package (FO-75).

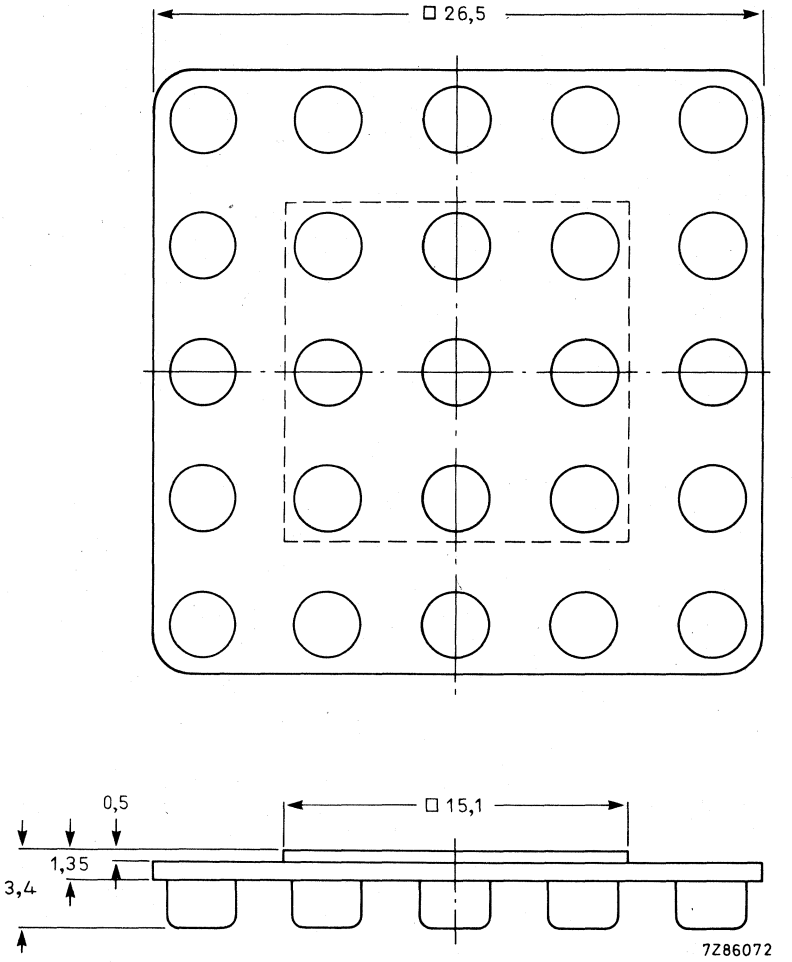


Fig. 12 Mechanical data: heatsink.

THERMAL RESISTANCE

T_{j-a} (K/W)		with air flow*	without
heatsink	with	13	25
	without	25	50

* Forced air flow of 5 m/s (= 1000 linear f/min).

FOUR-BYTE MULTIPLEXER

The HXA220-384 is a high-speed multiplexer that can multiplex four bytes and their parity bit, internally generate the parity of each byte, check it with the input parity bit and generate an output signal, if one of the four bytes parities is inaccurate.

It is intended for:

- EDP — high-speed multiplex, data transfer
- Telecommunications — digital transmission
  — digital multiplex networks
- Data communication — digital networks, high-speed multiplex
- Instrumentation — signal processors
- Video — digital video networks, high level multiplex.

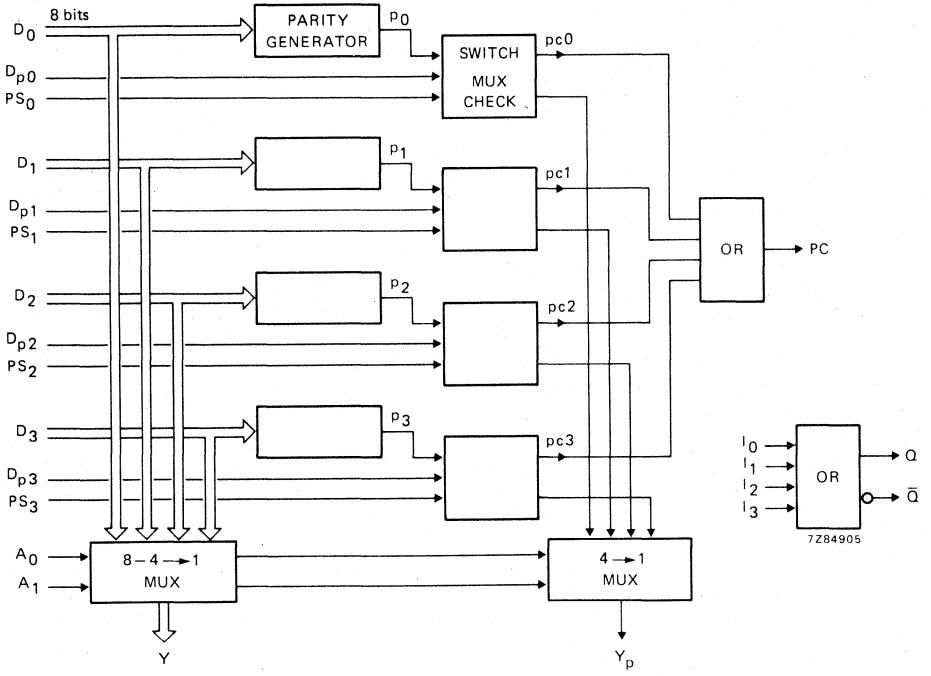


Fig. 1 Block diagram.

PACKAGE OUTLINE

64-pin plug-in package (FO-75)

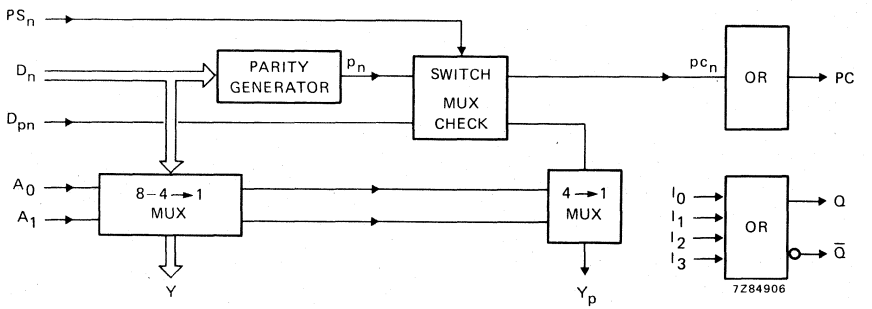


Fig. 2 Block diagram (one multiplexer).

Truth table

A_0	A_1	Y
L	L	D_0
H	L	D_1
L	H	D_2
H	H	D_3

A_0	A_1	PS_0	PS_1	PS_2	PS_3	Y_P
L	L	L	X	X	X	D_{p0}
L	L	H	X	X	X	p0
H	L	X	L	X	X	D_{p1}
H	L	X	H	X	X	p1
L	H	X	X	L	X	D_{p2}
L	H	X	X	H	X	p2
H	H	X	X	X	L	D_{p3}
H	H	X	X	X	H	p3

Positive logic: H = HIGH state {more positive (less negative) voltage)}
L = LOW state {less positive (more negative) voltage)}
X = state is immaterial.

D_{p0} = external parity bit

p0 = internally generated parity bit

pc0 = the check of D_{p0} and $_{p0}$

PC = $pc_0 + pc_1 + pc_2 + pc_3$

$\overline{p1}$ = $D_1{}^0 \oplus D_1{}^1 \oplus D_1{}^2 \oplus D_1{}^3 \oplus D_1{}^4 \oplus D_1{}^5 \oplus D_1{}^6 \oplus D_1{}^7$

pc_1 = $(D_{p1} \oplus p1) \cdot \overline{PS_1}$

$I_0 + I_1 + I_2 + I_3 = Q$ (for the four input OR-NOR gates).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	$-V_{EE}$	max.	7 V
Output current	I_O	max.	50 mA
Storage temperature	T_{stg}		−65 to +150 °C

D.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 0$ V (ground) $-V_{EE} = 4{,}5$ V ± 5%; $R_L = 50\ \Omega$ to −2 V.
$T_j = 30$ to 125 °C.

parameter	symbol			unit	remarks
Output voltage HIGH	V_{OH}	typ.	−955	mV	$V_{IHA} = -0{,}88$ V
	V_{OHA}		−880	mV	
	V_{OHB}		−1025	mV	
Output voltage LOW	V_{OL}	typ.	−1705	mV	$V_{ILB} = -1{,}81$ V
	V_{OLA}		−1620	mV	
	V_{OLB}		−1820	mV	
Output threshold voltage HIGH	V_{OHC}		−1035	mV	with 30% noise margin; $V_{IHB} = -1{,}165$ V
Output threshold voltage LOW	V_{OLC}		−1610	mV	$V_{ILA} = -1{,}475$ V
Input voltage HIGH	V_{IH}	max.	−550	mV	to avoid saturation
Input current HIGH	I_{IHA}		265	μA	
Input current LOW	I_{ILB}		0,5	μA	
Supply current	I_{EE}	min.	210	mA	
		typ.	307	mA	
		max.	430	mA	

FAMILY DATA see Family Specifications.

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 0$ V (ground); $V_{EE} = -4{,}5$ V ± 5%; $R_L = 50\ \Omega$ to -2 V.
$T_j = 30$ to 125 °C.

parameter	symbol	min.	typ.	max.	unit	remarks
Rise/fall time	t_{TLH} t_{THL}	—	1	2	ns	input rise — or fall time = 0,7 ns
Propagation delay time						
$D_{pn} \longrightarrow Y_p$	t_{PLH}/t_{PHL}	2,3	—	5,4	ns	
$A_n \longrightarrow Y_p$		2,0	—	4,8	ns	
$D_n \longrightarrow Y_p$		4,10	—	9,65	ns	corresponding PS HIGH
$PS_n \longrightarrow Y_p$		2,4	—	5,6	ns	
$A_n \longrightarrow Y$		2,3	—	5,35	ns	
$D_n \longrightarrow Y$		1,8	—	4,2	ns	
$D_n \longrightarrow PC$		3,6	—	8,4	ns	
$D_{pn} \longrightarrow PC$		1,8	—	4,2	ns	
$PS_n \longrightarrow PC$		1,7	—	3,9	ns	other PS inputs HIGH
$I_n \longrightarrow Q$		1,25	—	3,1	ns	
$I_n \longrightarrow \overline{Q}$		1,25	—	3,1	ns	

Notes

1. This device is compatible with the voltage and temperature compensated 100 K ECL.
2. Voltages are defined with respect to ground.
3. Unit is in a test socket or mounted on a printed circuit board with transverse air flow of 1000 LFPM.
4. The d.c. and a.c. limits apply after thermal equilibrium has been established.
5. The inputs can be left open (low level), but never connected to V_{CC} for high level.
6. The two V_{CC1} pins must be connected out of the package with a low impedance. Same for V_{CC2} and V_{EE} pins.

See also Chapters Definition of Symbols and Family Specifications.

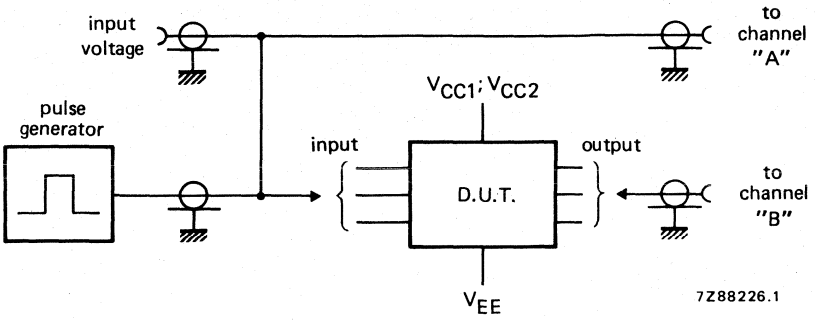


Fig. 3 Test circuit.

Cable impedance = input oscilloscope impedance = 50 Ω

Test condition input rise time = 0,7 ns

$V_{CC1} = V_{CC2} = +2$ V; $V_{EE} = -2,5$ V; input voltage HIGH = 1,045 V
LOW = 0,295 V

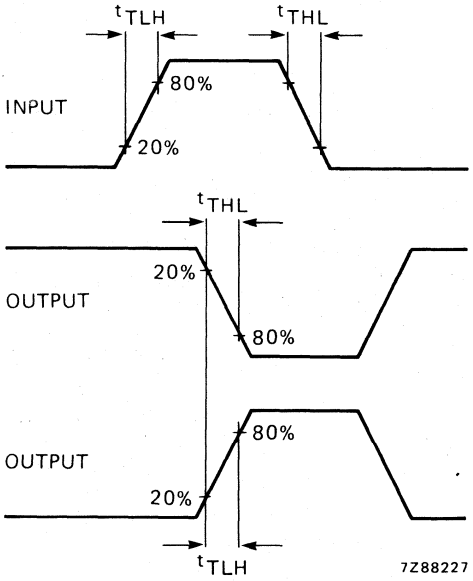


Fig. 4 Transition times (rise and fall times).

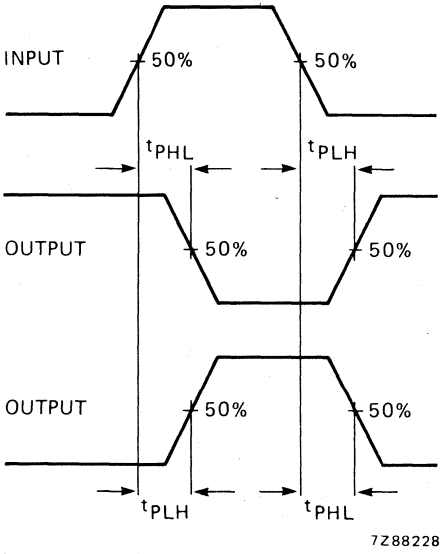


Fig. 5 Propagation delay times.

Pin connections

V_{CC1} = 24; 56	A_0 = 52	A_1 = 60	Y_p = 59	PC = 25
V_{CC2} = 22; 54				
V_{EE} = 26; 58				

I_0 = 63;	I_1 = 28;	I_2 = 19;	I_3 = 20;	Q = 49;	$\overline{Q}$ = 51

D_0^0 = 46	D_1^0 = 39	D_2^0 = 2	D_3^0 = 9	Y_0 = 55
D_0^1 = 47	D_1^1 = 38	D_2^1 = 1	D_3^1 = 11	Y_1 = 53
D_0^2 = 44	D_1^2 = 37	D_2^2 = 3	D_3^2 = 10	Y_2 = 29
D_0^3 = 45	D_1^3 = 36	D_2^3 = 4	D_3^3 = 13	Y_3 = 27
D_0^4 = 42	D_1^4 = 35	D_2^4 = 5	D_3^4 = 12	Y_4 = 61
D_0^5 = 43	D_1^5 = 33	D_2^5 = 6	D_3^5 = 15	Y_5 = 57
D_0^6 = 41	D_1^6 = 34	D_2^6 = 7	D_3^6 = 14	Y_6 = 23
D_0^7 = 40	D_1^7 = 32	D_2^7 = 8	D_3^7 = 16	Y_7 = 21
D_{p0} = 48	D_{p1} = 30	D_{p2} = 64	D_{p3} = 18	
PS_0 = 50	PS_1 = 31	PS_2 = 62	PS_3 = 17	

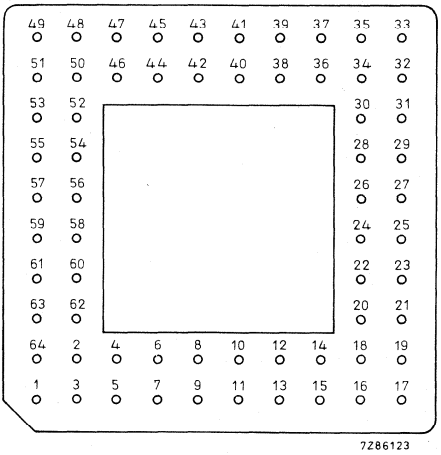


Fig. 6 Pin designations.

FOUR-BYTE COMPARATOR AND MULTIPLEXER

The HXA220-402 is a high-speed multiplexer that can multiplex four bytes of 8 bits, compare each of them with an external fifth byte, generate parity for the five bytes and check the parity for the input bytes. A function select input (F) can select on the output the results of parity checking or one of the four input bytes, selected by two select inputs (S_0 and S_1).

It is intended for:

- EDP — High-speed multiplex, data transfer
- Telecommunication — Digital transmission, digital multiplex, networks
- Data communication — Digital networks, high-speed multiplex
- Instrumentation — Signal processors
- Video — Digital video networks, high level multiplex.

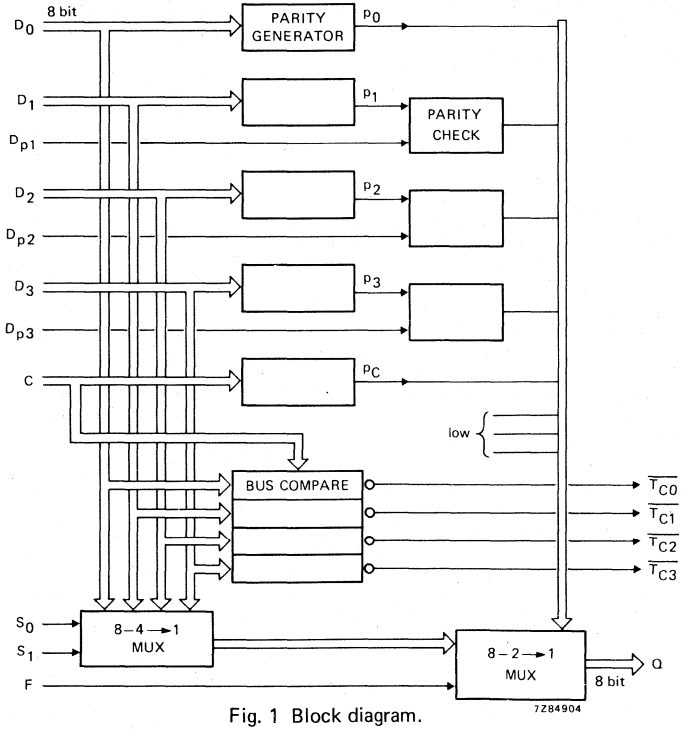


Fig. 1 Block diagram.

PACKAGE OUTLINE

64-pin plug-in package (FO-75).

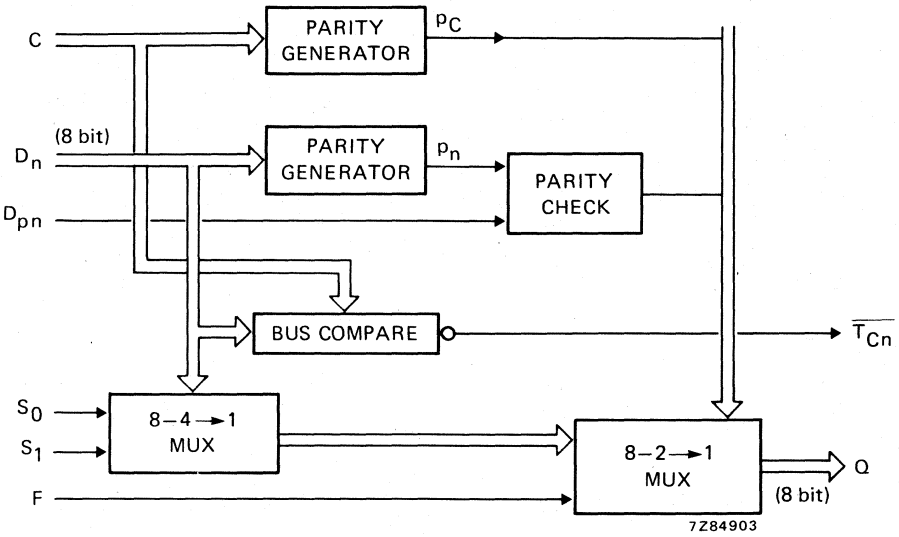


Fig. 2 Logic function.

Truth table

inputs			output
S_0	S_1	F	
L	L	L	D_0
H	L	L	D_1
L	H	L	D_2
H	H	L	D_3
X	X	H	$Q_0 = p_0$ $Q_n = p_n \oplus D_{pn}$ (n = 1 to 3) $Q_4 = p_C$ Q_n = L (n < 7; n > S)

Positive logic
H = HIGH state
(the more positive voltage) = 1
L = LOW state
(the less positive voltage) = 0
X = state is immaterial
⊕ = exclusive OR

$p_n = \oplus D_n^j$

$\overline{T_{Cn}} = \oplus (C_n \oplus D_n^j)$

p_n is the internally generated parity bit after D_n

p_C is the internally generated parity bit after C

n = 0 to 3

j = 0 to 7

RATINGS *

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (d.c.)	$-V_{EE}$	max.	7 V
Output current	I_O	max.	50 mA
Storage temperature	T_{stg}		−65 to +150 °C
Input voltage	V_i		0 to 4,75 V

D.C. CHARACTERISTICS *

$V_{CC1} = V_{CC2} = 0$ V (ground); $V_{EE} = -4{,}5$ V ± 5%; $R_L = 50\ \Omega$ to −2 V.
$T_j = 30$ to 125 °C.

parameter	symbol			unit	remarks
Output voltage HIGH	V_{OH}	typ.	−955	mV	$V_{IHA} = -0{,}88$ V
	V_{OHA}		−880	mV	
	V_{OHB}		−1025	mV	
Output voltage LOW	V_{OL}	typ.	−1705	mV	$V_{ILB} = -1{,}81$ V
	V_{OLA}		−1620	mV	
	V_{OLB}		−1810	mV	
Output threshold voltage HIGH**	V_{OHC}		−1035	mV	$V_{IHB} = -1{,}165$ V
Output threshold voltage LOW**	V_{OLC}		−1610	mV	$V_{ILA} = -1{,}475$ V
Input current HIGH	I_{IHA}		265	μA	
Input current LOW	I_{ILB}		0,5	μA	
Supply current	I_{EE}	min.	263	mA	
		typ.	368	mA	
		max.	515	mA	
Input voltage HIGH	V_{IH}	max.	−550	mV	to avoid saturation

DEVELOPMENT SAMPLE DATA

* See also **Family Specifications.**
** With 30% noise margin.

A.C. CHARACTERISTICS *

$V_{CC1} = V_{CC2} = 0$ V (ground); $V_{EE} = -4{,}5$ V ± 5 %; $R_L = 50\ \Omega$ to -2 V.
$T_j = 30$ to 125 °C.

parameter	symbol	min.	typ.	max.	unit	remarks
Rise time	t_{TLH}	–	1	2	ns	input rise time 0,7 ns
Fall time	t_{THL}	–	1	2	ns	input fall time 0,7 ns
Propagation delay time *through parity*	t_{PLH}/t_{PHL}					
C, $D_0 \rightarrow Q$		3,2	–	7,3	ns	F = HIGH
$D_1, D_2, D_3 \rightarrow Q$		3,8	–	8,5	ns	F = HIGH
$D_{pn} \rightarrow Q$		2,0	–	4,65	ns	F = HIGH
through multiplex	t_{PLH}/t_{PHL}					
$D_n \rightarrow Q$		2,3	–	5,45	ns	F = LOW
$S_0 \rightarrow Q$		2,9	–	6,10	ns	F = LOW
$S_1 \rightarrow Q$		3,1	–	6,55	ns	F = LOW
F $\rightarrow Q$		2,0	–	4,80	ns	F = LOW
C $\rightarrow \overline{T_{Cn}}$		2,0	–	4,10	ns	F = LOW
D $\rightarrow \overline{T_{Cn}}$		2,0	–	4,60	ns	F = LOW

Notes

1. This device is compatible with the voltage and temperature compensated 100 K ECL.
2. Voltages are defined with respect to ground.
3. Unit is in a test socket or mounted on a printed circuit board with transverse air flow of 1000 LFPM.
4. The DC and AC limits apply after thermal equilibrium has been established.
5. The inputs can be left open (low level), but never connected to V_{CC} for high level.
6. The two V_{CC1} pins must be connected out of the package with a low impedance. Same for V_{CC2} and V_{EE} pins.

* See also Family Specifications and Definition of Symbols.

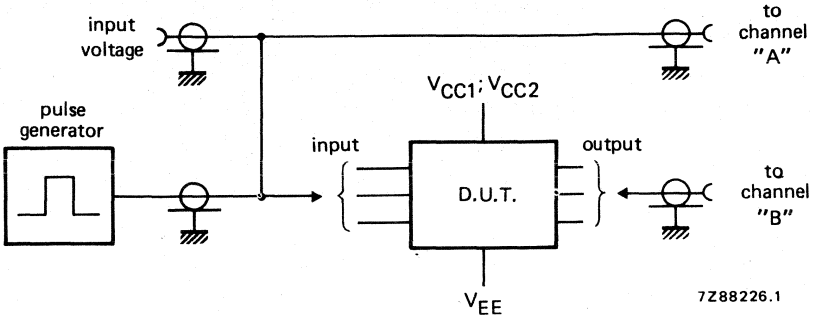


Fig. 3 Test circuit.

Cable impedance = input oscilloscope impedance = 50 Ω.
Test condition input rise time = 0,7 ns.
Input voltage HIGH = 1,045 V; LOW = 0,295 V; $V_{CC1} = V_{CC2} = +2$ V; $V_{EE} = -2,5$ V.

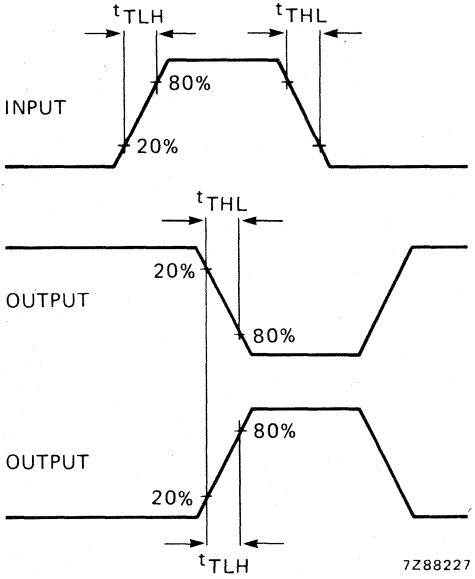


Fig. 4 Transition times (rise and fall times).

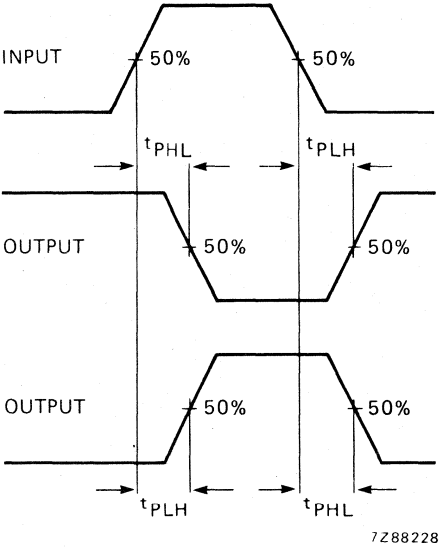


Fig. 5 Propagation delay times.

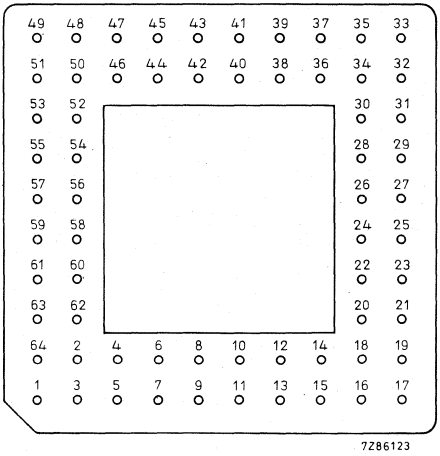


Fig. 6 Pin designation.

V_{CC1} = 24; 56 F = 29 S_0 = 19; S_1 = 18.
V_{CC2} = 22; 54
V_{EE} = 26; 58

bit (j)*	D_0	D_1	D_2	D_3	C	Q	$\overline{T_C}$	D_p
0	40	41	46	45	51	55	32	–
1	43	42	44	47	50	53	48	60
2	5	6	3	2	63	59	64	49
3	8	7	4	1	62	57	16	52
4	35	33	38	36	31	27		
5	34	30	37	39	28	25		
6	12	15	10	13	20	23		
7	14	17	11	9	61	21		

* For $\overline{T_C}$ and D_p byte 0 to 3.

HIGH LEVEL CONNECTION MATRIX 16 → 8

A very high speed device capable of interconnecting eight of the sixteen input lines with the 8 output lines. Both input and output lines ECL100 000 compatible. Once connected, the transmission rate from input to output is over 300 Mbit/s. The connection is made via a multiplexer for each output; the multiplexer address being latched internally.

Two clock inputs and two output enable lines allow the matrix to be extended.

It is intended for:

- EDP — high speed, high complexity multiplex multiprocessing systems
- Telecommunications — digital transmission; digital networks wideband automatic branch exchange
- Data communication — digital networks; high level multiplex
- Instrumentation — signal processing; fast channel switching
- Video — digital video networks; wideband multiplexing.

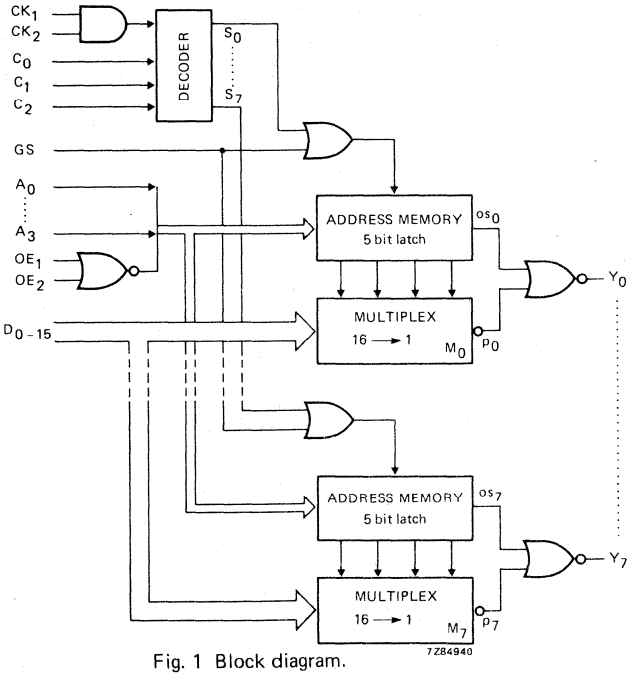


Fig. 1 Block diagram.

PACKAGE OUTLINE

64-pin plug-in package (FO-75).

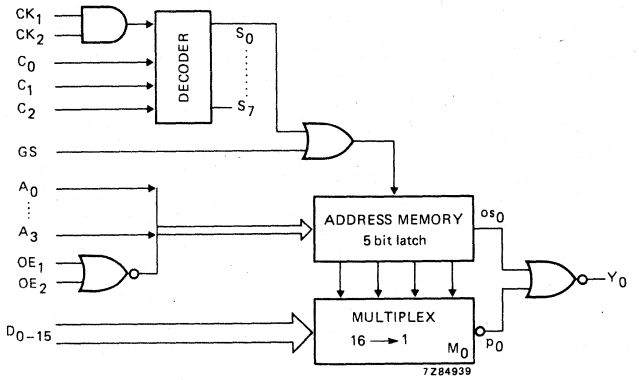


Fig. 2 Block diagram (one multiplexer).

Logic function
positive logic

H = HIGH state
more positive voltage = 1

L = LOW state
more negative voltage = 0

X = state is immaterial

$^+$ = next state

$^-$ = previous state

$\backslash$ = trailing edge

* = address while latching

The trailing edge latches the previous address A_0^*; A_1^*; A_2^* and A_3^* that interconnect the selected input D_n to p_n till next pulse.

$OE = \overline{OE_1 + OE_2}$

$Y_n = \overline{p_n + OS_n}$

input (S_n + GS)	output OS_n^+
L	OS_n^-
H	OE

Function table

S_n + GS	inputs A_0	A_1	A_2	A_3	internal output p_n^+
L	X	X	X	X	p_n^-
H	L	L	L	L	D_0
H	H	L	L	L	D_1
H	L	H	L	L	D_2
H	H	H	L	L	D_3
H	L	L	H	L	D_4
H	H	L	H	L	D_5
H	L	H	H	L	D_6
H	H	H	H	L	D_7
H	L	L	L	H	D_8
H	H	L	L	H	D_9
H	L	H	L	H	D_{10}
H	L		H	H	D_{11}
H	H	L	H	H	D_{12}
H	H	H	L	H	D_{13}
H	L	H	H	H	D_{14}
H	H	H	H	H	D_{15}
$\backslash$	A_0^*	A_1^*	A_2^*	A_3^*	D_n

Decoder

inputs				outputs							
$(CK_1 \cdot CK_2)$	C_0	C_1	C_2	S_0	S_1	S_2	S_3	S_4	S_5	S_6	S_7
L	X	X	X	L	L	L	L	L	L	L	L
H	L	L	L	H	L	L	L	L	L	L	L
H	H	L	L	L	H	L	L	L	L	L	L
H	L	H	L	L	L	H	L	L	L	L	L
H	H	H	L	L	L	L	H	L	L	L	L
H	L	L	H	L	L	L	L	H	L	L	L
H	H	L	H	L	L	L	L	L	H	L	L
H	L	H	H	L	L	L	L	L	L	H	L
H	H	H	H	L	L	L	L	L	L	L	H

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (d.c.)	V_{EE}	max. −7	V
Input voltage	V_i	0,5 V to V_{EE}	
Output current	I_O	max. 50	mA
Storage temperature	T_{stg}	−55 to + 150	°C

THERMAL RESISTANCE

With air flow of 0,5 m/s from junction to ambient			
with heatsink	$R_{th\ j\text{-}a}$	13	K/W
without heatsink	$R_{th\ j\text{-}a}$	25	K/W
Without forced air flow from junction to ambient			
with heatsink	$R_{th\ j\text{-}a}$	25	K/W
without heatsink	$R_{th\ j\text{-}a}$	50	K/W

D.C. CHARACTERISTICS*

V_{CC} = 0 V (ground); V_{EE} = −4,5 V ± 5%; R_L = 50 Ω to −2 V; T_j = 30 to 125 °C

parameter	symbol		unit		remarks
Output voltage HIGH	V_{OH}	typ.	− 955	mV	V_{IHA} = −0,88 V
	V_{OHA}		− 880	mV	
	V_{OHB}		−1025	mV	
Output voltage LOW	V_{OL}	typ.	−1705	mV	V_{ILB} = −1,81 V
	V_{OLA}		−1620	mV	
	V_{OLB}		−1810	mV	

* See Family Specifications and Definition of Symbols.

parameter	symbol			unit	remarks
Output threshold voltage HIGH	V_{OHC}		−1035	mV	with 30% noise margin; V_{IHB} = −1,165 V; V_{ILA} = −1,475 V
Output threshold voltage LOW	V_{OLC}		−1610	mV	
Input voltage HIGH	V_{IHA}		− 550	mV	to avoid saturation
Input current HIGH	I_{IHA}		265	μA	
Input current LOW	I_{ILB}		0,5	μA	
Supply current	I_{EE}	min.	340	mA	
		typ.	480	mA	
		max.	670	mA	

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 0$ V (ground); $V_{EE} = -4{,}5$ V ± 5%; $R_L = 50\ \Omega$ to −2 V; $T_j = 30$ to 125 °C.

parameter	symbol	min.	typ.	max.	unit	remarks
Output rise time	t_{TLH}	–	0,75	2,0	ns	input rise and fall time = 0,7 ns
Output fall time	t_{THL}	–	0,75	2,0	ns	
Propagation delay times	t_{PHL} / t_{PLH}					
D → Y		4,0	–	10	ns	output enabled
A → Y		3,5	–	12	ns	transparent latch
C → Y		4,0	–	10	ns	to inhibit output $OE_1 + OE_2$ = LOW
CK → Y		4,0	–	10	ns	
GS → Y		3,5	–	9	ns	
C → Y		6,0	–	15	ns	$OE_1 + OE_2$ = HIGH
CK → Y		6,0	–	15	ns	
GS → Y		6,0	–	15	ns	
OE → Y		3,0	–	7,0	ns	transparent latch
Clock pulse duration						
HIGH	t_{CKH}	3,0	–	–	ns	see Fig. 5
LOW	t_{CKL}	1,5	–	–	ns	
GS pulse duration						
HIGH	t_{GSH}	3,0	–	–	ns	
LOW	t_{GSL}	1,5	–	–	ns	

parameter	symbol	min.	typ.	max.	unit	remarks
Pulse duration						
C	t_C	3,5	–	–	ns	See Fig. 5
A	t_A	3,5	–	–	ns	
OE	t_{OE}	3,5	–	–	ns	
Set-up time						
C → CK	t_{CKSC}	–	1,0	–	ns	
A → CK	t_{CKSA}	–	3,3	–	ns	
OE → CK	t_{CKSOE}	–	3,3	–	ns	
A → GS	t_{GSSA}	–	2,8	–	ns	
OE → GS	t_{GSSOE}	–	2,9	–	ns	
Hold time						
CK → C	t_{CKHC}	–	1,5	–	ns	
CK → A	t_{CKHA}	–	1,8	–	ns	
CK → OE	t_{CKHOE}	–	1,7	–	ns	
GS → A	t_{GSHA}	–	2,9	–	ns	
GS → OE	t_{GSHOE}	–	2,9	–	ns	

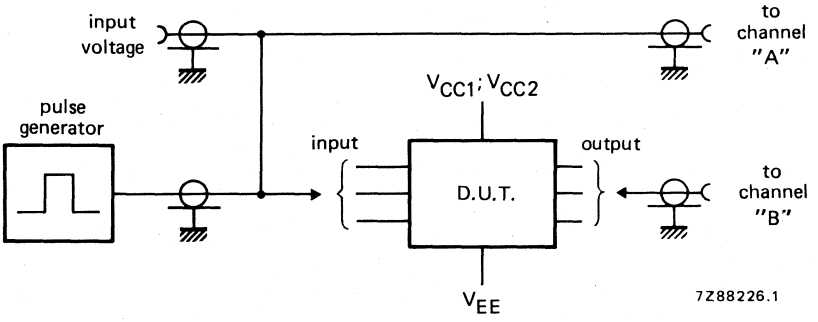


Fig. 3 Switching times test circuit.

Input and output cables are 50 Ω coaxial.
The input impedance of the oscilloscope is 50 Ω.
$V_{CC1} = V_{CC2} = +2$ V; $V_{EE} = -2,5$ V.

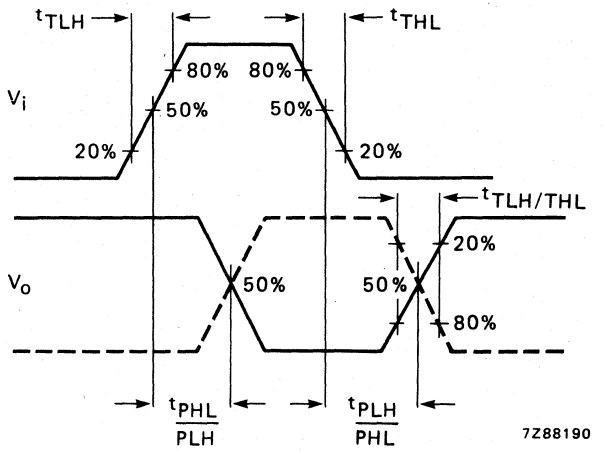


Fig. 4 Switching times waveform.

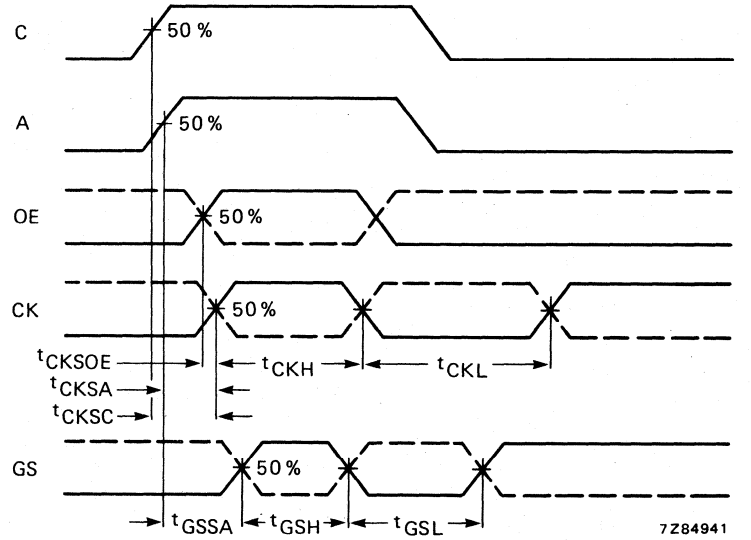


Fig. 5 Set-up and hold times waveform.

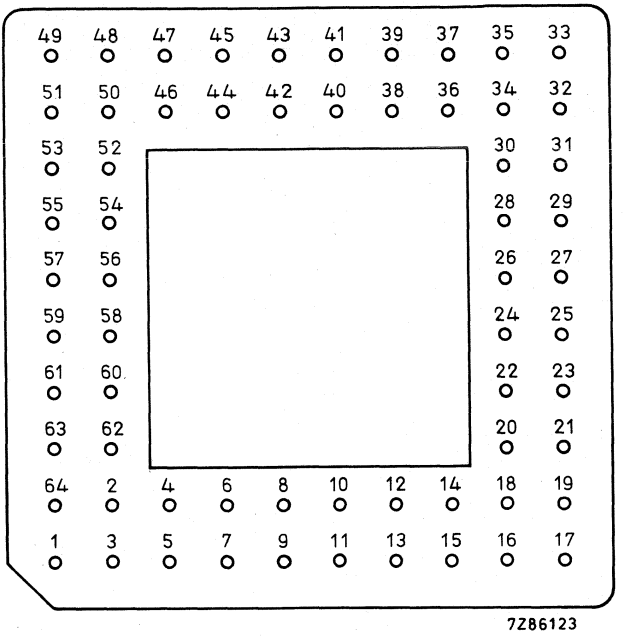


Fig. 6 Pin designation.

V_{CC1} = 56, 24	CK_1 = 7	C_0 = 60	A_0 = 39	OE_1 = 33
V_{CC2} = 54, 22	CK_2 = 8	C_1 = 17	A_1 = 40	OE_2 = 34
V_{EE} = 58, 26	GS = 42	C_2 = 9	A_2 = 41	
			A_3 = 43	

D_0 = 12	D_5 = 1	D_{10} = 36	Y_0 = 18	Y_4 = 50
D_1 = 14	D_6 = 4	D_{11} = 35	Y_1 = 23	Y_5 = 53
D_2 = 10	D_7 = 6	D_{12} = 45	Y_2 = 27	Y_6 = 57
D_3 = 11	D_8 = 37	D_{13} = 44	Y_3 = 30	Y_7 = 62
D_4 = 2	D_9 = 38	D_{14} = 47		
		D_{15} = 46		

Not connected: 3, 5, 13, 15, 16, 19, 20, 21, 25, 28, 29, 31, 32, 48, 49, 51, 52, 55, 59, 61, 63, 64.

APPLICATION INFORMATION

The circuit shows a HIGH level digital automatic branch exchange module, that can interconnect 64 lines into 32. The transmission speed through the module is over 200 MHz and the switching can be controlled by an external processor.

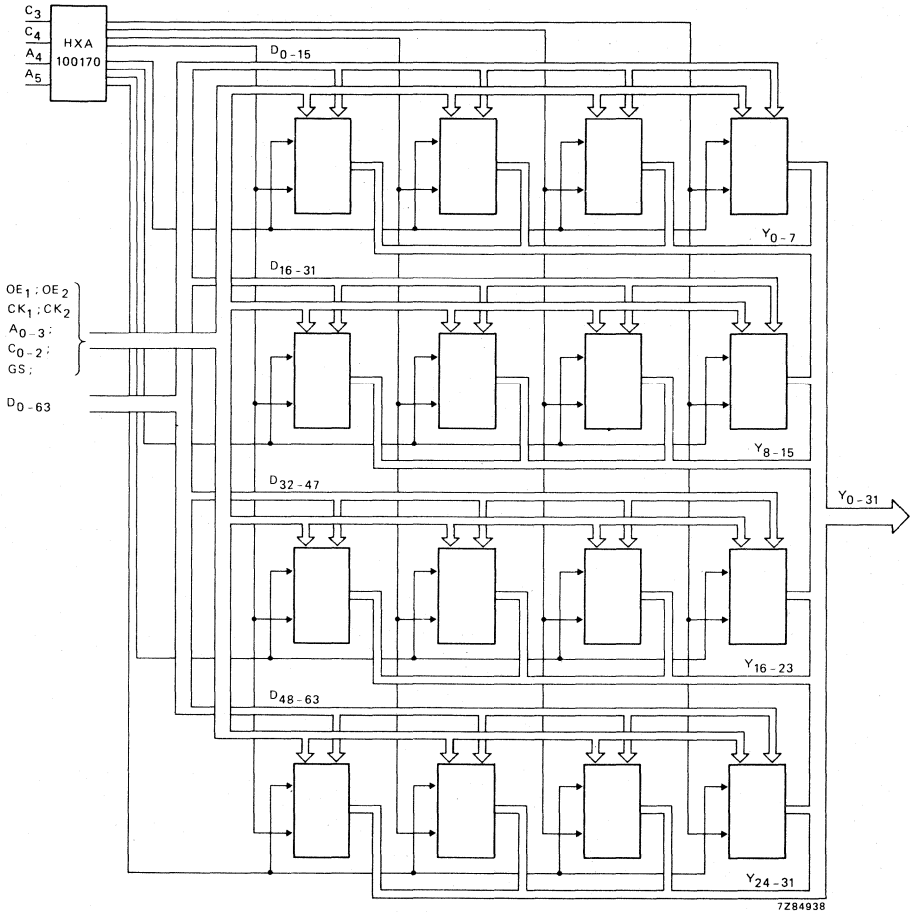


Fig. 7 Layout with 16 devices HXA230-101.

DEVICE DATA

Dedicated designs

125 MHz AMPLIFIER AND DIVIDER-BY-32/33

The silicon monolithic integrated circuit SAA1059 is designed as a programmable-ratio divide-by-32/33 prescaler. It is intended for use in digital radio tuning systems and frequency counters in radio applications with an input frequency range from 0,5 to 125 MHz. The high-frequency inputs are differential inputs of a preamplifier for handling a.m. as well as f.m. oscillator signals. One output set provides complementary ECL levels by emitter followers and a second output buffer set is intended to drive MOS circuits by open collectors.

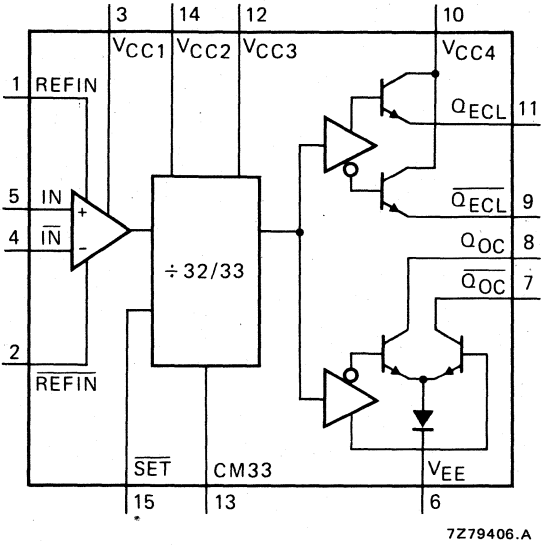


Fig. 1 Block diagram.

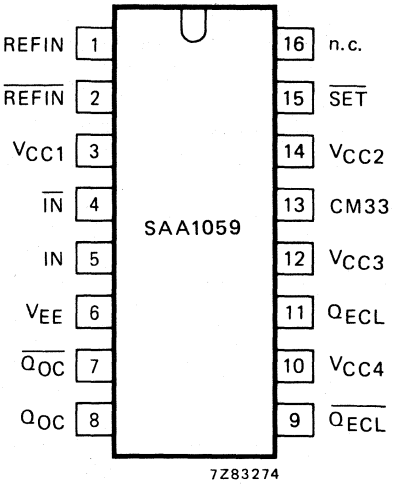


Fig. 2 Pin diagram.
V_{CC2} = 5 V (see Fig. 6)
V_{EE} = 0 V (ground)
Pin 16 preferably connected to V_{EE}

QUICK REFERENCE DATA

Supply voltage	V_B	max.	14	V
	V_{CC2}	typ.	5 ± 10%	V
Input frequency range	f_i		0,5 to 125	MHz
Input voltage range				
f = 0,5 to 30 MHz	$V_{i(rms)}$		5 to 100	mV
f = 30 to 125 MHz	$V_{i(rms)}$		10 to 100	mV
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	typ.	760	mW

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

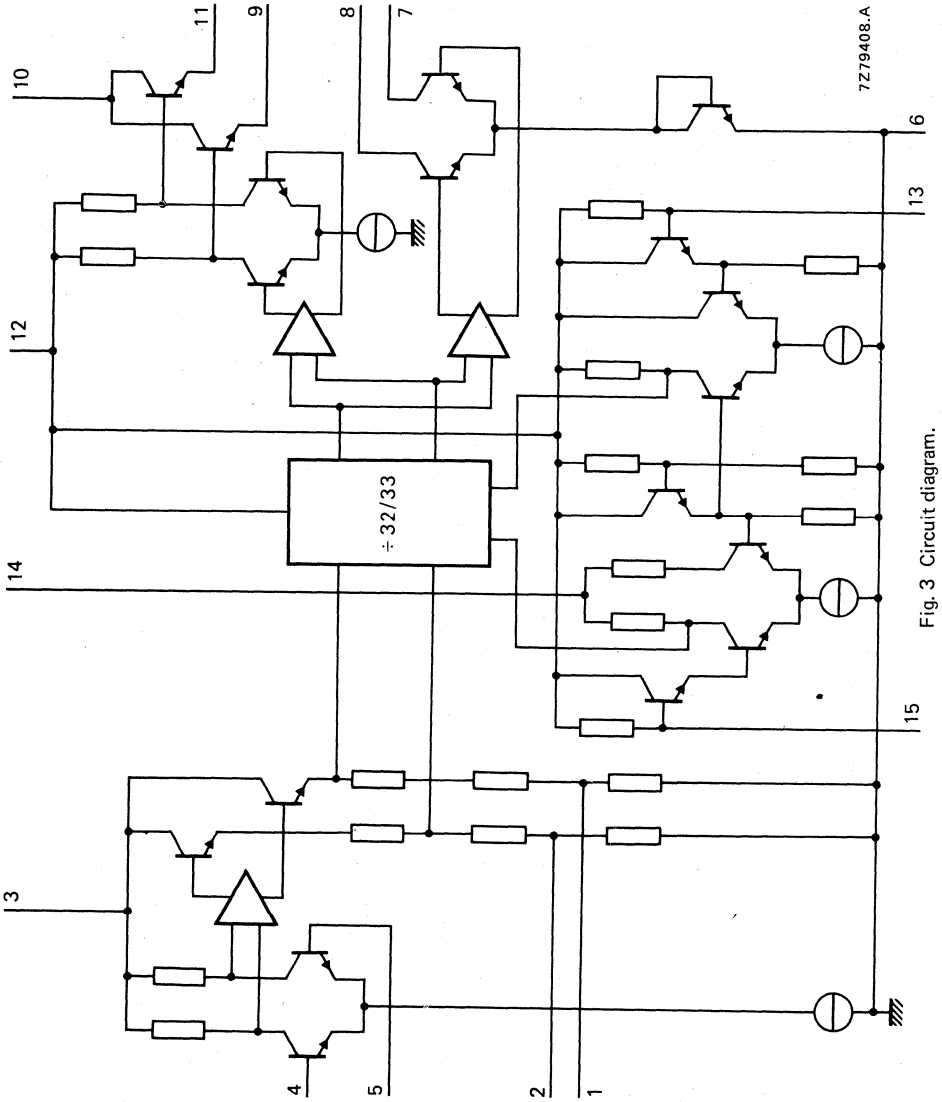
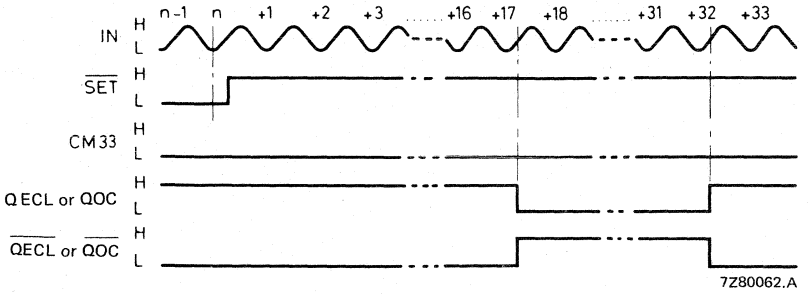
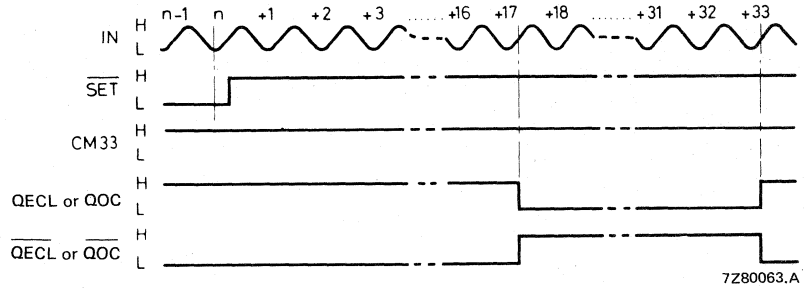


Fig. 3 Circuit diagram.





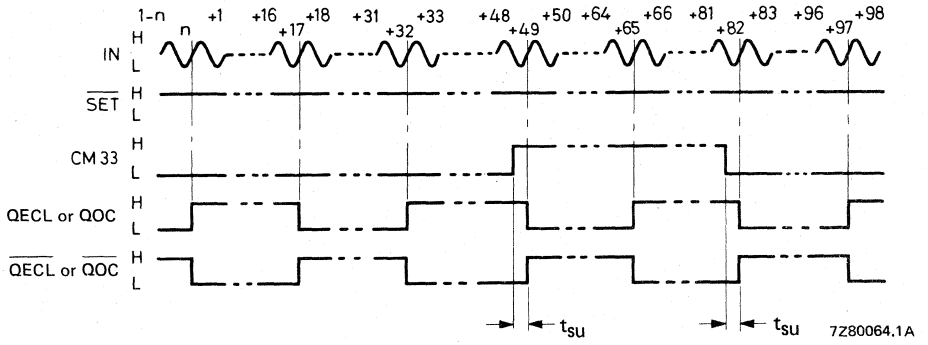


Fig. 4 Timing diagrams of programmable frequency dividing.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{CC2}	max.	7 V
Output supply voltage (pins 7 and 8, R_L = 470 Ω)	V_B	max.	14 V
Input voltage	V_I	0 to V_{CC}	
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	760 mW
Storage temperature	T_{stg}	−25 to + 125	°C
Operating ambient temperature	T_{amb}	−20 to + 80	°C

CHARACTERISTICS

V_{EE} = 0 V; V_{CC} = 5 V; V_B = 9 V; T_{amb} = 25 °C, unless otherwise specified.

Supply current ($I_3 + I_{10} + I_{12} + I_{14}$)*	I_{CC}	typ.	110 mA
		<	135 mA
Count input voltage*			
A.M. (0,5 MHz to 30 MHz) pin 5	$V_{i(rms)}$	5 to 100	mV
F.M. (30 MHz to 125 MHz) pin 4	$V_{i(rms)}$	10 to 100	mV
A.C. input impedance at 1 MHz	Z_4, Z_5	>	1 kΩ
Count mode input (pin 13)			
input voltage for division-ratio 32	V_{CML}	<	2 V
input voltage for division-ratio 33	V_{CMH}	>	3 V
input impedance	Z_{13}	1 to 1,5	kΩ
Set-up time changing the division-ratio from 32 to 33 or vice versa	t_{su}	typ.	50 ns
Reset (pin 15)			
input voltage reset	V_{RL}	<	2 V
input voltage no reset	V_{RH}	>	3 V
input impedance	Z_{15}	1,7 to 2,6	kΩ
Emitter follower outputs (pins 9 and 11)			
output voltage; R_L = 4,7 kΩ to ground	V_{OH}	>	3,7 V
	V_{OL}	<	3,3 V
Open collector outputs (pins 7 and 8)			
V_B = 11 V; R_L = 470 Ω; $I_B \leqslant$ 20 mA			
Output voltage HIGH	V_{OH}	>	9 V
Output voltage LOW	V_{OL}	<	2 V

* See Fig. 6.

CHARACTERISTICS (continued)

Open collector outputs (pins 7 and 8)
transition times, no capacitive load

t_{TLH}	typ.	15 ns
t_{THL}	typ.	12 ns

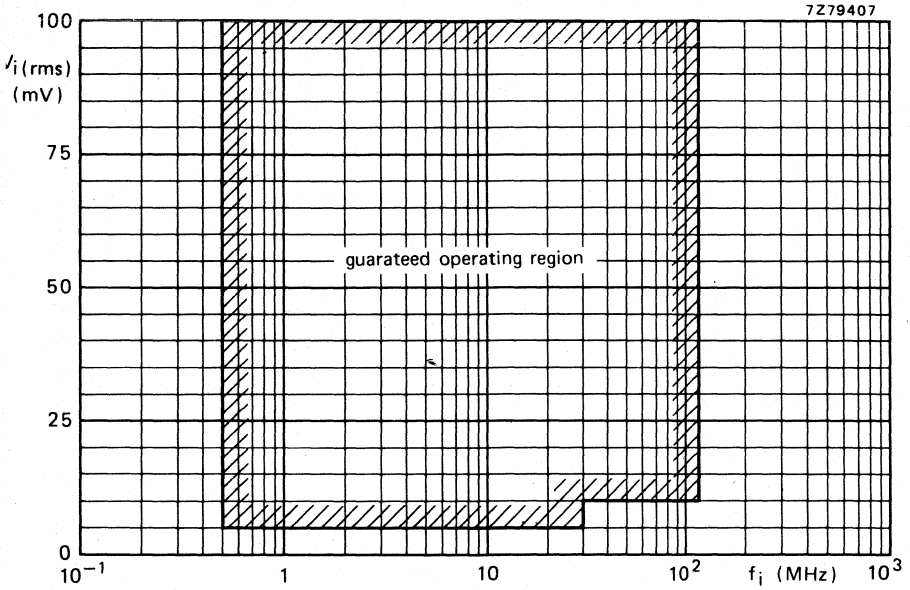


Fig. 5 Triggering level requirements.

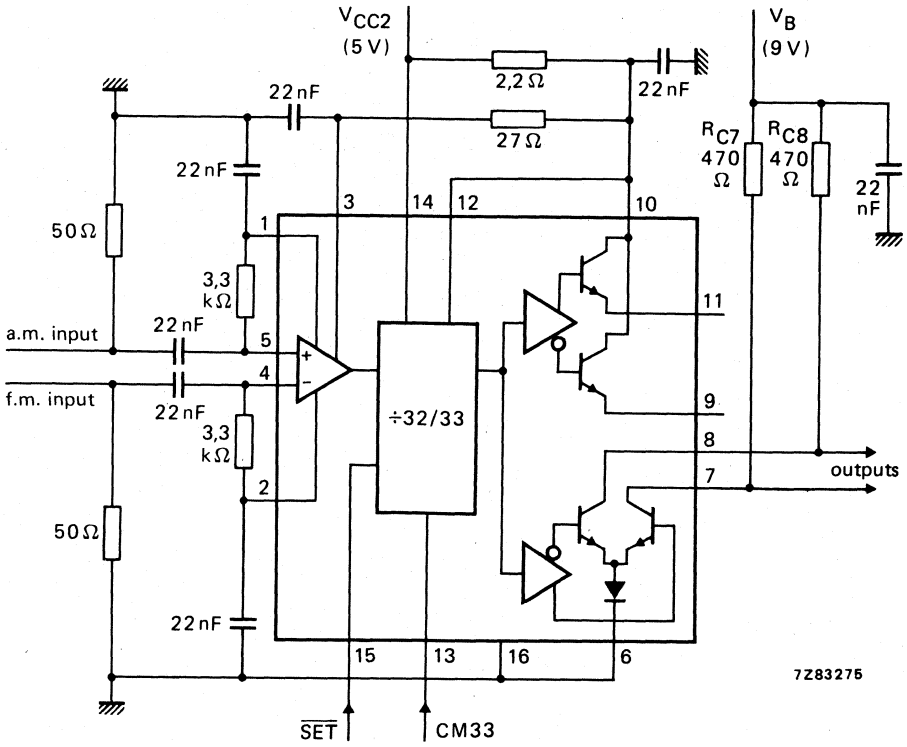


Fig. 6 Test circuit.

APPLICATION INFORMATION

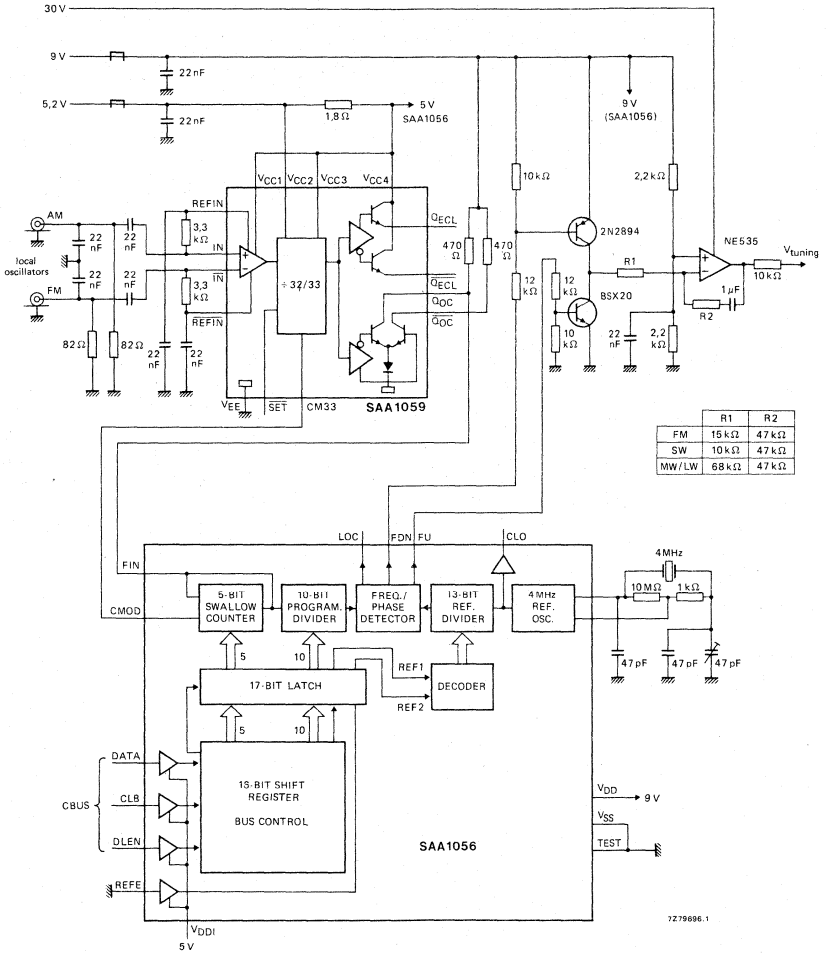
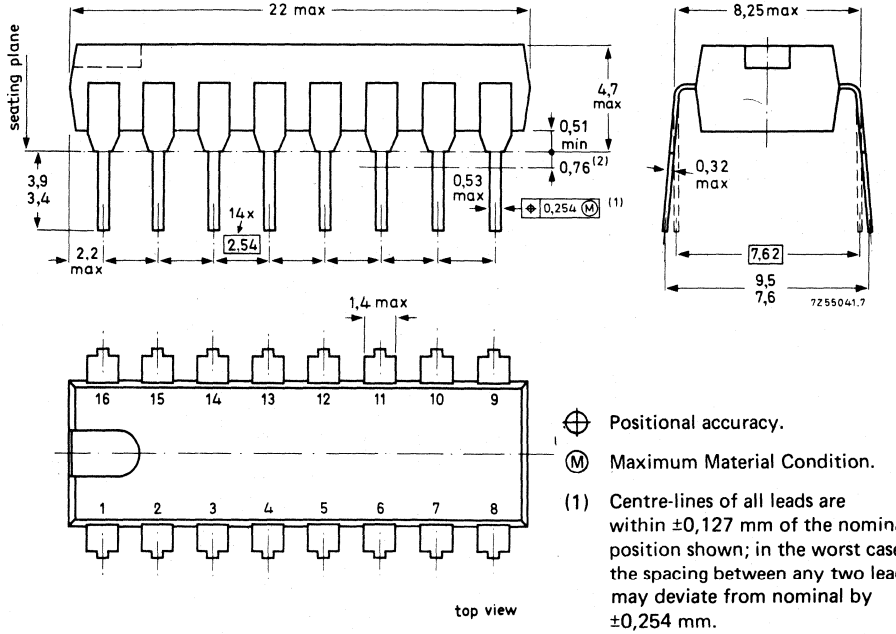


Fig. 7 A practical digital frequency synthesizer.

16-LEAD DUAL IN-LINE; PLASTIC (SOT-38)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

SENSITIVE 950 MHz DIVIDER-BY-256

This silicon monolithic integrated circuit is a prescaler in current-mode logic. It contains an amplifier, a divide-by-256 scaler and an output stage. It has been designed to be driven by a sinusoidal signal from the local oscillator of a television tuner, with frequencies from 70 to 350 or 500 to 950 MHz, for a supply voltage of 5 V ± 5% and an ambient temperature of 0 to 70 °C.

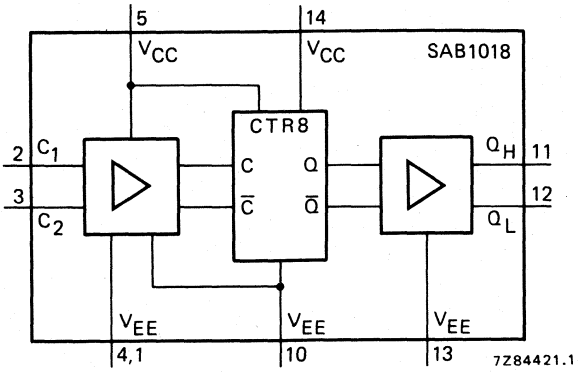


Fig. 1 Block diagram. CTR8 = 8 binary dividers = (÷ 256).

QUICK REFERENCE DATA

Supply voltage	V_{CC}	5 ± 5%	V
Input frequency range (pins 2 and 3)	f_i	70 to 350	MHz
		and 500 to 950	MHz
Input voltage	$V_{i(rms)}$ min.	10	mV
Output voltage swing	$V_{o(p-p)}$ typ.	1	V
Output current LOW	I_{OL} typ.	2,4	mA
Power consumption per package (no load)	P_{av} typ.	300	mW
Operating ambient temperature	T_{amb}	0 to +70	°C

PACKAGE OUTLINE

SAB1018P: 14-lead DIL; plastic (SOT-27S, T, V).

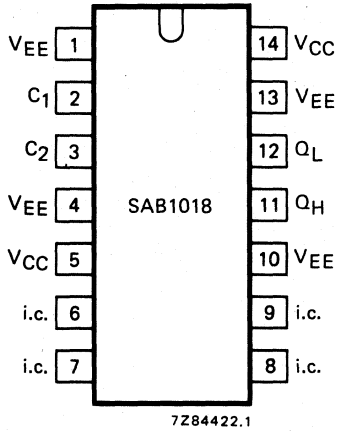


Fig. 2 Pinning diagram.

PINNING

V_{CC}	positive supply
V_{EE}	0 V; ground
C_1, C_2	differential inputs
Q_H, Q_L	complementary outputs
i.c.	internally connected

FUNCTIONAL DESCRIPTION

The circuit contains an amplifier, a divide-by-256 scaler and an output stage. It has been designed to be driven by a sinusoidal signal from the local oscillator of a TV tuner, with frequencies from 70 to 350 or 500 to 950 MHz, for a supply voltage of 5 V ± 5% and an ambient temperature of 0 to 70 °C.

The inputs are differential and are internally biased to permit capacitive coupling. For asymmetrical drive the unused input should be connected to ground via a 56 Ω resistor and a capacitor, to give approximately equal impedances at the two inputs of the amplifier.

The first divider stage will oscillate in the absence of an input signal; an input signal within the specified range will suppress this oscillation.

The outputs are complementary open-collector current sources. The output current edges are slowed down internally to reduce the harmonic contents of the signal. The external load and the supply voltage to which it is connected determine the output voltage.

There are three limitations to this output voltage and consequently to the load and to the supply voltage to which it is connected. Firstly it should not be possible under any circumstances that the output voltage becomes lower than 1,6 V below V_{CC}, to avoid saturation of the output transistor. Further it should not be possible that the output voltage becomes higher than 10 V, to avoid breakdown of the output transistor. Finally the output voltage swing should not be much larger than 1 V peak to peak, to keep the capacitive feedback to the inputs of the circuit small.

Wide, low-impedance ground connections and a short capacitive bypass from the V_{CC} pins to ground are recommended.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (d.c.)	V_{CC}	max.	7	V
Input voltage	V_i	0 to V_{CC}		V
Output voltage	V_o	max.	10	V
Storage temperature	T_{stg}	−55 to +125		°C
Junction temperature	T_j	max.	125	°C

D.C. CHARACTERISTICS

V_{EE} = 0 V (ground); V_{CC} = 5 V; T_{amb} = 25 °C unless otherwise specified.

The circuit has been designed to meet the d.c. specifications as shown below, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed-circuit board.

Output voltage				
HIGH level	V_{OH}	max.	10	V
LOW level	V_{OL}	min.	V_{CC}−1,6	V
Output current				
at $V_{OL} = V_{CC} - 1{,}6$ V	I_{OL}	min.	2	mA
at $V_{OL} = V_{CC}$	I_{OL}	max.	2,8	mA
Supply current	I_{CC}	typ.	60	mA
		max.	75	mA

A.C. CHARACTERISTICS

V_{EE} = 0 V (ground); V_{CC} = 5 V ± 5%; T_{amb} = 0 to +70 °C.

Input voltage (see Fig. 3)				
f_i = 70, 350, 500 and 950 MHz	$V_{i(rms)}$		10 to 150	mV
Output rise time *	t_{TLH}	<	140	ns
Output fall time *	t_{THL}	<	140	ns

* Between 10% and 90% of observed waveform; R_L = 510 Ω; C_L = 60 pF.

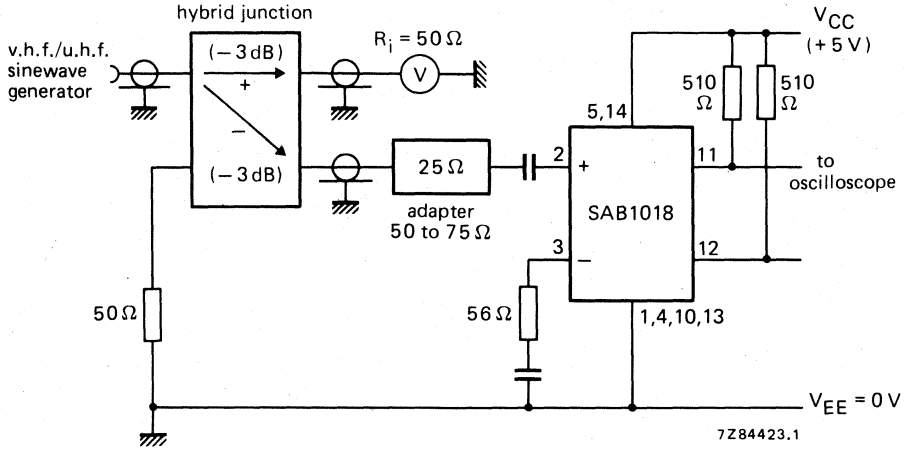


Fig. 3 Test circuit for defining input voltage.

- Cables must be 50 Ω coaxial.
- The capacitors are leadless ceramic (multilayer capacitors) of 10 nF.
- All connections to the device and to the meter must be kept short and of approximately equal lengths.
- Hybrid junction is ANZAC H-183-4 or similar.

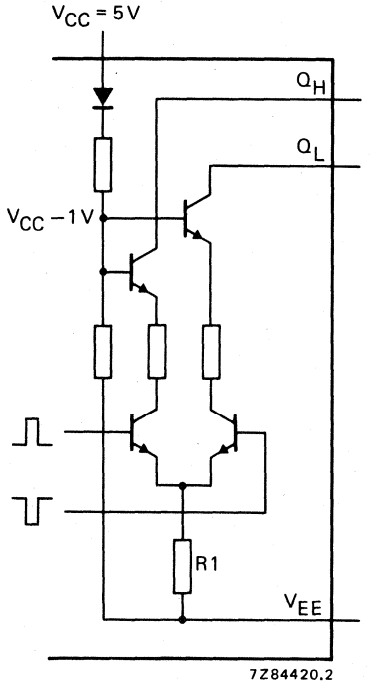


Fig. 4 Output stage.
Q_H = pin 11
Q_L = pin 12
V_{EE} = pin 13
V_{CC} = pin 14
R1 = 600 Ω

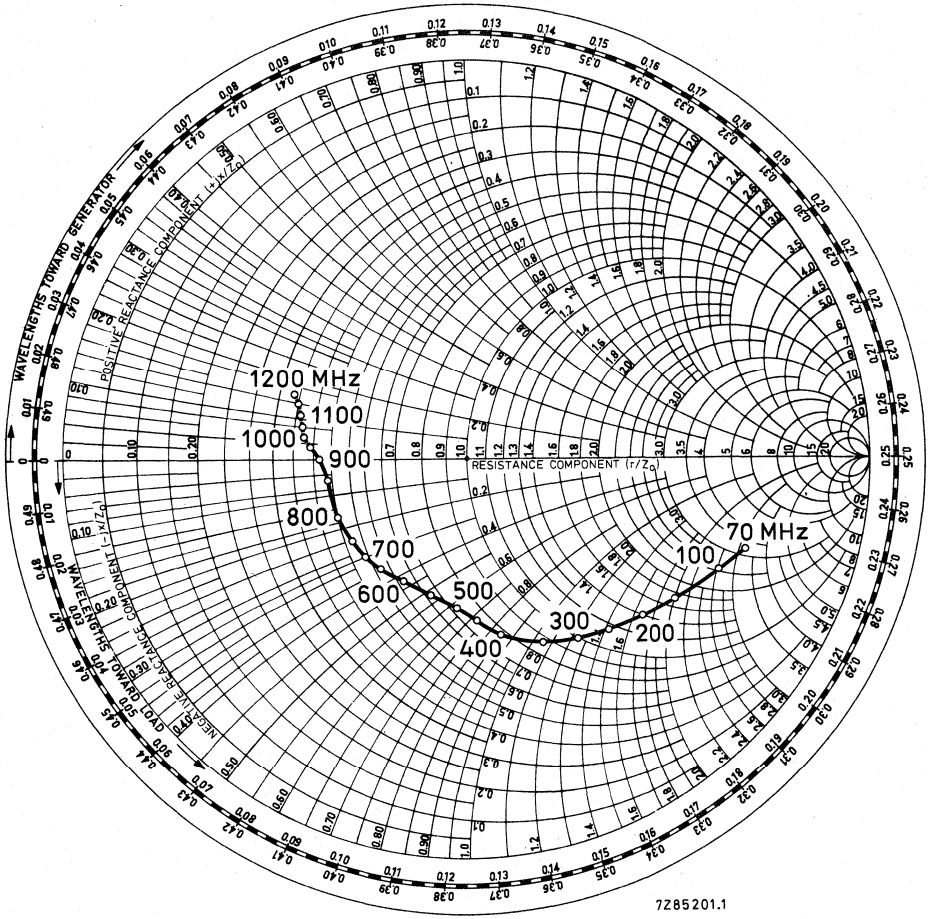


Fig. 5 Smith chart of typical input impedance.
$V_{i(rms)}$ = 25 mV; V_{CC} = 5 V; reference value = 75 Ω.

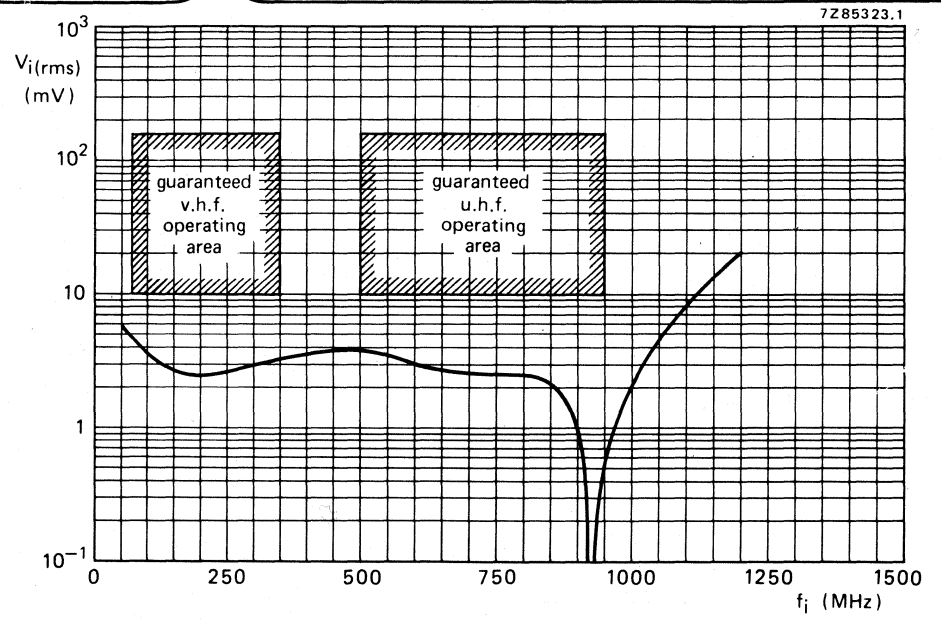


Fig. 6 Typical sensitivity curve under nominal conditions.

APPLICATION INFORMATION

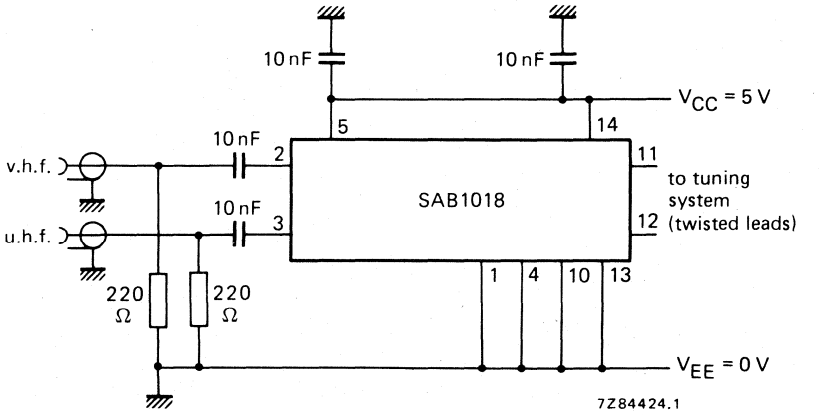
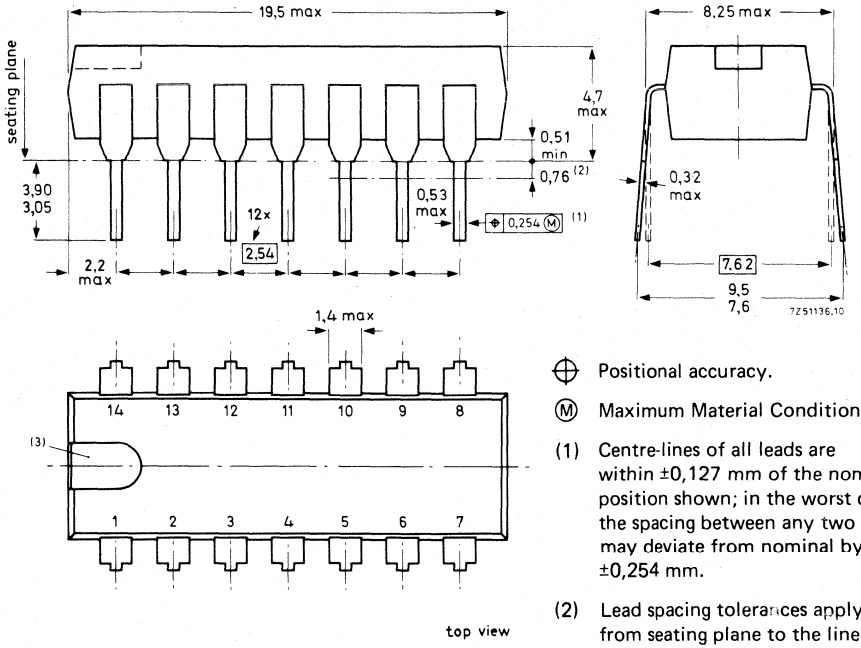


Fig. 7 Circuit diagram.

Application in a television tuning system. The output peak-to-peak voltage is about 1 V. For tuning circuits requiring a higher input voltage a transistor stage will be needed.

14-LEAD DUAL IN-LINE; PLASTIC (SOT-27S, T, V)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

SENSITIVE 950 MHz DIVIDER-BY-256

This silicon monolithic integrated circuit is a prescaler in current-mode logic. It contains an amplifier, a divide-by-256 scaler and an output stage. It has been designed to be driven by a sinusoidal signal from the local oscillator of a television tuner, with frequencies from 70 to 350 or 500 to 950 MHz, for a supply voltage of 5 V ± 5% and an ambient temperature of 0 to 70 °C.

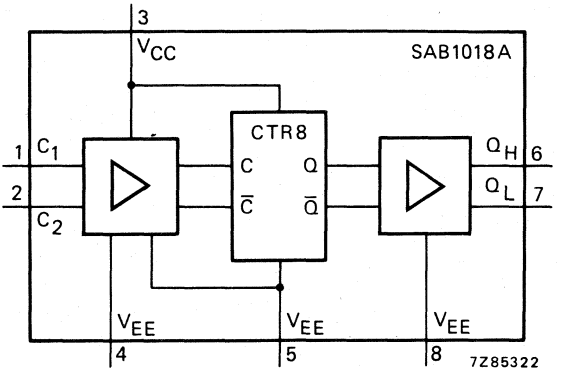


Fig. 1 Block diagram. CTR8 = 8 binary dividers = (÷ 256).

QUICK REFERENCE DATA

Supply voltage	V_{CC}		5 ± 5% V
Input frequency range (pins 1 and 2)	f_i		70 to 350 MHz
			and 500 to 950 MHz
Input voltage	$V_{i(rms)}$	min.	10 mV
Output voltage swing	$V_{o(p-p)}$	typ.	1 V
Output current LOW	I_{OL}	typ.	2,4 mA
Power consumption per package (no load)	P_{av}	typ.	300 mW
Operating ambient temperature	T_{amb}		0 to + 70 °C

PACKAGE OUTLINE

SAB1018A: 8-lead DIL; plastic (SOT-97A).

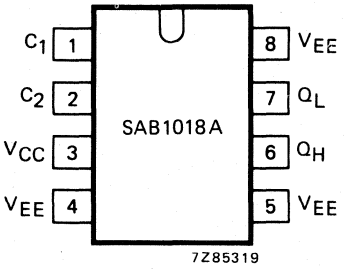


Fig. 2 Pinning diagram.

PINNING

V_{CC}	positive supply
V_{EE}	0 V; ground
C_1, C_2	differential inputs
Q_H, Q_L	complementary outputs

FUNCTIONAL DESCRIPTION

The circuit contains an amplifier, a divide-by-256 scaler and an output stage. It has been designed to be driven by a sinusoidal signal from the local oscillator of a TV tuner, with frequencies from 70 to 350 or 500 to 950 MHz, for a supply voltage of 5 V ± 5% and an ambient temperature of 0 to 70 °C.

The inputs are differential and are internally biased to permit capacitive coupling. For asymmetrical drive the unused input should be connected to ground via a 56 Ω resistor and a capacitor, to give approximately equal impedances at the two inputs of the amplifier.

The first divider stage will oscillate in the absence of an input signal; an input signal within the specified range will suppress this oscillation.

The outputs are complementary open-collector current sources. The output current edges are slowed down internally to reduce the harmonic contents of the signal. The external load and the supply voltage to which it is connected determine the output voltage.

There are three limitations to this output voltage and consequently to the load and to the supply voltage to which it is connected. Firstly it should not be possible under any circumstances that the output voltage becomes lower than 1,6 V below V_{CC}, to avoid saturation of the output transistor. Further it should not be possible that the output voltage becomes higher than 10 V, to avoid breakdown of the output transistor. Finally the output voltage swing should not be much larger than 1 V peak to peak, to keep the capacitive feedback to the inputs of the circuit small.

Wide, low-impedance ground connections and a short capacitive bypass from the V_{CC} pin to ground are recommended.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (d.c.)	V_{CC}	max.	7 V
Input voltage	V_i	0 to	V_{CC} V
Output voltage	V_o	max.	10 V
Storage temperature	T_{stg}	−55 to	+125 °C
Junction temperature	T_j	max.	125 °C

D.C. CHARACTERISTICS

V_{EE} = 0 V (ground); V_{CC} = 5 V; T_{amb} = 25 °C unless otherwise specified.

The circuit has been designed to meet the d.c. specifications as shown below, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed-circuit board.

Output voltage			
HIGH level	V_{OH}	max.	10 V
LOW level	V_{OL}	min.	V_{CC}−1,6 V
Output current			
at $V_{OL} = V_{CC} - 1{,}6$ V	I_{OL}	min.	2 mA
at $V_{OL} = V_{CC}$	I_{OL}	max.	2,8 mA
Supply current	I_{CC}	typ.	60 mA
		max.	75 mA

A.C. CHARACTERISTICS

V_{EE} = 0 V (ground); V_{CC} = 5 V ± 5%; T_{amb} = 0 to +70 °C.

Input voltage (see Fig. 3)			
f_i = 70, 350, 500 and 950 MHz	$V_{i(rms)}$		10 to 150 mV
Output rise time *	t_{TLH}	<	140 ns
Output fall time *	t_{THL}	<	140 ns

* Between 10% and 90% of observed waveform; R_L = 510 Ω; C_L = 60 pF.

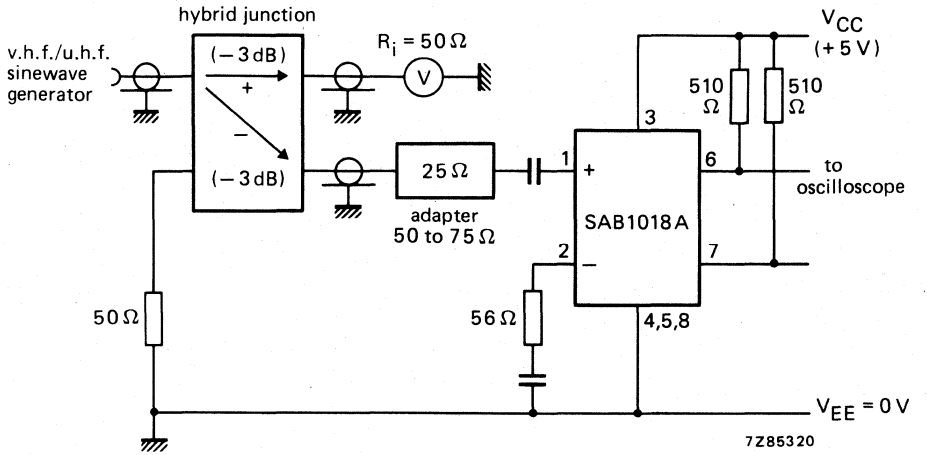


Fig. 3 Test circuit for defining input voltage.

- Cables must be 50 Ω coaxial.
- The capacitors are leadless ceramic (multilayer capacitors) of 10 nF.
- All connections to the device and to the meter must be kept short and of approximately equal lengths.
- Hybrid junction is ANZAC H-183-4 or similar.

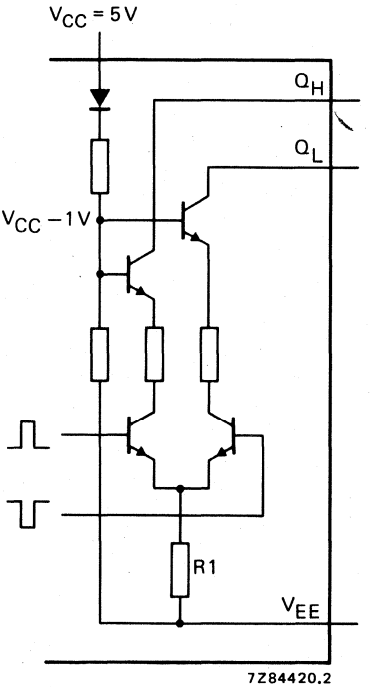


Fig. 4 Output stage.
Q_H = pin 6
Q_L = pin 7
V_{EE} = pin 8
V_{CC} = pin 3
R1 = 600 Ω

DEVELOPMENT SAMPLE DATA

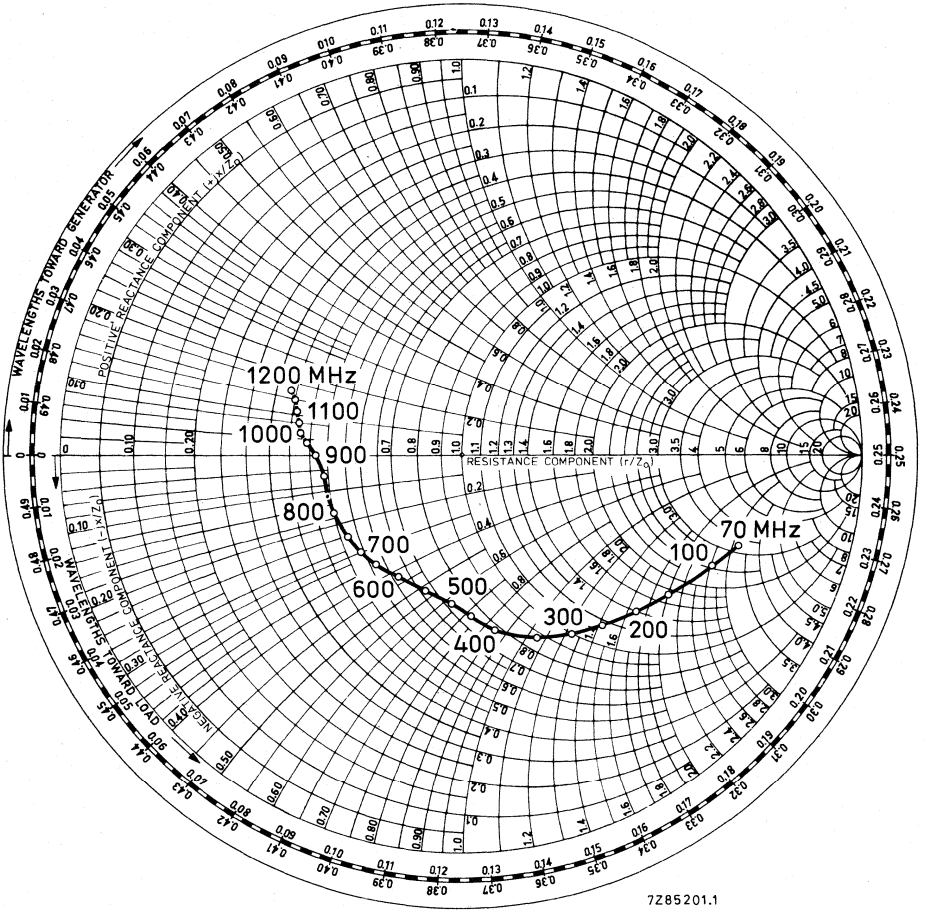


Fig. 5 Smith chart of typical input impedance.
$V_{i(rms)}$ = 25 mV; V_{CC} = 5 V; reference value = 75 Ω.

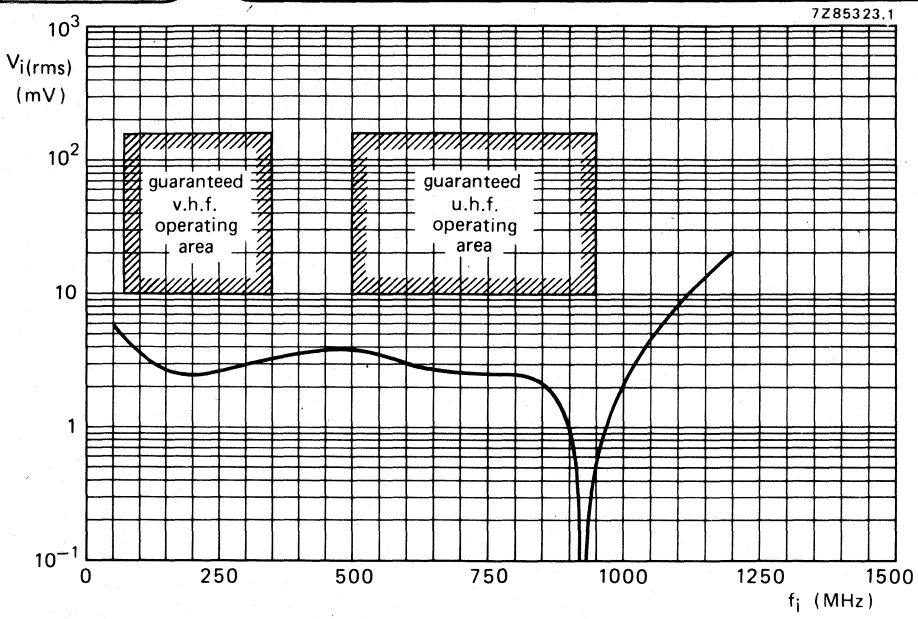


Fig. 6 Typical sensitivity curve under nominal conditions.

APPLICATION INFORMATION

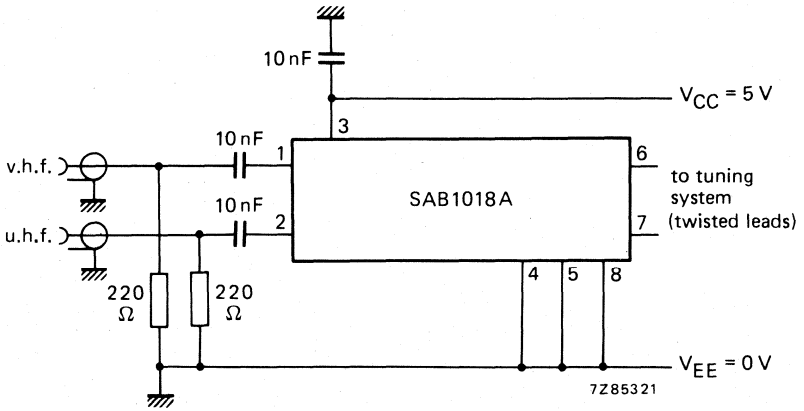
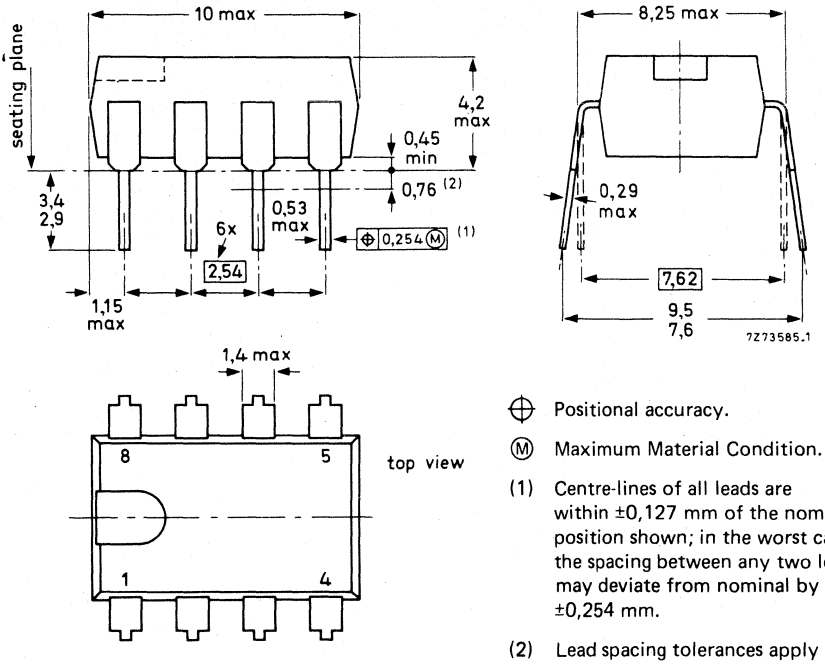


Fig. 7 Circuit diagram.

Application in a television tuning system. The output peak-to-peak voltage is about 1 V. For tuning circuits requiring a higher input voltage a transistor stage will be needed.

8-LEAD DUAL IN-LINE; PLASTIC (SOT-97A)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

SENSITIVE 1 GHz DIVIDER-BY-248/256

This silicon monolithic integrated circuit in current-mode logic is a dual-modulus prescaler for digital television tuning systems based on frequency synthesis. The device has separate band-selected inputs for the v.h.f. and u.h.f. oscillator signals.

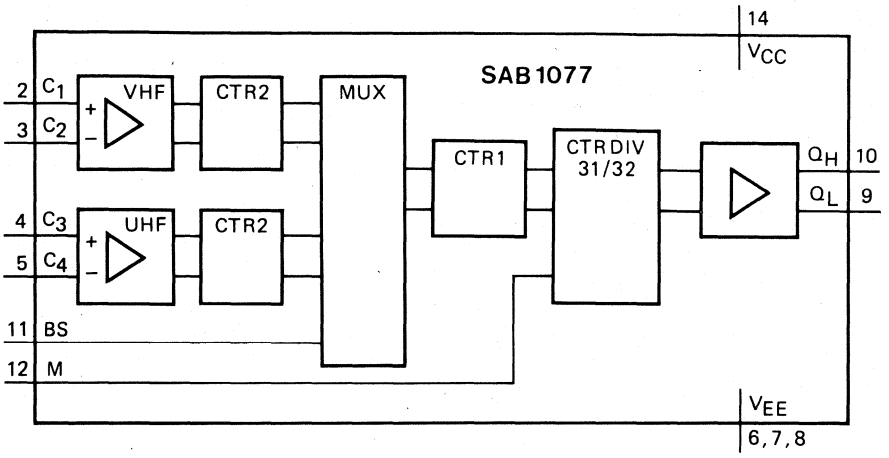


Fig. 1 Block diagram.

Pins 1 and 13 (not connected) preferably grounded or connected to V_{CC}.
CTR2 = 2 binary dividers (÷ 4); CTRDIV 31/32 = divider-by-31 or 32.

QUICK REFERENCE DATA

Supply voltage	V_{CC}	5 ± 5%	V
Input frequency range, v.h.f.	f_{2-3}	70 to 350	MHz
Input frequency range, u.h.f.	f_{4-5}	500 to 950	MHz
Count input voltage	$V_{i(rms)}$	> 7	mV
Output voltage swing	$V_{o(p-p)}$	typ. 1	V
Power consumption per package (no load)	P_{av}	typ. 200	mW
Operating ambient temperature	T_{amb}	0 to 70	°C

PACKAGE OUTLINE

SAB1077T: 14-lead flat pack; plastic (SO-14; SOT-108A).
SAB1077P: 14-lead DIL; plastic (SOT-27S, T, V).

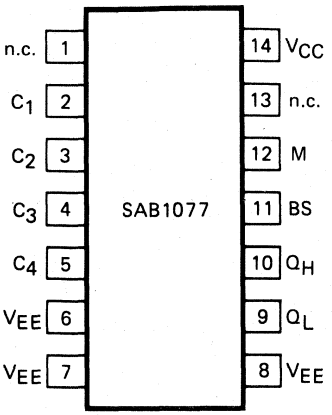


Fig. 2 Pinning diagram.

V_{CC}	positive supply
V_{EE}	0 V; ground
C_{1-2}	differential v.h.f. inputs
C_{3-4}	differential u.h.f. inputs
Q_H; Q_L	complementary outputs
M	mode control input
BS	band select input
n.c.	not connected (pins preferably grounded or connected to V_{CC})

FUNCTIONAL DESCRIPTION

Count inputs

The differential count inputs are made equally well suited for asymmetrical and symmetrical drive by a sinusoidal signal from the local oscillator of a television tuner. Two sets of count inputs are present, one for oscillator frequencies for the v.h.f. band including the S channels, 70 to 350 MHz, the other for the u.h.f. band (500 to 950 MHz). These inputs are internally biased to permit capacitive coupling. For asymmetrical drive the unused input of each pair should be connected to ground via a capacitor. Symmetrical drive by a coupling loop is possible with a single capacitor.

The first divider stage oscillates in the absence of an input signal, giving an output signal corresponding with an input frequency of about 350 or 850 MHz when either the v.h.f. or the u.h.f. input is activated. An input signal within the specified range suppresses the oscillation.

Band select

The band select input enables one input section and switches off the other. It may either be driven by a band select signal from a MOS circuit or by the supply voltage of the u.h.f. tuner, provided that the voltage limits on this input are not exceeded.

Mode control

The mode control input selects the division ratio. The input is internally biased to the HIGH level. It may be driven by an open-drain output. For a fixed division ratio of 256 it may be left open. To change the division ratio of a particular counting cycle the mode control signal should have attained its new level before a counting cycle of 232 input cycles is completed. See timing diagram (Fig. 3).

Outputs

The outputs are complementary open-collector current sources. The external load and the supply voltage to which this load is connected determine the output voltage. They should be chosen such that the 10 V rating will not be exceeded, that the output voltage will not drop more than 1,6 V below V_{CC}, and that the output voltage swing will not substantially exceed 1 V.

The output current edges are slowed down internally to reduce the harmonic contents of the output signal. Radiation by the output signal may be reduced further by transporting the two complementary signals via twisted wire or flat cable, even if only one signal is to be used to drive the subsequent circuit.

If radiation is no problem the unused output may be connected directly to the supply, preferably to the supply of the tuning system or alternatively to V_{CC}.

Wide, low-impedance ground connections and a short capacitive bypass from the V_{CC} pin to ground are recommended.

Pins, marked n.c., preferably should be grounded or connected to V_{CC}.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (d.c.)	V_{CC}	max.	7	V
Input voltage (d.c.)				
count input	V_I		0 to V_{CC}	V
band select input	V_{11}		0 to 16	V
mode control input	V_{12}		0 to V_{CC}	V
Output voltage (d.c.)	V_O	max.	10	V
Storage temperature	T_{stg}		−55 to + 125	°C
Junction temperature	T_j	max.	125	°C

D.C. CHARACTERISTICS

V_{EE} = 0 V (ground); V_{CC} = 5 V; T_{amb} = 25 °C unless otherwise specified.

The circuit has been designed to meet the d.c. specifications as shown below, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed-circuit board.

Band select inputs			
input voltage HIGH level	V_{IH}		2,6 to 16 V
input voltage LOW level	V_{IL}		0 to 1 V
input current at V_I = 12 V	I_{IH}	<	1,2 mA
input current at V_I = 0 V	$-I_{IL}$	<	10 μA
Mode control input			
input voltage HIGH level	V_{IH}		2,9 to 5 V
input voltage LOW level	V_{IL}		0 to 2,5 V
input current at V_I = 5 V	I_{IH}	<	10 μA
input current at V_I = 0 V	$-I_{IL}$	<	0,6 mA
Output voltage			
HIGH level	V_{OH}	<	10 V
LOW level	V_{OL}	>	V_{CC}−1,6 V
Output current			
at $V_O = V_{CC}$−1,6 V	I_{OL}	>	1 mA
at $V_O = V_{CC}$	I_{OL}	<	1,5 mA
Supply current			
at band select = L (v.h.f. enabled)	I_{CC}	typ.	35 mA
		<	45 mA
at band select = H (u.h.f. enabled)	I_{CC}	typ.	45 mA
		<	55 mA

A.C. CHARACTERISTICS

V_{EE} = 0 V (ground); V_{CC} = 5 V ± 5%; T_{amb} = 0 to + 70 °C.

Count input voltage (see Fig. 3)			
f_i = 70, 350, 500 and 950 MHz	$V_{i(rms)}$		7 to 150 mV
Count input voltage standing-wave ratio; $V_{i(rms)}$ = 25 mV; reference 75 Ω			
f_i = 70 to 350 MHz	VSWR	<	6
f_i = 500 to 950 MHz	VSWR	<	4
Propagation delay time (see Fig. 3) R_L = 820 Ω; C_L = 15 pF			
$C_n \longrightarrow Q_L$;	t_{PLH}	<	90 ns
$C_n \longrightarrow Q_H$;	t_{PHL}	<	90 ns
Set-up time (see Fig. 3)			
M $\longrightarrow$ C_n	t_{su}	>	0 ns

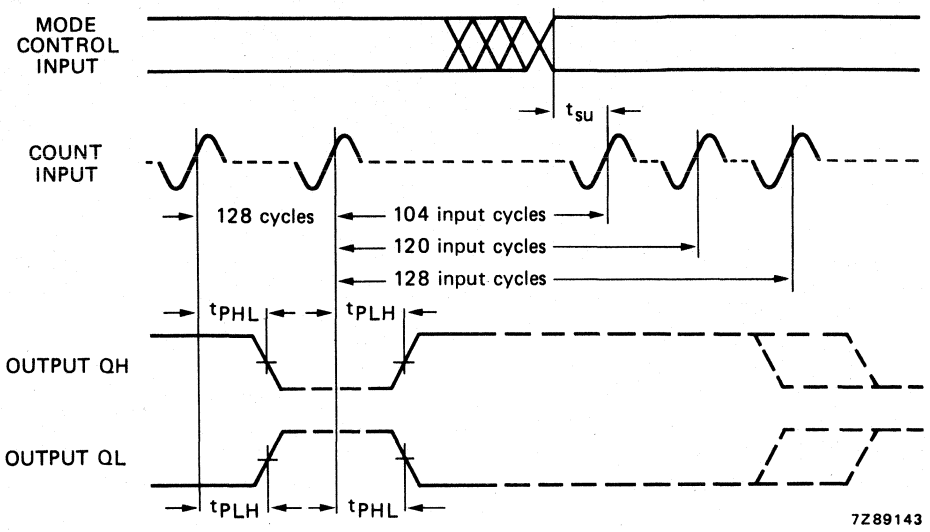


Fig. 3 Definition of propagation delay times and set-up time.

A positive set-up time is required (t_{su} = min. 0 ns). When the mode control signal has reached the LOW level before a counting cycle of 128 + 104 = 232 input cycles is completed, then the counting cycle will be terminated after 128 + 120 = 248 input cycles; a HIGH level extends the counting cycle to 128 + 128 = 256 input cycles.

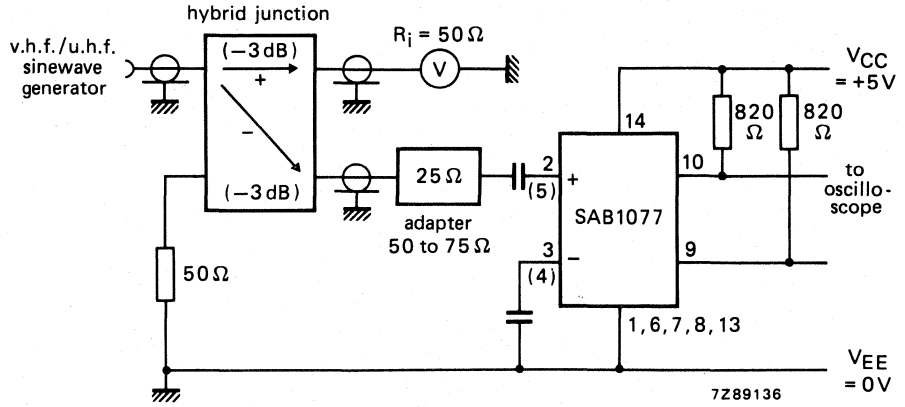


Fig. 4 Test circuit for defining input voltage.

- Cables must be 50 Ω coaxial.
- The capacitors should be low-inductance types e.g. leadless ceramic (multilayer capacitors) of 10 nF.
- All connections to the device and to the meter must be kept short and of approximately equal lengths.
- Hybrid junction is ANZAC H-183-4 or similar.

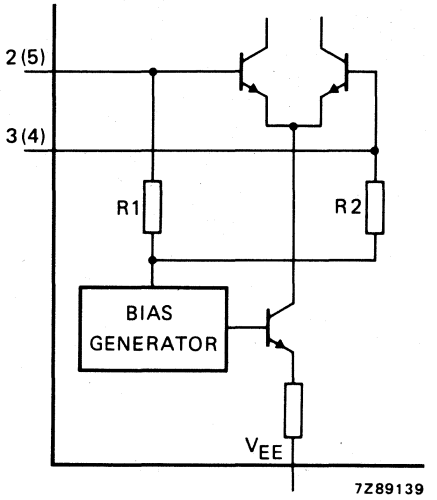


Fig. 5 Count input configuration.
v.h.f.: input pins 2 and 3.
$R_1 = R_2 = 200\ \Omega$.
u.h.f.: input pins 4 and 5.
$R_1 = R_2 = 330\ \Omega$.

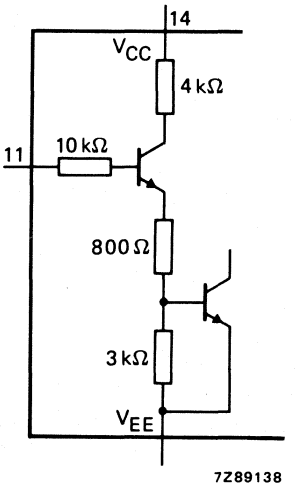


Fig. 6 Band select input.

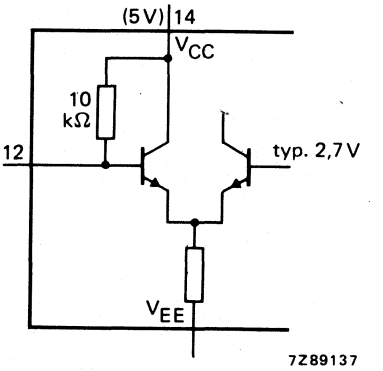


Fig. 7 Mode control input.

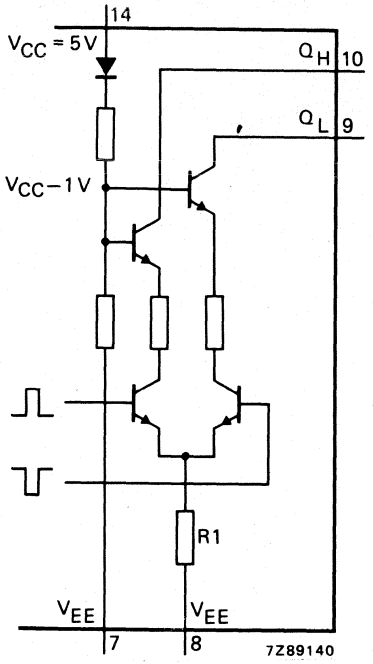


Fig. 8 Configuration of the output stage.
R_1 = 1,6 kΩ

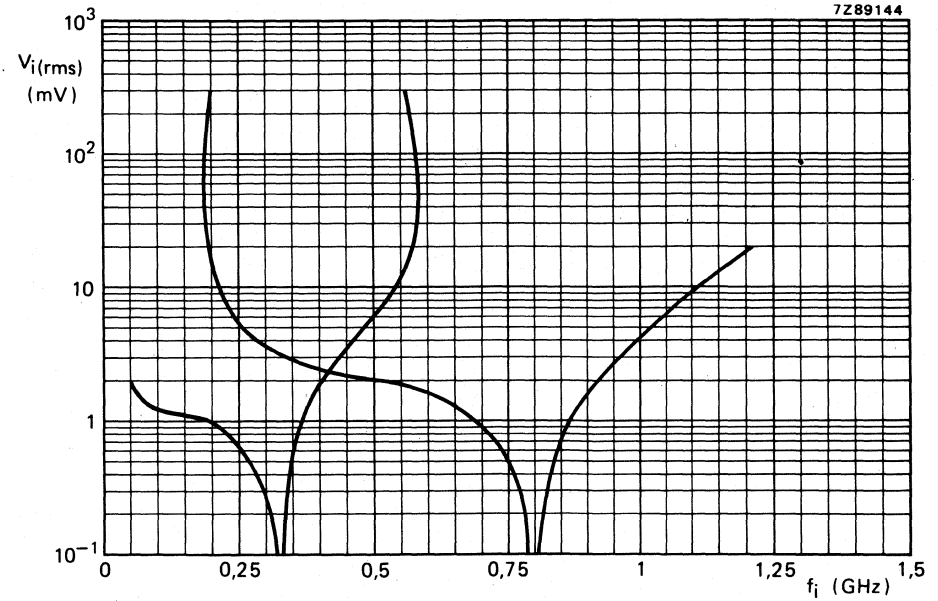


Fig. 9 Typical sensitivity curves under nominal conditions. V_{CC} = 5 V; T_{amb} = 25 °C.

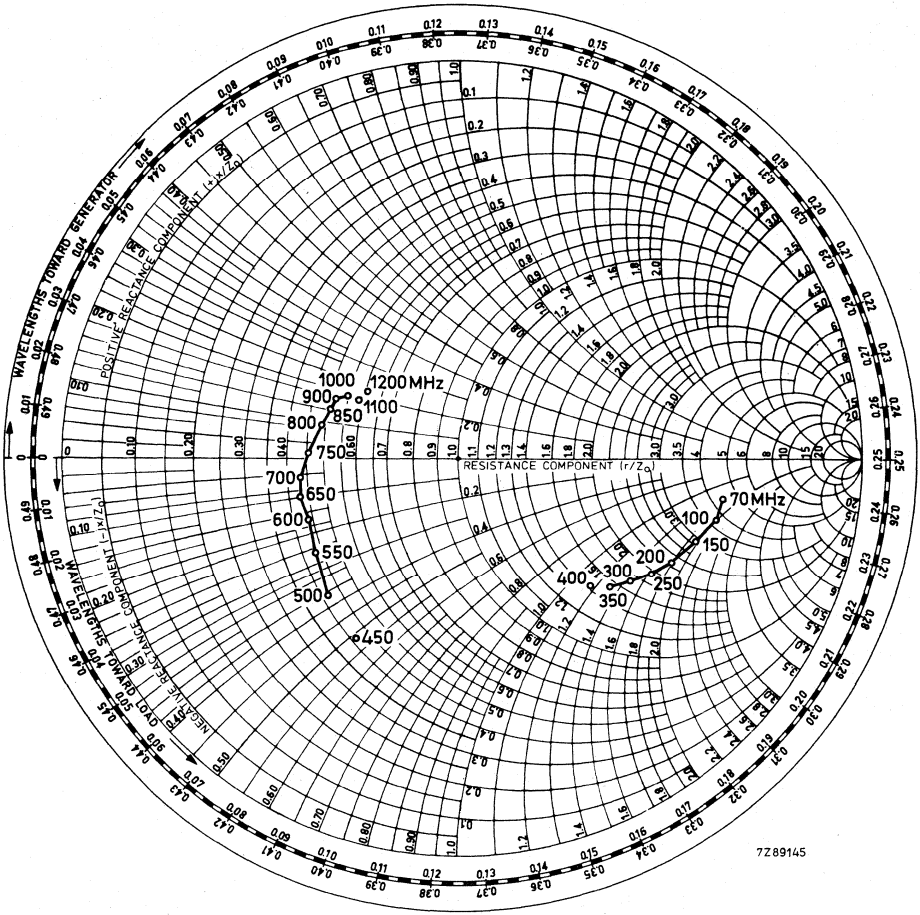


Fig. 10 Smith chart of typical input impedance.
$V_{i(rms)}$ = 25 mV; V_{CC} = 5 V; reference 75 Ω.

APPLICATION INFORMATION

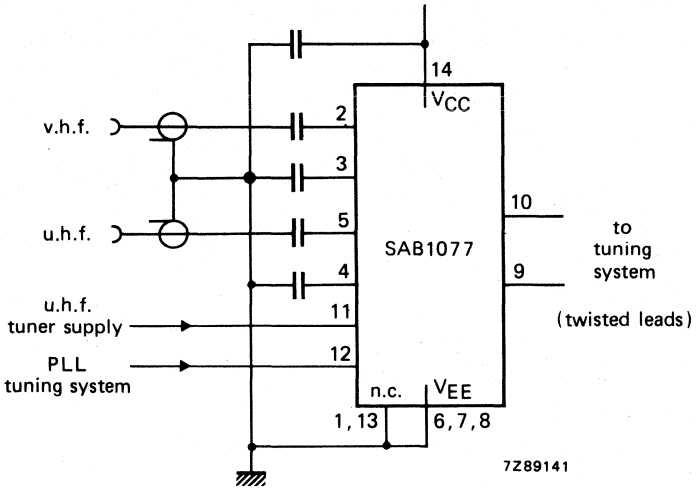
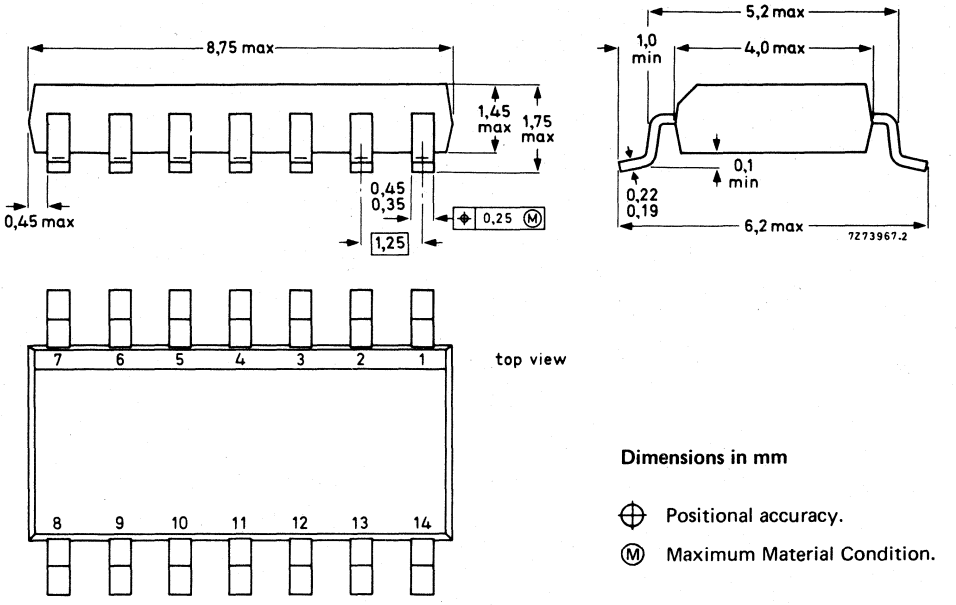


Fig. 11 Circuit diagram for application in a television tuning system.

For a fixed division ratio of 256 pin 12 may be left open. Ideally the load resistor is located near the subsequent tuning circuit. A tuning circuit that is not capable of being driven by a signal with a peak-to-peak voltage of about 1 volt will need an interface circuit.

14-LEAD FLAT PACK; PLASTIC (SO-14; SOT-108A)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

SOLDERING

The reflow solder technique

The preferred technique for mounting miniature components on hybrid thick or thin-film circuits is reflow soldering. Solder is applied to the required areas on the substrate by dipping in a solder bath or, more usually, by screen printing a solder paste. Components are put in place and the solder is reflowed by heating.

Solder pastes consist of very finely powdered solder and flux suspended in an organic liquid binder. They are available in various forms depending on the specification of the solder and the type of binder used. For hybrid circuit use, a tin-lead solder with 2 to 4% silver is recommended. The working temperature of this paste is about 220 to 230 °C when a mild flux is used.

For printing the paste onto the substrate a stainless steel screen with a mesh of 80 to 105 μm is used for which the emulsion thickness should be about 50 μm. To ensure that sufficient solder paste is applied to the substrate, the screen aperture should be slightly larger than the corresponding contact area.

The contact pins are positioned on the substrate, the slight adhesive force of the solder paste being sufficient to keep them in place. The substrate is heated to the solder working temperature preferably by means of a controlled hot plate. The soldering process should be kept as short as possible: 10 to 15 seconds is sufficient to ensure good solder joints and evaporation of the binder fluid.
After soldering, the substrate must be cleaned of any remaining flux.

650 MHz DIVIDE BY 10/11 PRESCALER

This silicon monolithic integrated circuit is a high speed prescaler. It will divide by either 10 or 11 over a frequency range from d.c. to typically 350 MHz (SAB1078) or 650 MHz (SAB1078A).

The divide by 10 or 11 capability allows the use of pulse swallowing techniques to control high speed counting modules by lower speed circuits. An internal extra gate makes it readily cascadable without using additional ECL clocks.

- Divide by 10/11 Mode Control
- TTL and complementary ECL outputs
- Pull-up resistors or Mode Control inputs for TTL compatibility
- Internal input pull-down resistors
- Internal biasing reference for a.c. coupled clocking
- Count gating input
- Asynchronous Reset for initializing
- Readily cascadable

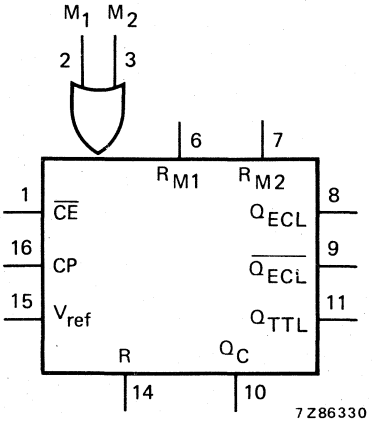


Fig. 1 Logic diagram.

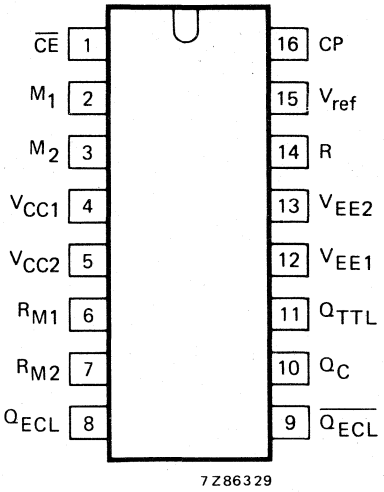


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE1} = V_{EE2} = -5{,}2$ V.

QUICK REFERENCE DATA

			SAB1078	SAB1078A	
Maximum input frequency	f_i	typ.	280	600	MHz
Operating ambient temperature	T_{amb}		0 to + 70		°C
Lower consumption per package	P_{av}	typ.	600		mW
Supply voltage	V_{EE1}	typ.	−5,2 ± 5%		V
Output voltage	V_{OH}, V_{OL}		ECL and TTL levels		V

PACKAGE OUTLINE (see Package Outlines).

SAB1078P; AP: plastic 16-lead dual in-line (SOT-38).
SAB1078D; AD: ceramic 16-lead dual in-line (SOT-74).

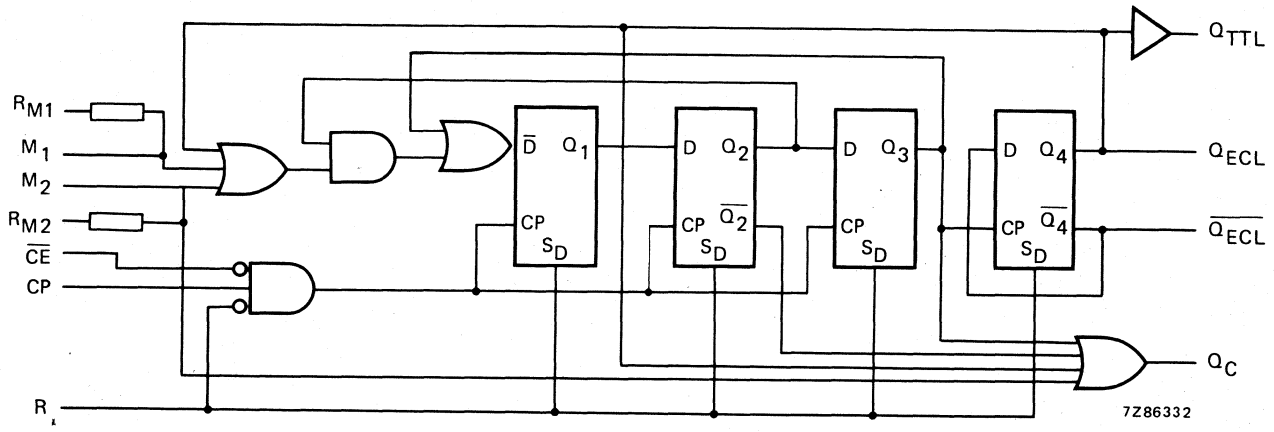


Fig. 3 Logic diagram.

Note: This diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many internal functions are achieved more efficiently than shown.

PIN DESIGNATIONS AND NAMES

1	$\overline{CE}$	Count Enable (active LOW)	11	Q_{TTL}	TTL output
2, 3	M1, M2	Mode Control inputs	12	V_{EE1}	Negative side of supply
4, 5	V_{CC1}, V_{CC2}	Positive side of supply	13	V_{EE2}	Negative side of supply for TTL output
6, 7	R_{M1}, R_{M2}	Resistors to M1, M2	14	R	Overriding reset input
8, 9	Q_{ECL}, $\overline{Q_{ECL}}$	Complementary ECL outputs	15	V_{ref}	Internal reference for count input
10	Q_C	Cascade output	16	CP	Count pulse

FUNCTIONAL DESCRIPTION

The SAB1078 contains four ECL flip-flops, an ECL to TTL converter and a Schottky TTL output buffer with an active pull-up. Three of the flip-flops operate as a synchronous shift counter driving the fourth flip-flop, operating as an asynchronous toggle. The internal feedback logic is such that the TTL output and the Q_4 output are HIGH for six clock periods and LOW for five clock periods. The Mode Control (M) inputs can modify the feedback to make the output HIGH for five clock periods and LOW for five clock periods, as indicated in the count sequence table.

When the output of the flip-flops are in the HHLL state shown in the table, M2 input state will be present on Q_C. The usefulness of this Q_C output lies in the timing required at the mode control pins when cascading two dividers. A low signal at both of these pins causes a ÷|| cycle to start each time the output Q_4 goes HIGH; thus, to achieve a single ÷|| cycle, the low pulse at the M pin must be shorter than one output period. If two 10/11 are cascaded, the faster counter requires, a narrower M pulse: that is the Q_C cascade out signal of the slower divider. The Q_C output is designed for driving the M input of the faster divider without any interfacing.

The feedback logic is such that at the instant the output goes HIGH, the circuit is already commited as to whether the output period will be 10 or 11 clock periods long. This means that subsequent changes in an M input signal, including decoding spikes, will have no effect on the current output period. The only timing restriction for an M input signal is that it be in the desired state at least a set-up time before the clock that follows the HHLL state shown in the table. The allowable propagation delay through external logic to an M input is maximized by designing it to use the positive transition of the SAB1078 output as its active edge. This gives an allowable delay of ten clock periods, minus the C to Q delay of the SAB1078 and the M to C set-up time. If the external logic uses the negative output transition as its active edge, the allowable delay is reduced to five clock periods minus the aforementioned delay and set-up time.

Capacitively coupled triggering is simplified by the 400 Ω resistor which connects pin 15 to the internal V_{BB} reference. By connecting this to the C input, as shown in Fig. 4 the clock is automatically centred about the input threshold. A clock duty factor of 50% provides the fastest operation, since the flip-flops are master/slave types with offset clock thresholds between master and slave. This feature ensures that the circuit will operate with clock waveforms having very slow rise and fall times, and thus, there is no minimum frequency restriction. Recommended minimum and maximum clock amplitude as a function of a frequency and temperature are shown in Fig. 8. When the C or any other input is driven from another ECL circuit, normal ECL termination methods are recommended. One method is indicated in Fig. 5.

When an M input is to be driven from a TTL output operating from the same V_{CC} and ground (V_{EE}), the internal 2 kΩ resistor can be used to pull the TTL output up as shown in Fig. 6. Some types of TTL putputs will only pull up to within two diode drops of V_{CC} which is not high enough for SAB1078 inputs. The resistor will pull the signal up through the threshold region, although this final rise may be somewhat slow, depending on wiring capacitance. A resistor network that gives faster rise and also lower impedance is shown in Fig. 7.

The ECL outputs have no pull-down resistors and can drive series or parallel terminated transmission lines. For short interconnections that do not require impedance matching, a 270 Ω to 510 Ω resistor to V_{EE} can be used to establish the V_{OL} level. Both V_{CC} pins must always be used and should be connected together as close to the package as possible. Pin 12 must always be connected to the V_{EE} side of the supply, while pin 13 is required only if the TTL output is used. Low impedance V_{CC} and V_{EE} distribution and r.f. bypass capacitors are recommended to prevent crosstalk with other circuits.

COUNT SEQUENCE TABLE

	Q_1	Q_2	Q_3	Q_4 (Q_{TTL})		Q_C
	H	H	H	H	÷ 11	H
÷ 10	L	H	H	H		H
	L	L	H	H		H
	L	L	L	H		H
	H	L	L	H		H
	H	H	L	H		H
	L	H	H	L		H
	L	L	H	L		H
	L	L	L	L		H
	H	L	L	L		H
	H	H	L	L		M_2

Note: A HIGH or R forces all outputs HIGH.

OPERATING MODE TABLE

inputs				output response
R	C_E	M_1	M_2	
H	X	X	X	set HIGH
L	H	X	X	hold
L	L	L	L	÷ 11
L	L	H	X	÷ 10
L	L	X	H	÷ 10

X = immaterial.

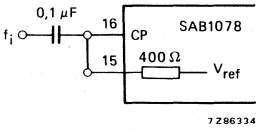
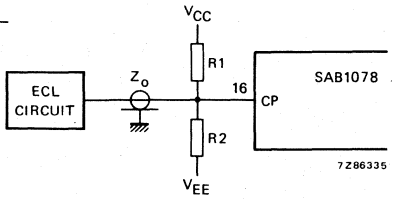


Fig. 4 Capacitively coupled clocking.



Z_o	50	75	100	Ω
R_1	81	122	163	Ω
R_2	130	195	260	Ω

Fig. 5 Clocking by ECL source via terminated line.

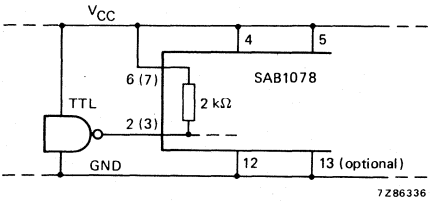


Fig. 6 Using internal pull-up with TTL Source.

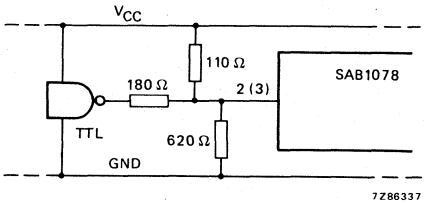


Fig. 7 Faster low impedance TTL to ECL interface.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (d.c.)	V_{EE}	max.	−7 V
Input voltage	V_i		V_{EE} to V_{CC} V
Output voltage	V_o	max.	V_{EE} to V_{CC} V
Storage temperature	T_{stg}		−55 to + 125 °C
Junction temperature	T_j	max.	125 °C

D.C. CHARACTERISTICS *TTL INPUT/OUTPUT OPERATION*

T_{amb} = 0 °C to + 75 °C. $V_{CC1} = V_{CC2}$ = 0 to 7 V unless otherwise specified. $V_{EE1} = V_{EE2}$ = GND.

characteristic	symbol	limits			units	conditions
		min.	typ. note 1	max.		
Input HIGH voltage M_1 and M_2 inputs	V_{IH}		4,1		V	guaranteed input HIGH threshold voltage (note 2); $V_{CC1} = V_{CC2}$ = 5,0 V
Input LOW voltage	V_{IL}		3,3		V	guaranteed input LOW threshold voltage (note 2); $V_{CC1} = V_{CC2}$ = 5,0 V
Output voltage HIGH Q_{TTL} output	V_{OH}	2,3	3,3		V	$V_{CC1} = V_{CC2}$ = min. I_{OH} = 640 μA
Output voltage LOW Q_{TTL} output	V_{OL}		0,2	0,5	V	$V_{CC1} = V_{CC2}$ = min. I_{OL} = 20 mA
Input current LOW M_1 and M_2 inputs	I_{IL}		−2,3	−5,0	mA	$V_{CC1} = V_{CC2}$ = max. V_I = 0,4 V; pins 6, 7 = V_{CC}
Output short circuit	I_{SC}	−20	−60	−80	mA	$V_{CC1} = V_{CC2}$ = max. V_O = 0 V; pin 14 = V_{CC}

Notes

1. Typical limits are at V_{CC} = 5,0 V and T_{amb} = 25 °C.
2. The M_1 and M_2 threshold specifications are normally referenced to the V_{CC} potential, as shown in the ECL operation tables. Using V_{EE} (gnd) as the reference as in normal TTL practice, effectively makes the threshold vary directly with V_{CC}. Threshold is typically 1,3 V below V_{CC} (e.g. + 3,7 V at V_{CC} = + 5 V). A signal swing about threshold of ± 0,4 V is adequate, which gives the stated V_{IH} and V_{IL} values. The internal 2 kΩ resistors are intended to pull TTL outputs up to the required V_{IH} range, as discussed in the functional description and shown in Fig. 6.

A.C. CHARACTERISTICS *TTL OPERATION*

$V_{CC1} = V_{CC2}$ = nom. 5,0 V; $V_{EE1} = V_{EE2} = 0$ V (ground); $T_{amb} = 25\ ^{o}C$

characteristic	symbol	min.	typ.	max.	units	remarks
propagation delay rise and fall time CP → Q_{TTL}	t_{PLH} / t_{PHL}	6	12	14	ns	all limits to be fixed see Fig. 10
transition fall time	t_{TLH} / t_{THL}	–	5	–	ns	between 20% and 80% see Fig. 10

TTL output swing is guaranteed of f_c max. at T_{amb} = 0 to + 75 °C.

D.C. CHARACTERISTICS *ECL OPERATION*

$V_{CC1} = V_{CC2}$ = GND. $V_{EE1} = -5,2$ V.

characteristic	symbol	limits min.	limits typ.	limits max.	units	T_{amb} °C	conditions
Output voltage HIGH Q_{ECL} and $\overline{Q}_{ECL}$	V_{OH}	−1060 −1025 −980	−995 −960 −910	−905 −880 −805	mV	0 25 75	load = 50 Ω to −2 V
Q_C	V_{OH}	–	−1020	–	mV	25	no load
Output voltage LOW Q_{ECL} and $\overline{Q}_{ECL}$	V_{OL}	−1820	−1705	−1620	mV		load = 50 Ω to −2 V
Q_C	V_{OL}		−1620		mV	25	no load
Input voltage HIGH	V_{IH}	−1135 −1095 −1035		−840 −810 −720	mV	0 25 75	M_1 or M_2 can be connected to V_{CC} for fixed divide-by-ten operation
Input voltage LOW	V_{IL}	−1870 −1850 −1830		−1500 −1485 −1460	mV	0 25 75	
Input current HIGH C input R input M_1 and M_2 input	I_{IH}			 400 400 250	 μA	 25 25 25	 $V_I = V_{IH}$ max.
Input current LOW	I_{IL}	0,5			μA	25	$V_I = V_{IL}$ min.
Supply current	I_{EE}	−100	−75		mA	0 to 75	pins 6,7,13 not connected
Supply voltage range	V_{EE}	−5,7	−5,2	−4,7	V	0 to 75	

A.C. CHARACTERISTICS *ECL OPERATION*

T_{amb} = 0 °C to + 75 °C. $V_{CC1} = V_{CC}$ = GND. V_{EE1} = −5,2 V.

characteristics	symbol	limits					units	conditions
		0 °C	+ 25 °C			+ 75 °C		
		typ.	min.	typ.	max.	typ.		
Propagation delay C → Q_{ECL}	$\frac{t_{PLH}}{t_{PHL}}$	2,2	1,3	2,5	3,0	3,0	ns	
R → Q_{ECL}	$\frac{t_{PLH}}{t_{PHL}}$	1,7		2,0	6,0	3,5	ns	
Set-up time M → C	t_s	1,0	4,0	1,0		1,0	ns	R_L = 50 Ω to −2,0 V
Hold time M → C	t_h	−0,5	0,0	−0,5		−0,5	ns	
Transition time LOW to HIGH	t_{TLH}	1,0		1,0		1,0	ns	$t_r = t_f$ = 2,0 ± 0,1 ns (20% - 80%)
HIGH to LOW	t_{THL}	1,0		1,0		1,0	ns	see Fig. 10; between 20% and 80%
Maximum count freq. SAB1078	f_i max.	350	280	350		325	MHz	input pulse = $V_{i\,(p\text{-}p)}$ = 350 mV
SAB1078A		650	600	650		625		

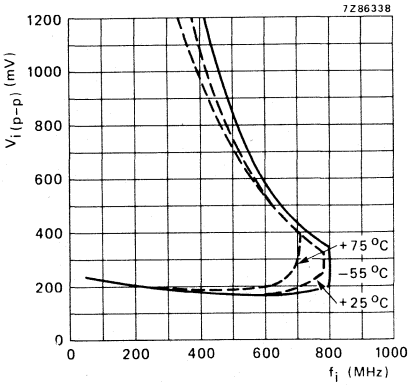


Fig. 8 A.C. coupled triggering characteristics.

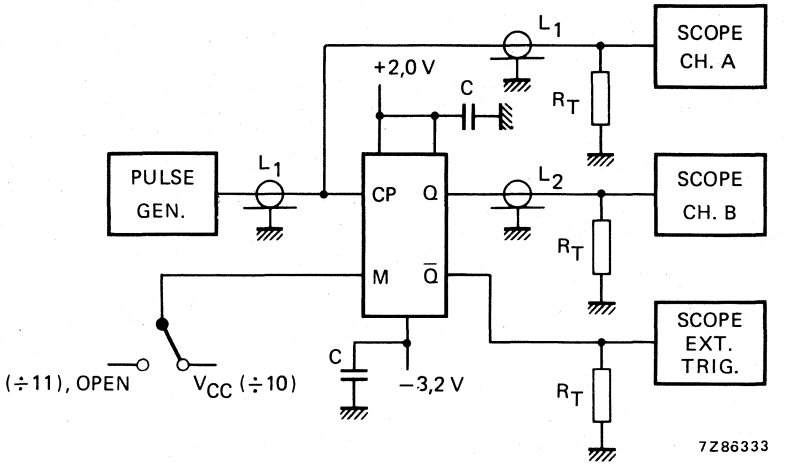


Fig. 9 Switching times test circuit.

V_{CC} = + 2,0 V
V_{EE} = −3,2 V
R_T = 50 Ω (scope input impedance)
C_L = jig and stray capacitance < 5,0 pF
L_1 = L_2 equal 50 Ω impedance lines
C = 0,1 pF

Notes

Use high impedance probes to test Q_{TTL}; connect pin 13 to V_{EE}.

For high frequency test use a.c. coupled input as in Fig. 4. Adjust input pulse $V_{i(p-p)}$ = 350 mV.

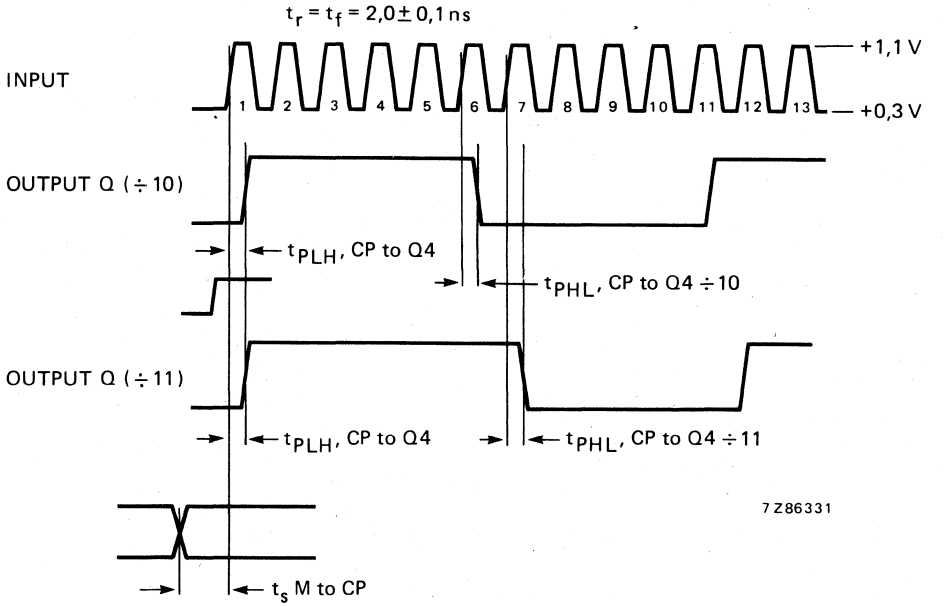


Fig. 10 Switching times test waveforms.

DUAL DIFFERENTIAL D-TYPE FLIP-FLOP

The silicon monolithic integrated circuit SAB1801D is an ECL dual D-type flip-flop with latch, including differential inputs and enabled outputs. The clock input is common to both flip-flops and each output gate is enabled by a common enable input. The input data (D) are registered at the output when the clock is HIGH and the output is latched by the negative transition of the clock (falling edge).

The SAB1801D is useful in applications such as phone repeaters, sensible line comparator-receivers and fast analogue-to-digital converters.

Features:

- fast propagation delay with low power dissipation;
- gated outputs for bus-oriented and line transmission codes applications;
- high fan-out capabilities (50 Ω lines);
- high immunity for power supply variations;
- fully compatible with ECL standard GX family.

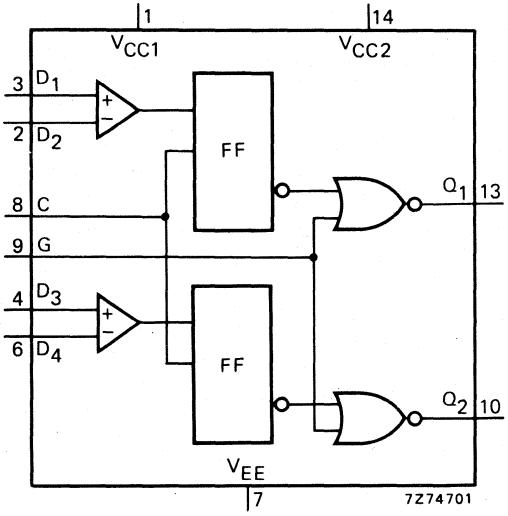
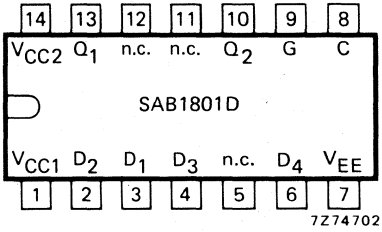


Fig. 1 Block diagram.



$V_{CC1} = V_{CC2} = 0$ V (ground)
$V_{EE} = -5{,}2$ V
Fig. 2 Pin designation.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 ± 10%	V
Operating frequency	f_{min}		110	MHz
Output voltage swing		typ.	840	mV
Operating ambient temperature	T_{amb}		0 to + 75	°C
Power consumption per package (no load)	P_{av}	typ.	310	mW

PACKAGE OUTLINE

14-lead DIL; ceramic (SOT-73).

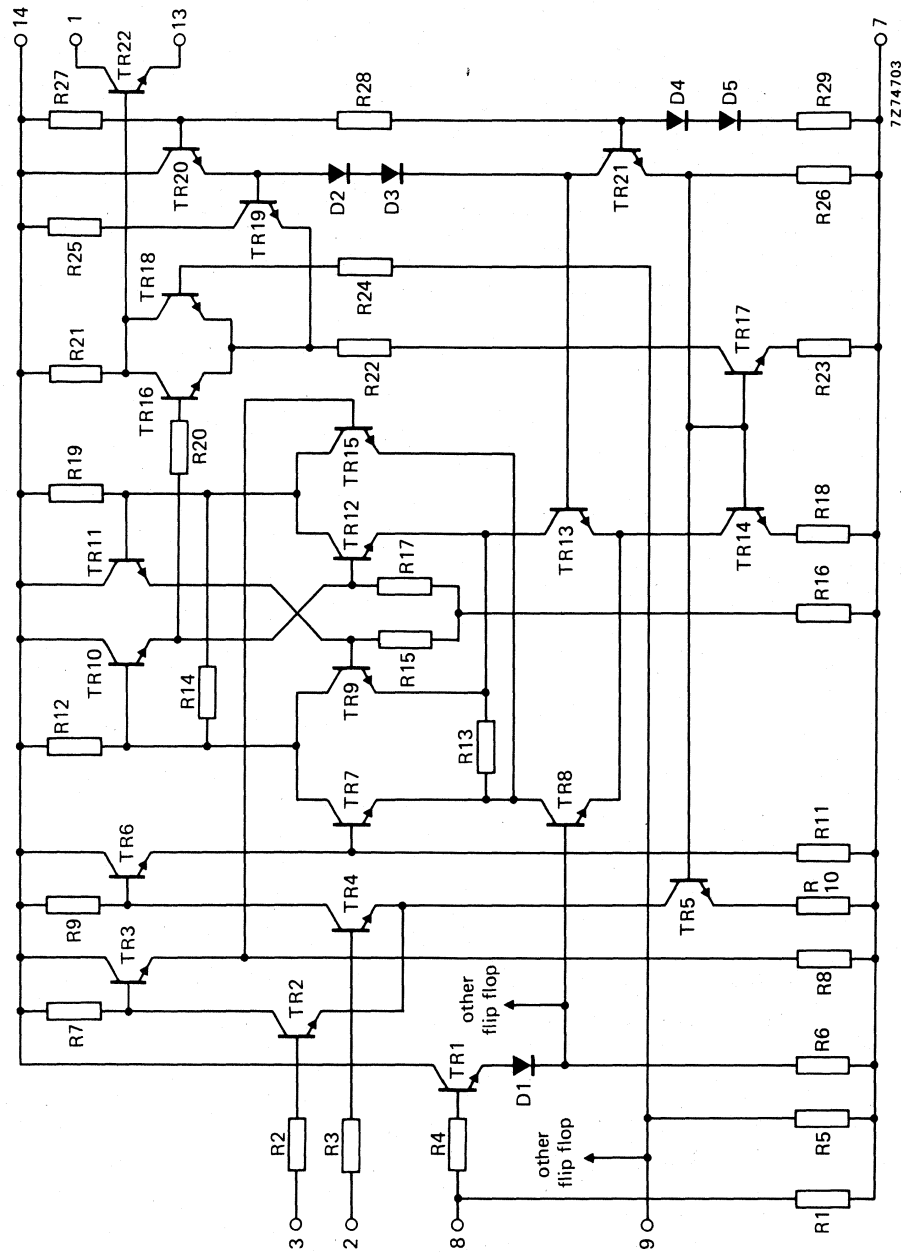


Fig. 3 Circuit diagram (½ circuit).

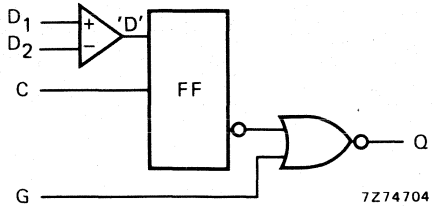


Fig. 4 Logic diagram (one flip-flop).

FUNCTION TABLE

G	C	'D'	Q_{n+1}
1	X	X	0
0	0	X	Q_n
0	1	0	0
0	1	1	1

Positive logic
1 = HIGH state (the more positive voltage) = H
0 = LOW state (the less positive voltage) = L
X = state is immaterial

'D' = HIGH when $V_{D1} - V_{D2} \geqslant 50$ mV
'D' = LOW when $V_{D1} - V_{D2} < 50$ mV

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (d.c.)	V_{EE}	max.	−8 V
Input voltage	V_I	0 to V_{EE}	V
Output current	I_O	max.	50 mA
Storage temperature	T_{stg}	−55 to +125	°C
Junction temperature	T_j	max.	125 °C

D.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 0$ V (ground); $V_{EE} = -5{,}2$ V

Each circuit has been designed to meet the d.c. specifications shown in the test table below, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed-circuit board and transverse air flow > 2,5 m/s is maintained.
Outputs are terminated via a 50 Ω resistor to −2,0 V. Test values for applied conditions are given in the table and defined in the figure.

Test table C and G inputs

T_{amb}	0	25	75	°C
V_{IHmax}	−0,840	−0,810	−0,720	V
V_{IHT}	−1,145	−1,105	−1,045	V
V_{ILT}	−1,490	−1,475	−1,450	V
V_{ILmin}	−1,870	−1,850	−1,830	V

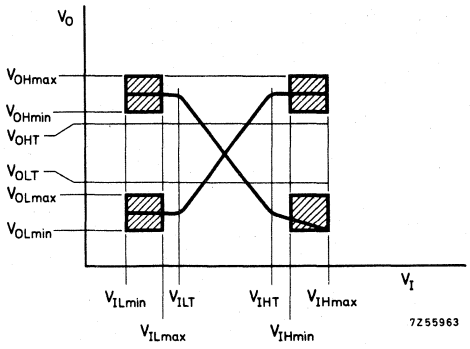


Fig. 5.

D.C. CHARACTERISTICS (continued)

Test table D^+ and D^- inputs

V_{IHmax}	−0,6 V
V_{ILmax} (the less negative input)	−3,0 V
V_{ILmin} (the more negative input)	−5,2 V

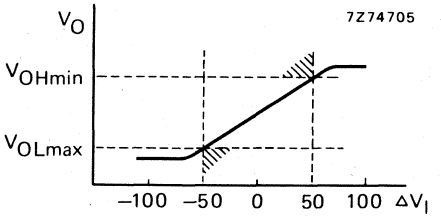


Fig. 6.

	symbol		pin under test	T_{amb} (°C) 0	25	75		conditions pin	test value
Output voltage HIGH	V_{OH}	min.		−1000	−960	−900	mV	9	V_{IHmin}
		typ.	13	–	−880	–	mV	8	V_{IHmax}
		max.		−840	−810	−720	mV	2,3	ΔV_I = 50 mV
Output voltage LOW	V_{OL}	min.		−1,870	−1,850	−1,830	V		
		typ.	13	–	−1,720	–	V	9	V_{IHmax}
		max.		−1,665	−1,650	−1,625	V		
Input current HIGH	I_{IH}	max.			45		μA		V_{IHmax}
Supply current	I_{EE}	typ.	every	–	–	–	mA	every	V_{ILmin}
		max.	input	–	60	–	mA	input	

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = +2$ V; $V_{EE} = -3{,}2$ V; $T_{amb} = 25$ °C

	symbol	pin under test	min.	typ.	max.		conditions: test voltage on pin	conditions: input pulse on pin
Propagation delay time								
C → Q	t_{pd}	13	2,2	3,6	5,4	ns	2,3 (note 1)	8
G → Q	t_{pd}	13	1,0	2,0	3,4	ns	8 0,31 V 2,3 (note 1)	9 (note 3)
Differential delay								
C → G	Δt_{CG}	13	1,3	1,6	1,9	ns	– –	–
$Q_1 \rightarrow Q_2$	$\Delta t_{Q_1Q_2}$	10,13	−0,25	0	0,25	ns	2,3 4,6 (note 1)	8
Set-up time	t_{su}	13	–	+0,5	–	ns	2,3 $\Delta V_I = 0{,}1$ V	8
			–	−0,5	–	ns	2,3 $\Delta V_I = 1$ V	8
Hold time	t_{hold}	13	–	+1,7	–	ns	2,3 $\Delta V_I = 0{,}1$ V	8
		13	–	+2,7	–	ns	2,3 $\Delta V_I = 1$ V	8
Rise time	t_r	13	1	1,5	2,5	ns	2,3 (note 1)	8
Fall time	t_f	13	1	1,5	2,5	ns	2,3 (note 1)	8

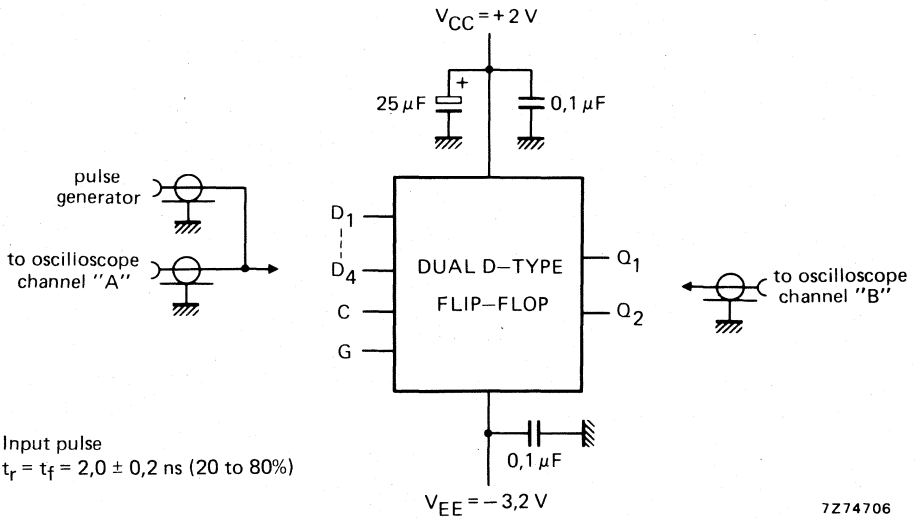


Fig. 7 Switching times test circuit.

Notes

1. See Fig. 8.
2. G-input (pin 9) must be connected to +0,31 V unless otherwise specified.
3. Input pulse on G identical to input pulse on C.

A.C. CHARACTERISTICS (continued)

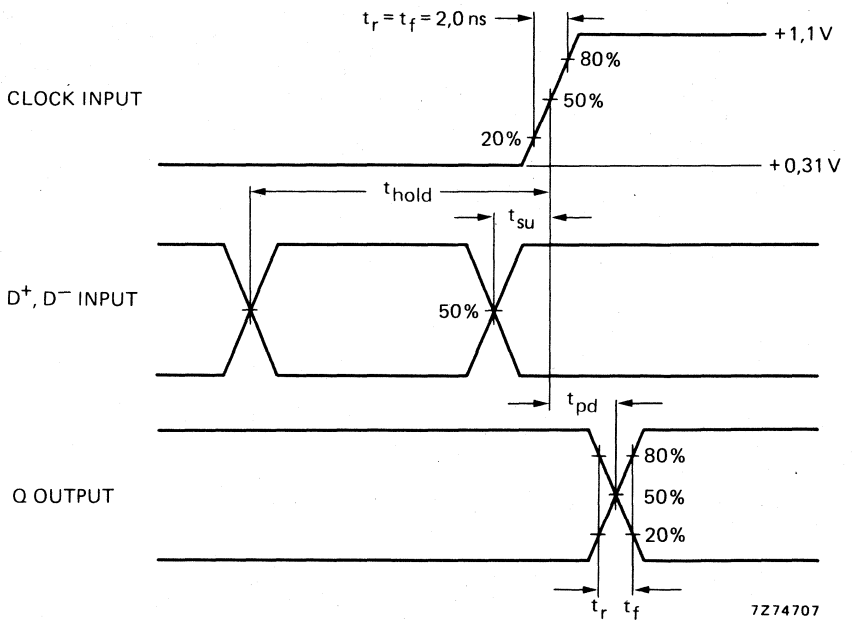


Fig. 8 Switching times waveforms.

t_{su} is the minimum time before (or after if negative) the positive transition of the clock pulse (C) that the information must be present at the D input.

t_{hold} is the maximum time before the positive transition of the clock pulse (C) that the information must be present at the D input.

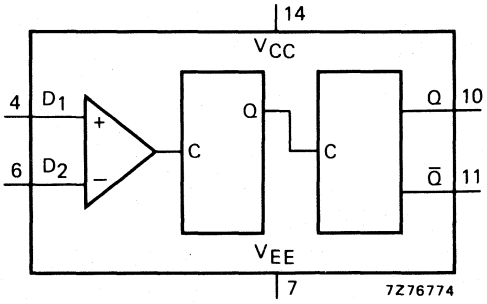
SUPERSEDES DATA SHEET OF JUNE 1977

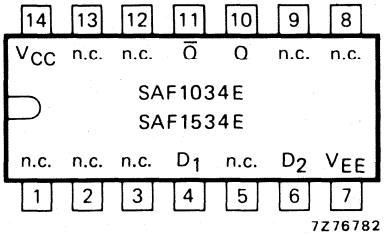
4-TO-1 DIVIDERS

The silicon monolithic integrated circuits SAF1034E and SAF1534E are ECL fixed-ratio divide-by-4 scalers for input frequencies in the ranges 70 MHz to 1,05 GHz (SAF1034E) and 100 MHz to 1,5 GHz (SAF1534E) and over an ambient temperature range of −40 to +85 °C.

The inputs of the circuits are differential and internally biased to permit capacitive coupling or asymmetrical drive. The ICs drive 50 Ω lines. The SAF1034E and SAF1534E are pin compatible with the Plessey SP8613 and SP8616B series v.h.f./u.h.f. divide-by-4 counters but are operated from standard ECL or TTL supply voltages.

Features:
- operation guaranteed over the whole band over an ambient temperature range of −40 to +85 °C;
- a.c. to d.c. coupled differential inputs;
- ECL or TTL power supply voltages;
- complementary emitter follower outputs, ECL compatible;
- 50 Ω line drive.





V_{CC} = 0 V (ground)

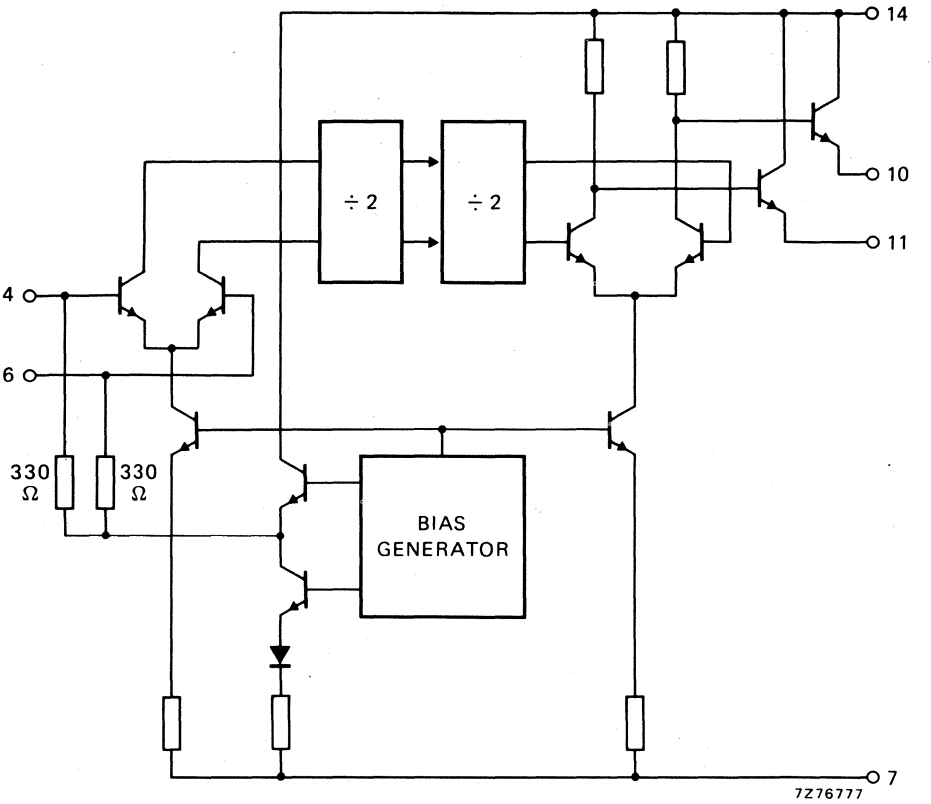
QUICK REFERENCE DATA

		SAF1034E	SAF1534E	
Input frequency range	f_i	70 to 1050	100 to 1500	MHz
Supply voltage	V_{EE}	−5,2 ± 10%		V
Input voltage range	V_I	0,2 to 1		V
Output voltage swing		typ 900		mV
Operating ambient temperature	T_{amb}	−40 to +85		°C
Power consumption per package	P_{av}	typ 250		mW

PACKAGE OUTLINE

14-lead DIL; metal-ceramic (SOT-83B).

CIRCUIT DIAGRAM



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (d.c.)	V_{EE}	max.	−7 V
Input voltage	V_I		−5,2 to 0 V
Output current	I_O	max.	50 mA
→ Storage temperature	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	125 °C

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5,2 V; the circuit has been designed to meet the d.c. specifications as shown below, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed-circuit board. Outputs are terminated via a 50 Ω resistor to −2 V. The outputs can also be terminated by 260 Ω to V_{EE}. Best results are obtained when both outputs are terminated via the same way.

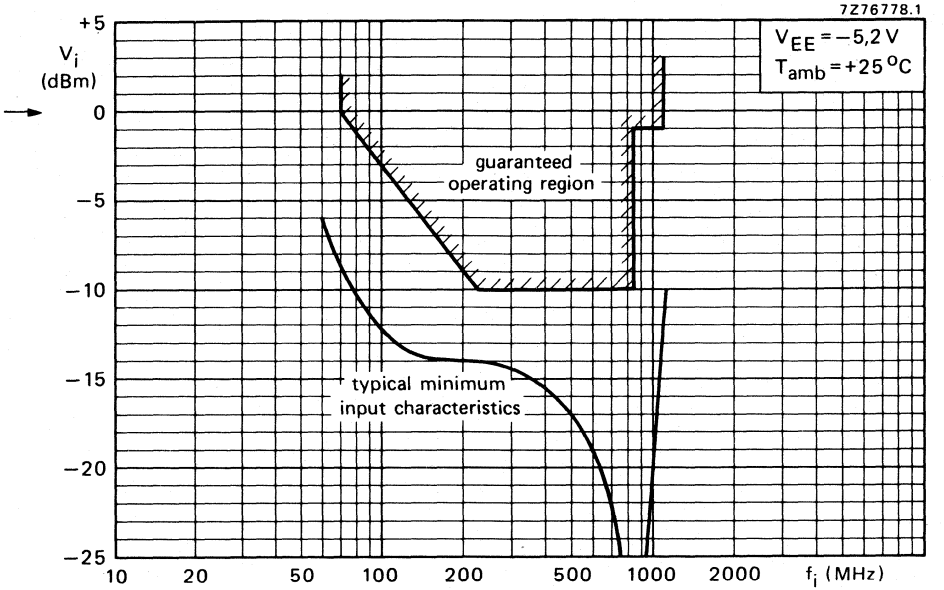
	symbol		pin under test	T_{amb} (°C) −40	25	85		conditions
Output voltage HIGH	V_{OH}	min.	10	−1100	−1060	−1020	mV	pin 6 open; pin 4 connected or unconnected
		typ.	or	—	—	—	mV	
		max.	11	−840	−810	−770	mV	
Output voltage LOW	V_{OL}	min.	10	−1925	−1905	−1885	mV	to −5,2 V as often as necessary for V_{OH} or V_{OL} at Q
		typ.	or	—	—	—	mV	
		max.	11	−1670	−1650	−1630	mV	
Reference voltage	V_{ref}	min.	4	−2750	−2750	−2750	mV	pins 4 and 6 open
		typ.	and	—	—	—	mV	
		max.	6	−2400	−2400	−2400	mV	
Supply current	I_{EE}	min.	7	—	−53	—	mA	pin 4: −5,2 V; pin 6: open
		typ.		—	—	—	mA	
Supply voltage	V_{EE}	min.	7	—	−5460	—	mV	
		typ.		—	−5200	—	mV	
		max.		—	−4940	—	mV	

A.C. CHARACTERISTICS

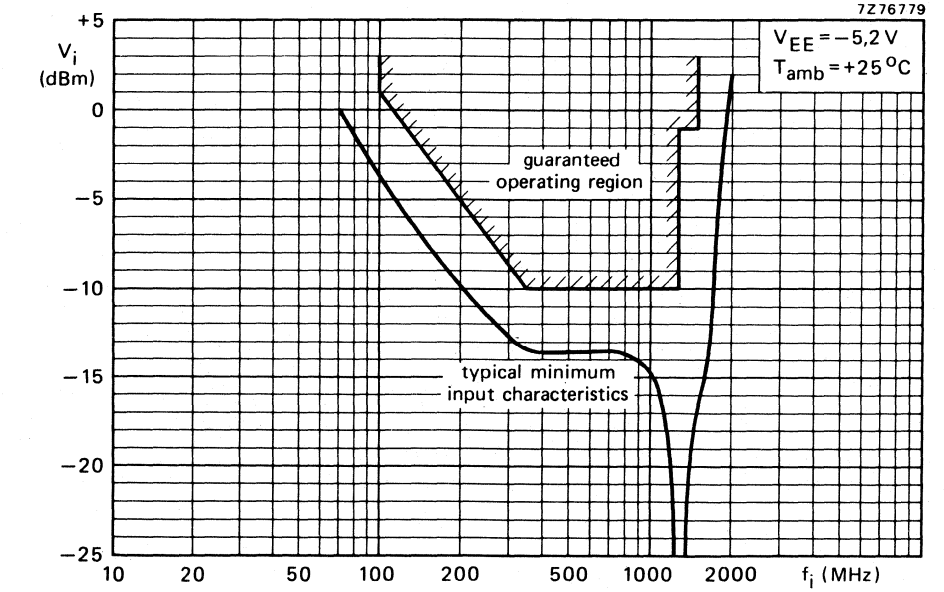
V_{CC} = 0 V (ground); V_{EE} = −5,2 V; T_{amb} = −40 to +85 °C

	symbol	pin under test	circuit under test	min	typ	max		conditions
Maximum input frequency	$f_{i\,max}$	10 or 11	SAF1034E	1050	—	—	MHz	sinusoidal input voltage $V_{i(p-p)}$ = 600 mV
			SAF1534E	1500	—	—	MHz	
Minimum input frequency	$f_{i\,min}$	10 or 11	SAF1034E	—	—	70	MHz	tested frequency on pin 10 or 11 is $f_i/4$.
			SAF1534E	—	—	100	MHz	
Minimum slew rate		10 or 11	SAF1034E	—	—	100	V/μs	square wave input to guarantee operation down to d.c.
			SAF1534E	—	—	160	V/μs	

A.C. CHARACTERISTICS (continued)

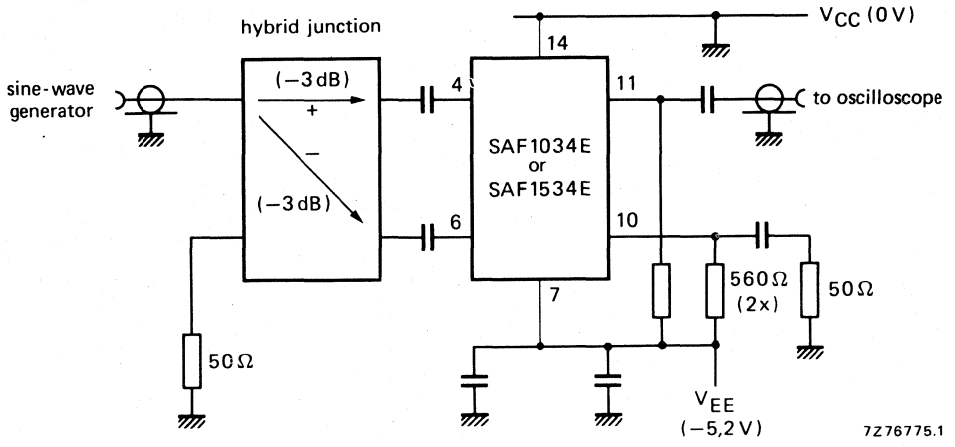


Triggering level requirements SAF1034E.



Triggering level requirements SAF1534E.

Test circuit (symmetrical drive)

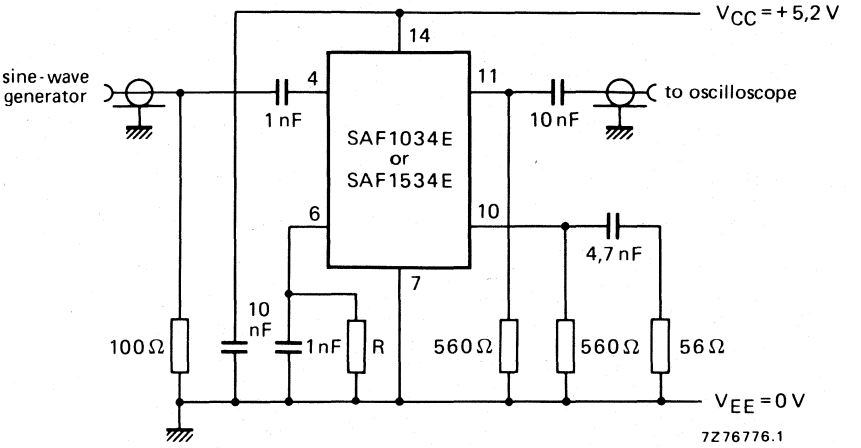


Notes

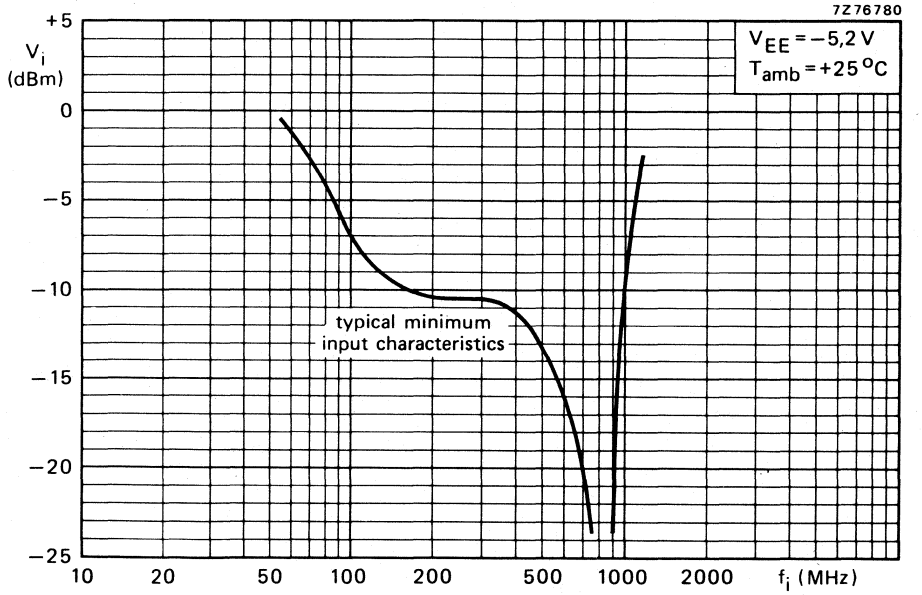
1. The capacitors are leadless ceramic (multilayer capacitors) of 10 nF.
2. All connections to the device must be kept short.
3. Input and output cables to the oscilloscope are 50 Ω coaxial cables.
4. All specified a.c. input voltages are measured at the output of the sine-wave generator with the hybrid junction disconnected.

A.C. CHARACTERISTICS (continued)

Test circuit (asymmetrical drive)



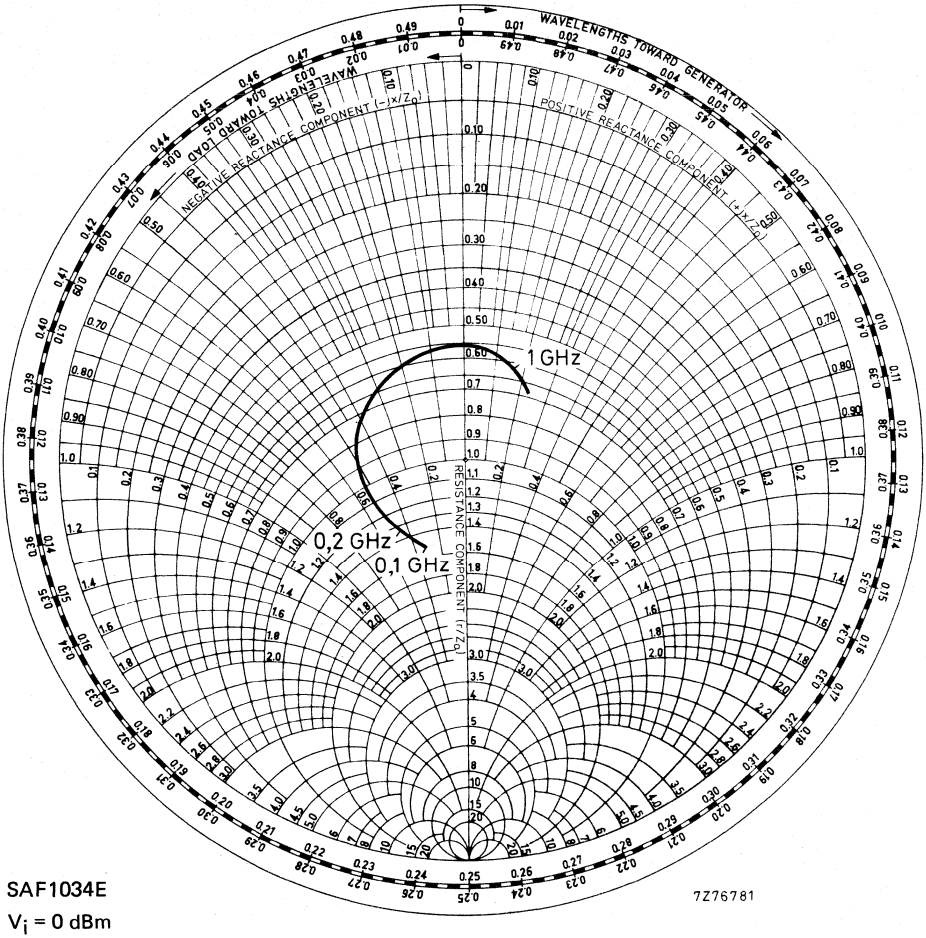
Resistor R can be added to prevent self oscillation when no input signal is present. The sensitivity is then reduced.



Operating range SAF1034E (asymmetrical drive).

DEVELOPMENT SAMPLE DATA

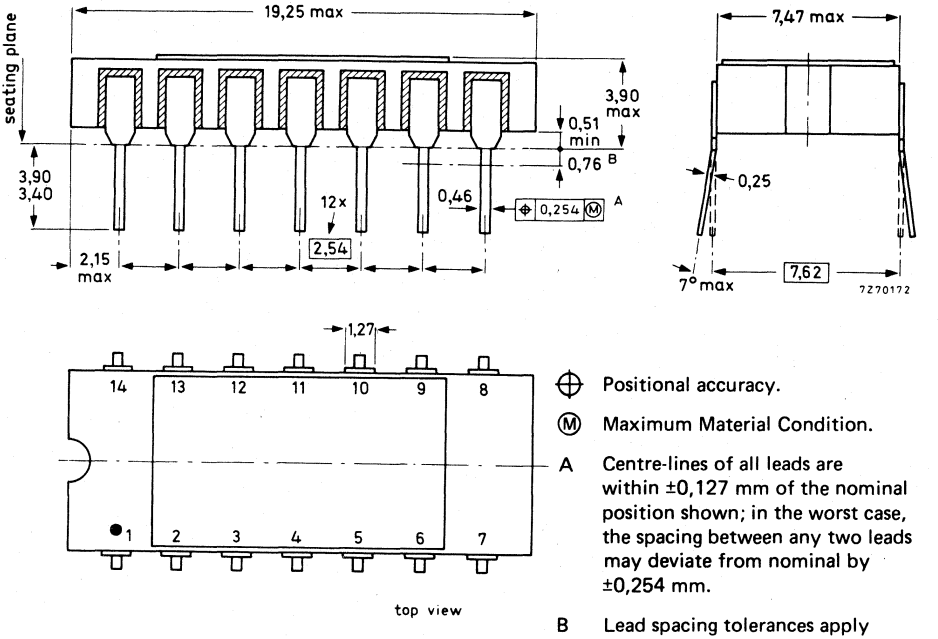
A.C. CHARACTERISTICS (continued)



SAF1034E
V_i = 0 dBm
V_{CC} = +5,2 V
T_{amb} = + 25 °C

Typical input SWR on 50 Ω.
(Asymmetrical drive; test set-up see page 6).

→ 14-LEAD DUAL IN-LINE; METAL-CERAMIC (SOT-83B)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

A Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

B Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

Remarks

1. Leads are given positive misalignment so that they grip after insertion.
2. Leads are Ni-Fe, pure tin plated.
3. → Side brazed, low profile.

DIGITAL INTEGRATED CIRCUITS - ECL

NUMERICAL AND FUNCTIONAL INDEX

GENERAL

FAMILY SPECIFICATIONS

LOGIC DIAGRAMS

PACKAGE OUTLINES

DEVICE DATA
GX family (ECL10 000)

DEVICE DATA
HX family (ECL100 000)

DEVICE DATA
Dedicated designs

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